BucklingBeam

Silicon Valley Test Workshop

Multi-Site Cost/Benefit Analysis

Dane Granicher
Director of Sales & Marketing
dgranicher@bucklingbeam.com

Agenda

- Purpose
- Description of Cost Model
- Discuss Cost Variables
  - Drivers
  - Multi-site inefficiencies
- Summary

Purpose

- Cost modeling for multi-site decision performed by most, but analysis typically simple
- Provide simple but comprehensive model to facilitate decision process
- An hour of analysis can have significant cost impact

Run Your Numbers!

Cost Model

Wafer/Test Data

Wafer Volume

Total Sort Time

Test Cell Cost

Single Site Sort

TD's/Wafer

PC's needed

PH rebuilds

Total Volume Test Cost

Dual Site Sort

TD's/Wafer

TD Efficiency

TT Efficiency

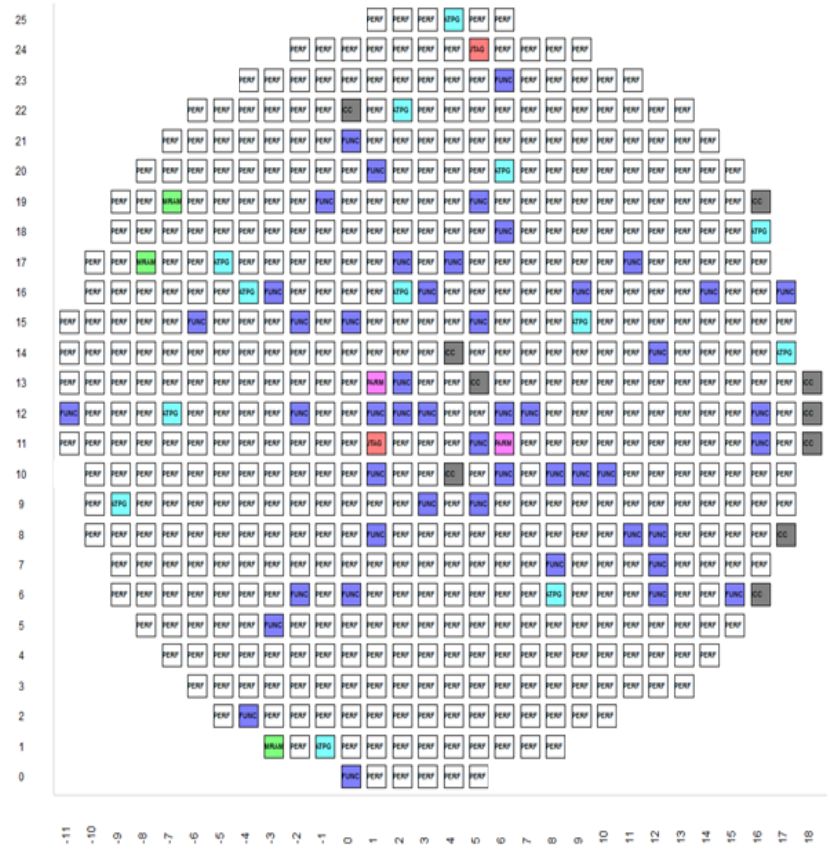
Yield Efficiency

PC's needed

PH rebuilds

Total Volume Test Cost

Base Data for Cost Analysis



- 592 die per wafer
- 3000 contacts/DUT
- Test Time
  - Two Sort Steps, 10s each
- Pure digital test
- Base Test Cell Cost $50/hr
- $30K NRE for Dual Site

Bigger is Better!

Delta Test Cell Cost	Total Program Wafer Volume							
	500	1,000	1,500	2,000	2,500	3,000	3,500	4,000
$ -	$ 51	$ 125	$ 200	$ 274	$ 349	$ 409	$ 484	$ 575
$ 5.00	$ 39	$ 103	$ 166	$ 230	$ 293	$ 342	$ 405	$ 485
$ 10.00	$ 28	$ 80	$ 133	$ 185	$ 237	$ 275	$ 327	$ 396
$ 15.00	$ 17	$ 58	$ 99	$ 140	$ 181	$ 208	$ 249	$ 306
$ 20.00	$ 6	$ 36	$ 66	$ 95	$ 125	$ 140	$ 170	$ 217
$ 25.00	$ (5)	$ 13	$ 32	$ 51	$ 69	$ 73	$ 92	$ 127
$ 30.00	$ (17)	$ (9)	$ (2)	$ 6	$ 13	$ 6	$ 14	$ 38

Thousands

- No Dual-site inefficiencies
- Model dominated by pure reduced wafer test cost
- Probe card price + NRE only a factor at low volume and at higher dual site test cell cost

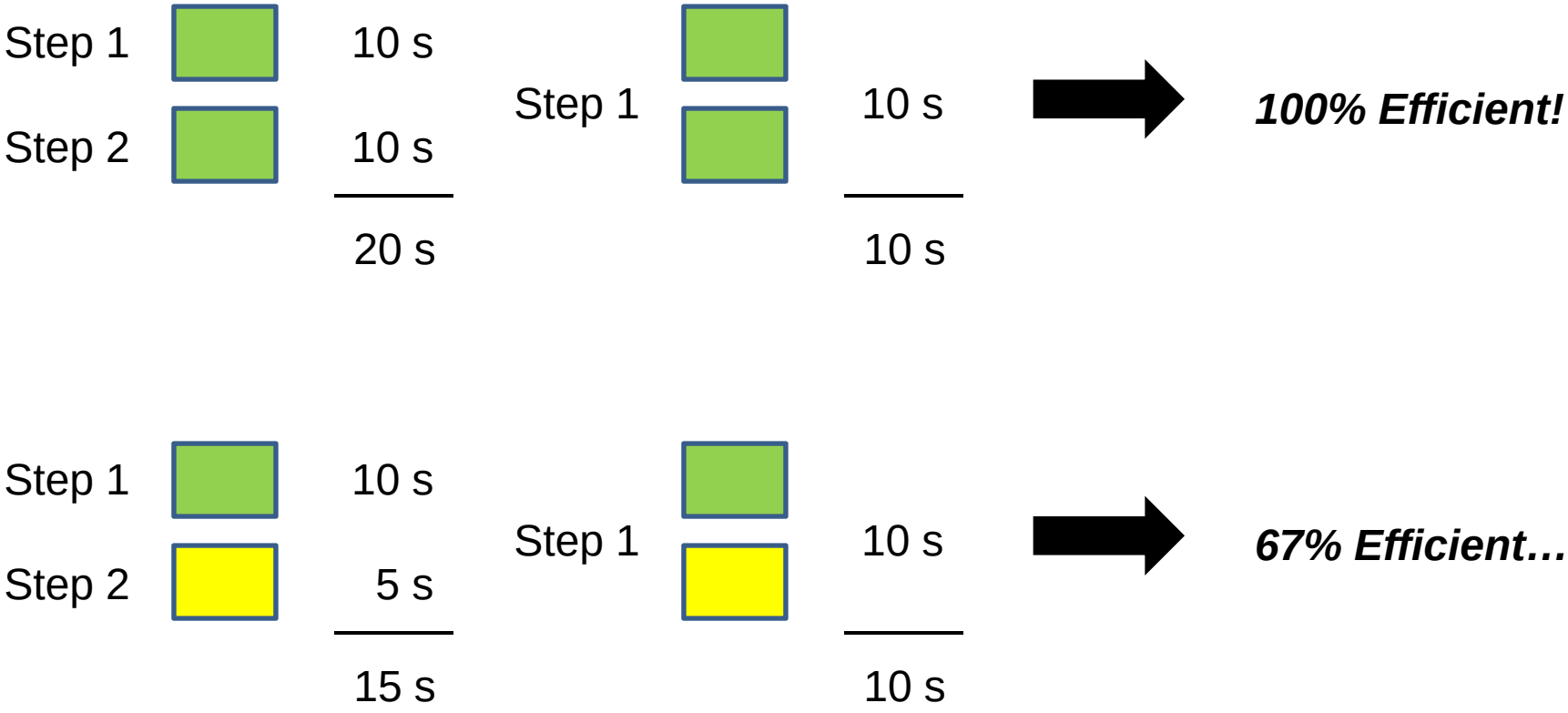
Multi-site Inefficiencies - Tester

Delta Test Cell Cost	Wafer Volume 500	1,000	1,500	2,000	2,500	3,000	3,500	4,000
$ -	$ 51	$ 125	$ 200	$ 274	$ 349	$ 409	$ 484	$ 575
$ 5.00	$ 39	$ 103	$ 166	$ 230	$ 293	$ 342	$ 405	$ 485
$ 10.00	$ 28	$ 80	$ 133	$ 185	$ 237	$ 275	$ 327	$ 396
$ 15.00	$ 17	$ 58	$ 99	$ 140	$ 181	$ 208	$ 249	$ 306
$ 20.00	$ 6	$ 36	$ 66	$ 95	$ 125	$ 140	$ 170	$ 217
$ 25.00	$ (5)	$ 13	$ 32	$ 51	$ 69	$ 73	$ 92	$ 127
$ 30.00	$ (17)	$ (9)	$ (2)	$ 6	$ 13	$ 6	$ 14	$ 38

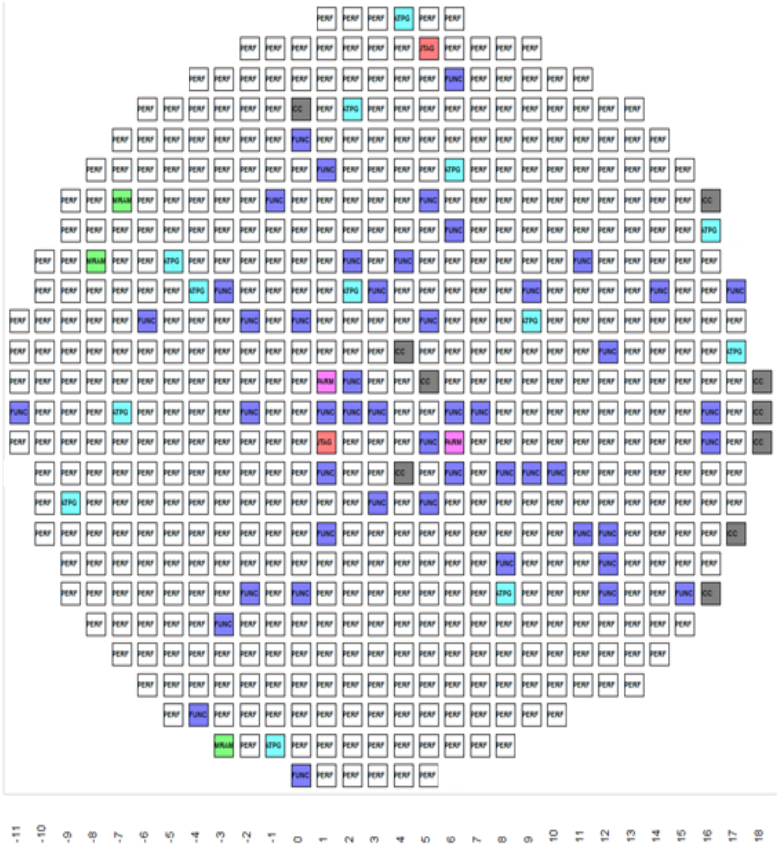
Thousands

- Inefficiency
  - CPU, Data Handling, Analog Resources
  - Test Resources
- Assume 5% dual site efficiency test time hit

Multi-site Inefficiencies - Yield



Multi-site Inefficiencies - Yield



Result	Percent	Total Test Time (s)
Good	86.8%	5140
Fail	13.2%	390
Total Test Time Single Site		**5530**
Good/Good	75.4%	2262
Good/Bad	22.8%	686
Bad/Bad	1.7%	26
Total Test Time Dual Site		**2974**

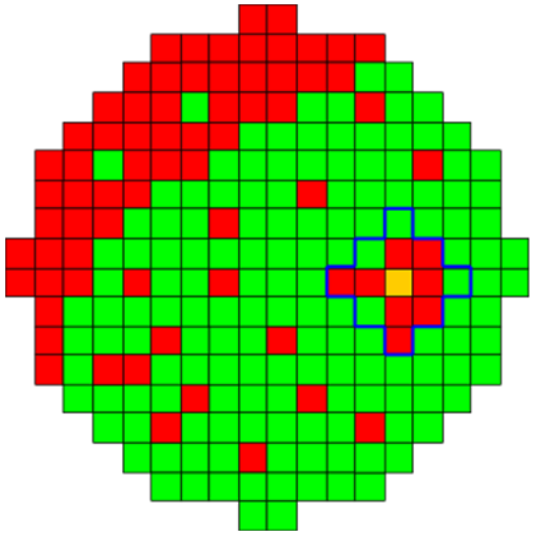
592 dpw

514 Pass – 86.8%

79 Fail

$$\frac{(5530/2)}{2974} = 93.0\%$$

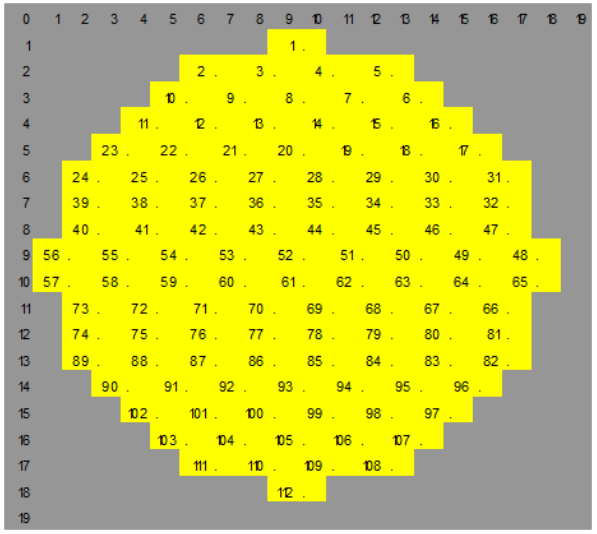
Multi-site Inefficiencies - Yield



Wafer Yield 66.5%

– Model predicts
88.2% Yield Impact

Step Analysis indicates yield inefficiency of 92.3%



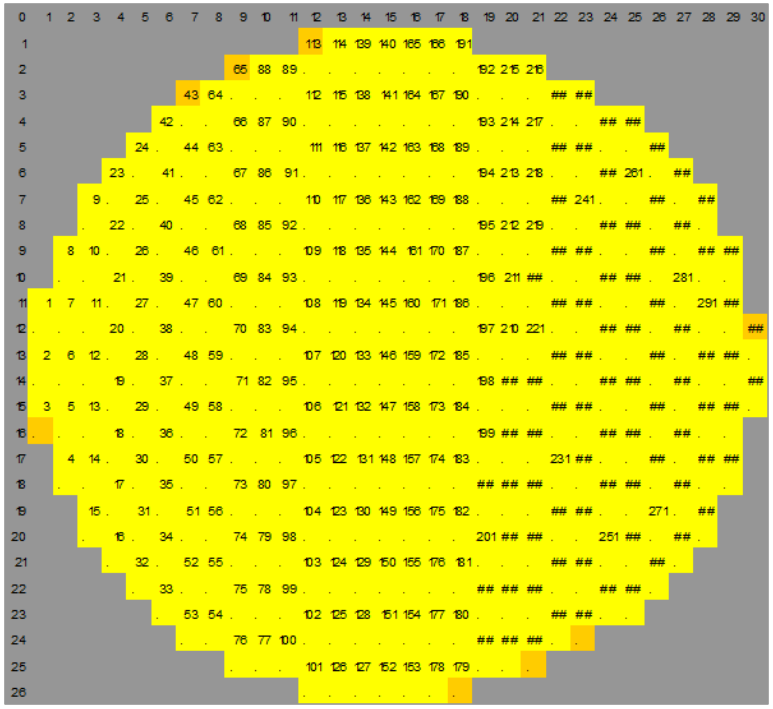
Multi-site Inefficiencies - Yield

		500	1,000	1,500	2,000	2,500	3,000	3,500	4,000
$	-	$ (4)	$ 61	$ 125	$ 190	$ 255	$ 336	$ 401	$ 483
$	5.00	$ (17)	$ 35	$ 87	$ 139	$ 192	$ 260	$ 313	$ 381
$	10.00	$ (30)	$ 10	$ 49	$ 89	$ 128	$ 184	$ 224	$ 280
$	15.00	$ (42)	$ (15)	$ 11	$ 38	$ 65	$ 108	$ 135	$ 179
$	20.00	$ (55)	$ (41)	$ (27)	$ (13)	$ 2	$ 32	$ 47	$ 77
$	25.00	$ (68)	$ (66)	$ (65)	$ (63)	$ (62)	$ (44)	$ (42)	$ (24)
$	30.00	$ (80)	$ (91)	$ (103)	$ (114)	$ (125)	$ (120)	$ (131)	$ (125)

Thousands

- Wafer Yield 86.8% equals inefficiency of 93%

Multi-site Inefficiencies - Stepping



- Multi-site Arrays typically not 100% efficient
  - Theoretical best stepping on 592 wafer would be 296 steps
  - This wafer requires 300 steps – 98.8% efficient

Multi-site Inefficiencies - Stepping

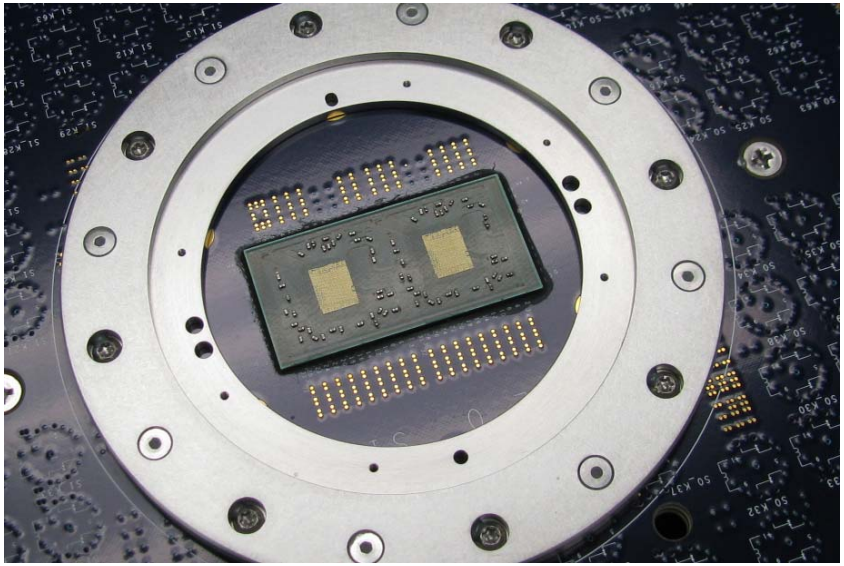
Wafer Volume

	500	1,000	1,500	2,000	2,500	3,000	3,500	4,000
$ -	$ (4)	$ 61	$ 125	$ 190	$ 255	$ 336	$ 401	$ 483
$ 5.00	$ (17)	$ 35	$ 87	$ 139	$ 192	$ 260	$ 313	$ 381
$ 10.00	$ (30)	$ 10	$ 49	$ 89	$ 128	$ 184	$ 224	$ 280
$ 15.00	$ (42)	$ (15)	$ 11	$ 38	$ 65	$ 108	$ 135	$ 179
$ 20.00	$ (55)	$ (41)	$ (27)	$ (13)	$ 2	$ 32	$ 47	$ 77
$ 25.00	$ (68)	$ (66)	$ (65)	$ (63)	$ (62)	$ (44)	$ (42)	$ (24)
$ 30.00	$ (80)	$ (91)	$ (103)	$ (114)	$ (125)	$ (120)	$ (131)	$ (125)

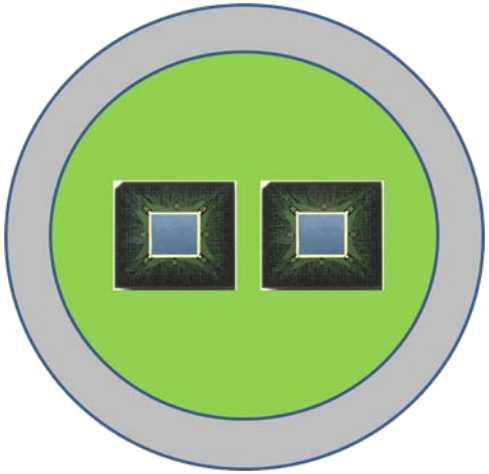
Thousands

- Effect of 98.8% Stepping Efficiency
- NRE buys best Stepping, but can it be reduced?

Strategies to Reduce PC NRE

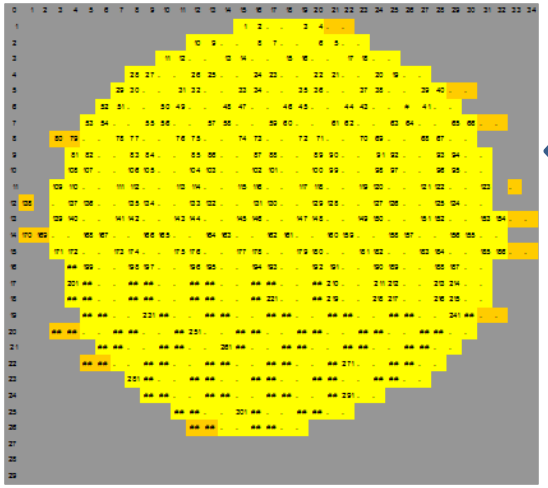


- Dual site MLO based on device package



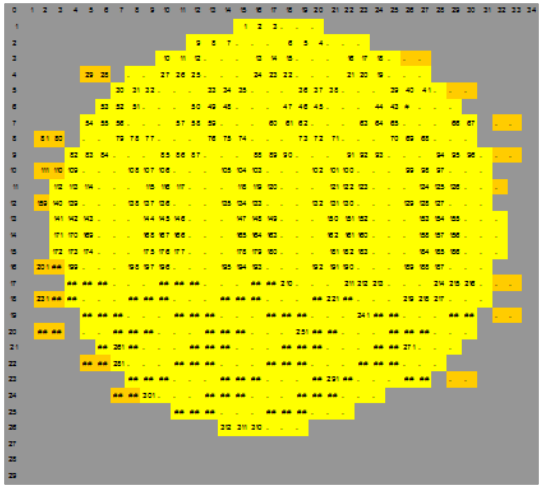
- Two final MLO packages attached to Probe Card PCB

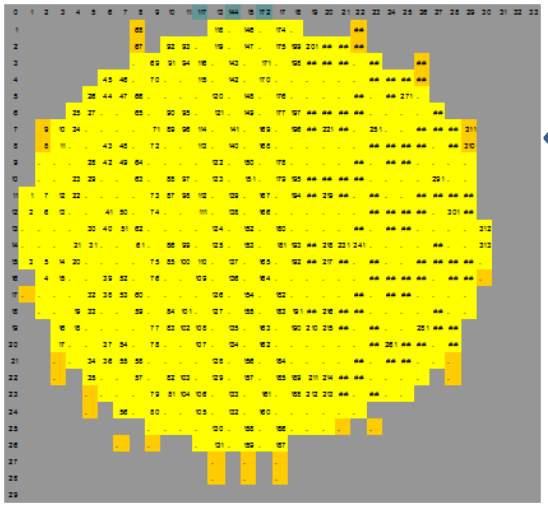
Stepping Efficiency Analysis



2x1 S1C
308 TDs
95.9%

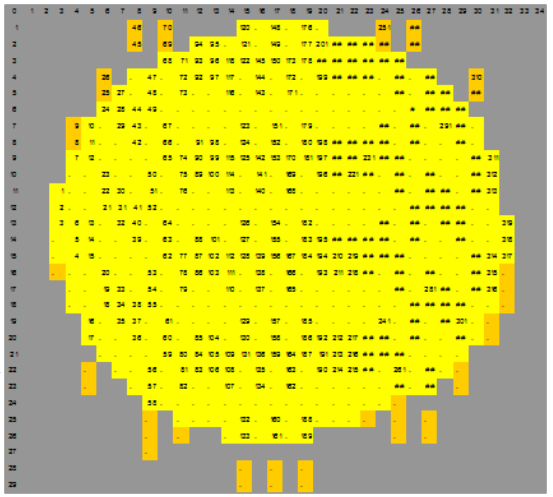
2x1 S2C
312 TDs
94.6%





1x2 S1R
313 TDs
94.3%

1x2 S2R
319 TDs
92.2%



Effect of Skips

Wafer Volume

	500	1000	1500	2000	2500	3000	3500	4000	
$ -	$ (5)	$ 58	$ 122	$ 186	$ 249	$ 330	$ 393	$ 474	
$ 7.50	$ (18)	$ 33	$ 83	$ 134	$ 185	$ 253	$ 303	$ 371	
$ 15.00	$ (31)	$ 7	$ 45	$ 83	$ 121	$ 176	$ 214	$ 268	
$ 22.50	$ (44)	$ (19)	$ 6	$ 31	$ 57	$ 99	$ 124	$ 166	Solid 1x2
$ 30.00	$ (57)	$ (44)	$ (32)	$ (20)	$ (8)	$ 21	$ 34	$ 63	98.8% efficient
$ 37.50	$ (70)	$ (70)	$ (71)	$ (71)	$ (72)	$ (56)	$ (56)	$ (40)	Includes $30K NRE
$ 45.00	$ (82)	$ (96)	$ (109)	$ (123)	$ (136)	$ (133)	$ (146)	$ (143)	

	500	1000	1500	2000	2500	3000	3500	4000	
$ -	$ 18	$ 76	$ 133	$ 190	$ 248	$ 322	$ 379	$ 422	
$ 7.50	$ 5	$ 48	$ 92	$ 135	$ 179	$ 239	$ 283	$ 312	
$ 15.00	$ (9)	$ 21	$ 50	$ 80	$ 110	$ 157	$ 186	$ 201	
$ 22.50	$ (23)	$ (7)	$ 9	$ 25	$ 41	$ 74	$ 90	$ 91	2x1 S2R
$ 30.00	$ (37)	$ (35)	$ (32)	$ (30)	$ (28)	$ (9)	$ (7)	$ (19)	92.2% efficient
$ 37.50	$ (51)	$ (62)	$ (74)	$ (85)	$ (97)	$ (91)	$ (103)	$ (129)	No NRE
$ 45.00	$ (64)	$ (90)	$ (115)	$ (140)	$ (166)	$ (174)	$ (199)	$ (240)	

$ 24	$ 17	$ 11	$ 5	$ (1)	$ (8)	$ (14)	$ (52)
$ 23	$ 16	$ 8	$ 1	$ (6)	$ (13)	$ (21)	$ (59)
$ 22	$ 14	$ 6	$ (3)	$ (11)	$ (19)	$ (27)	$ (67)
$ 21	$ 12	$ 3	$ (6)	$ (16)	$ (25)	$ (34)	$ (74)
$ 20	$ 10	$ (0)	$ (10)	$ (20)	$ (30)	$ (40)	$ (82)
$ 19	$ 8	$ (3)	$ (14)	$ (25)	$ (36)	$ (47)	$ (89)
$ 18	$ 6	$ (6)	$ (18)	$ (30)	$ (42)	$ (53)	$ (97)

Summary

- All inefficiencies have equal impact, so all should be analyzed
- Model can be used for other 'what-if' analysis
  - Is it cost effective to upgrade testers?
  - Is it cost effective to re-buy probe cards?

Run Your Numbers!

Acknowledgments

Joe Foerstel

Manufacturing Engineering – Altera Corporation