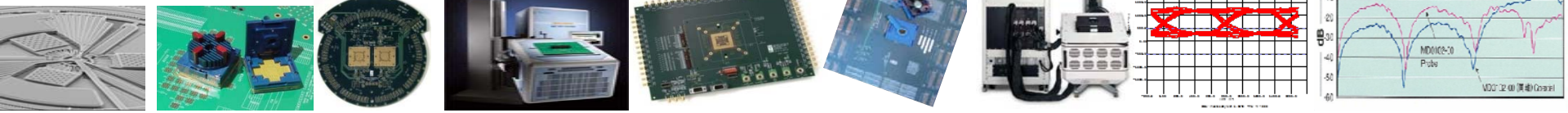

New approach for Post-Silicon Verification on Automated Test Equipment

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Outline

- **Issues in Post-Silicon verification**
  - Conventional Test Development Flow
- **The new approach for Post-Silicon verification**
  - Key points of The New Approach
  - Verilog-Like code on ATE / Interactive Verification / Direct EDA Link
- **Post-Silicon verification with FTA: A Case Study**
- **Conclusion**

Issues in Post-Silicon verification

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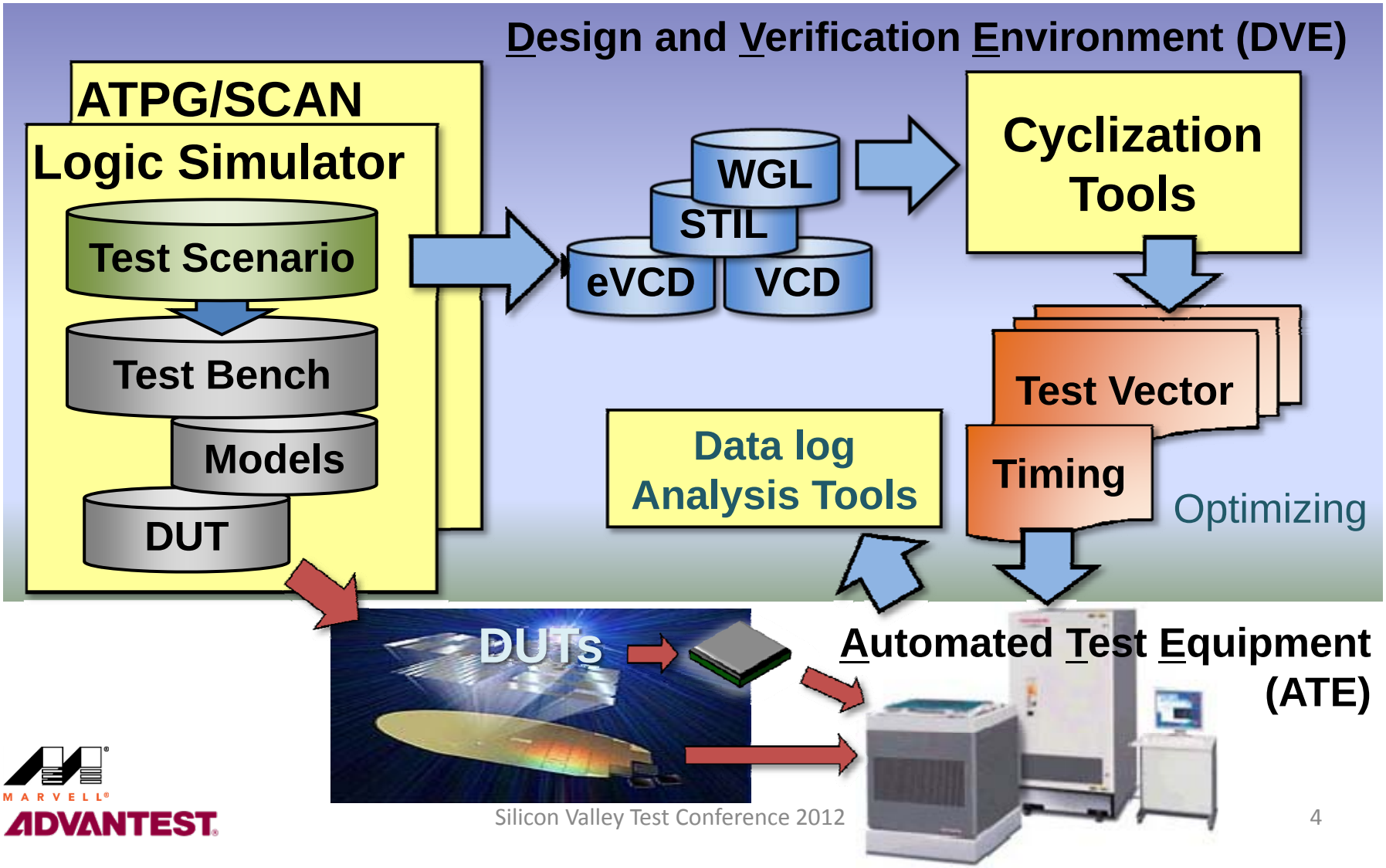
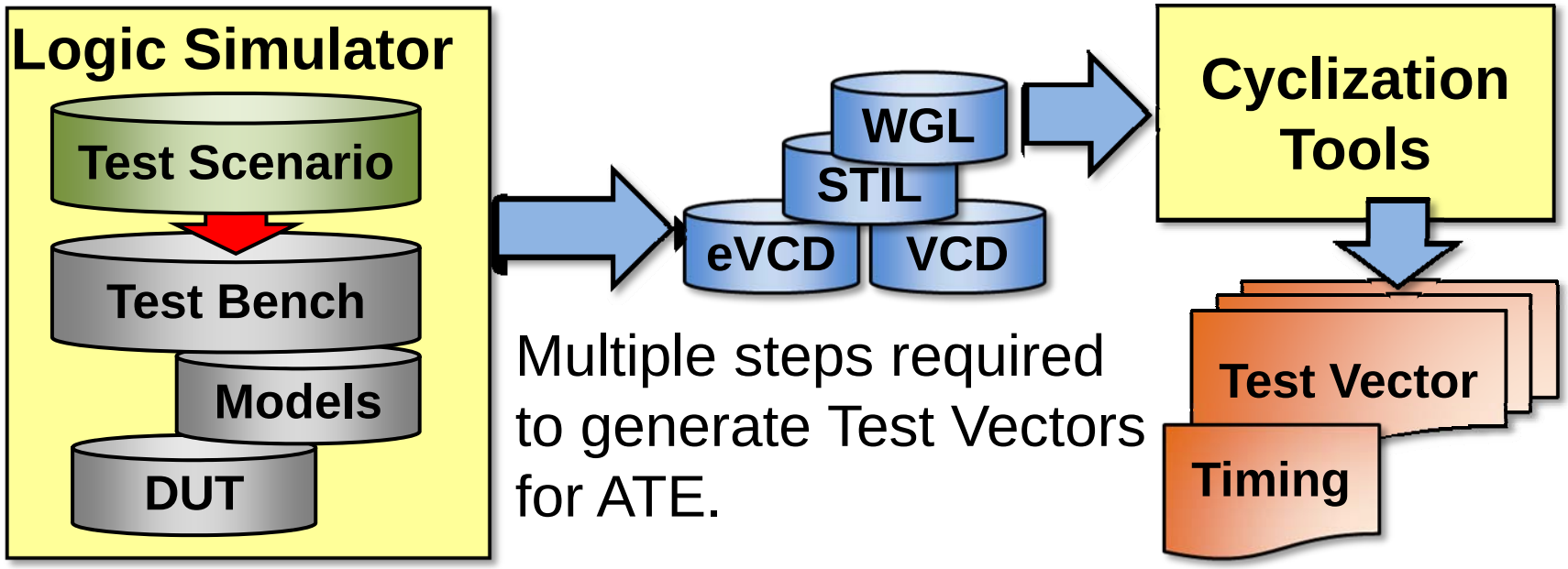
Conventional test flow



Issue1
Complicated ATE Vector Generation

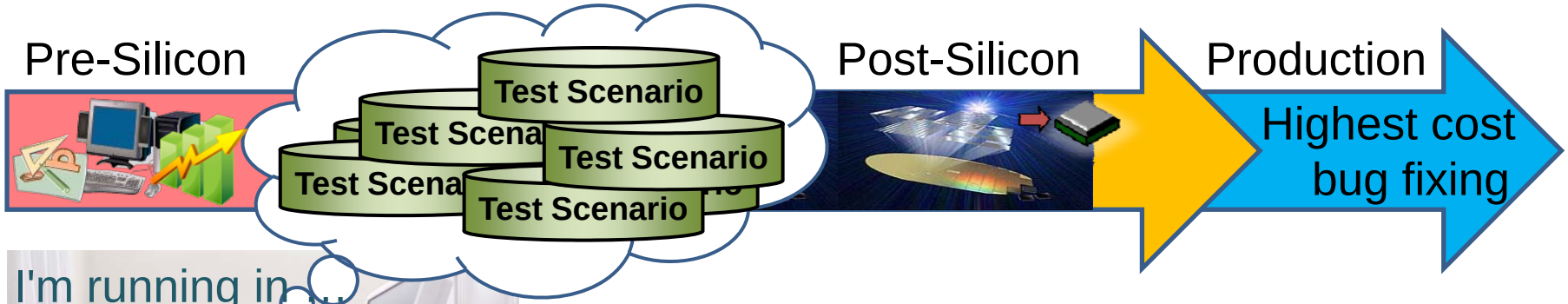


Multiple steps required to generate Test Vectors for ATE.

It takes a long time to generate test vectors despite improvements of environment, including specs.

Issue2

Too many test patterns for production



How many test cases do you have to check out in time?

The market cannot wait for your job completion.

Post-Silicon verification is the last step in the Silicon Development. Get up, get up, and just do it anyway…

Issue3

No observability on ATE

```
01011010XLLLXX
00011010XLLLXX
01011000XLLLXX
00011000XHHLXX
01011000XLHLXX
```

Cyclization Tools

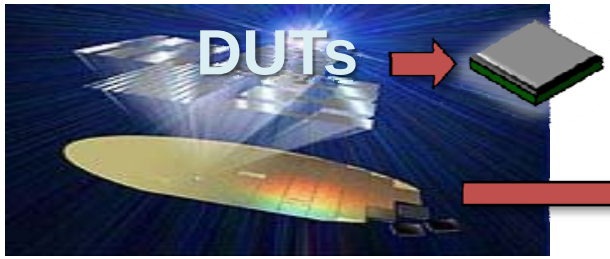
Test Vector

Timing

What's going on?

zero, one, zero, one, one, …

Need to analyze fail data log.



Automated Test Equipment (ATE)

The new approach for Post-Silicon verification

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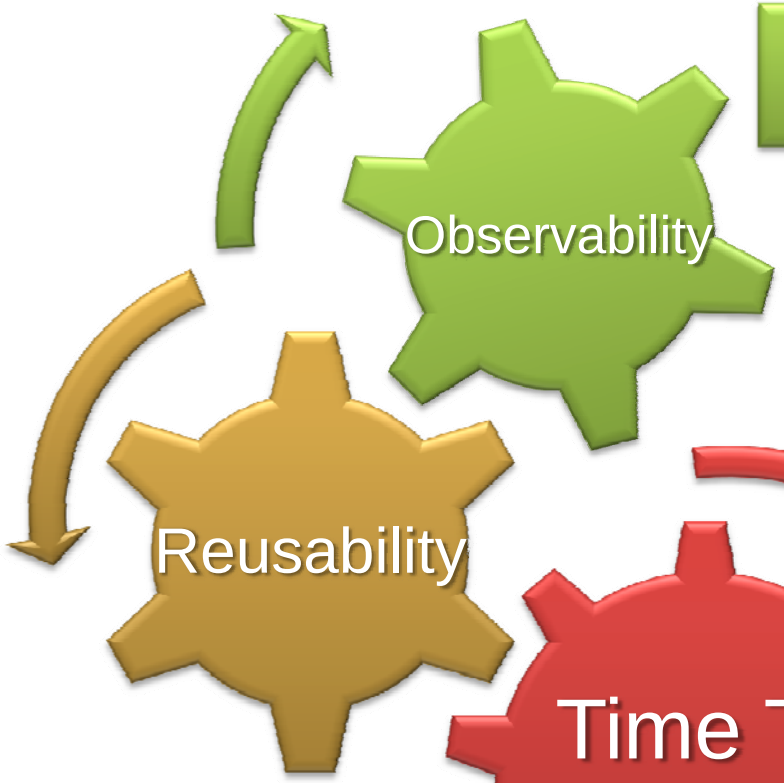
Key points of The New Approach



Test is easily understood by all engineers

Issue3

No observability on ATE

Easy to reuse tests across devices.

Issue2

Too many test patterns for production

Faster program development.

Issue1

Complicated ATE vector generation

Verilog-Like code on ATE

The New Approach is Functional Test Abstraction (FTA).
Test is expressed by transaction level similar to Verilog code.

Conventional Test Pattern

```
NOP 01110001 00000101
NOP 00000000 XXXXXXXX
 :      :       :      :
NOP 01000000 XXXXXXXX
NOP 00000000 XXXXXXXX
NOP 01100001 LLLLLHLH
NOP 00000000 XXXXXXXX
```

FTA Test

Procedure definition

```
Write(4'h1, 8'h05);
Wait(10);
Read(4'h1, 8'h05);
```

Under-standable!!

Function definition

```
Func Write ( adrs, wdat ) {
  Cmd<=2'b11,
  Adrs<=adrs, Dat<=wdat;
};
  :     :
```

Direct EDA Link

Silicon Valley Test Workshop

Design and Verification Environment (DVE)

Logic Simulator

- Test Scenario
- Test Bench
- FTA-Model
- DUT

FTA-Model is Verilog based model which represents FTA hardware on your DVE.

Directly converted from Verilog code

- FTA Test
- Timing

FTA-Elink provides minimum transfer time to ATE.

One step preparation

Automated Test Equipment (ATE)

MARVELL ADVANTEST

Before/After Conversion

Original Test Bench

(Verilog code)

```
module xbist ();
  initial begin
    test_start;
    jtag_loadir ( XBIST_CTL, 9'h001 );
    jtag_loaddr ( 36'h1, 36'h0, 36 );
    (snip)
    //Wait for XBIST done
    xbist_status_read;
    test_end;
  end
endmodule
```

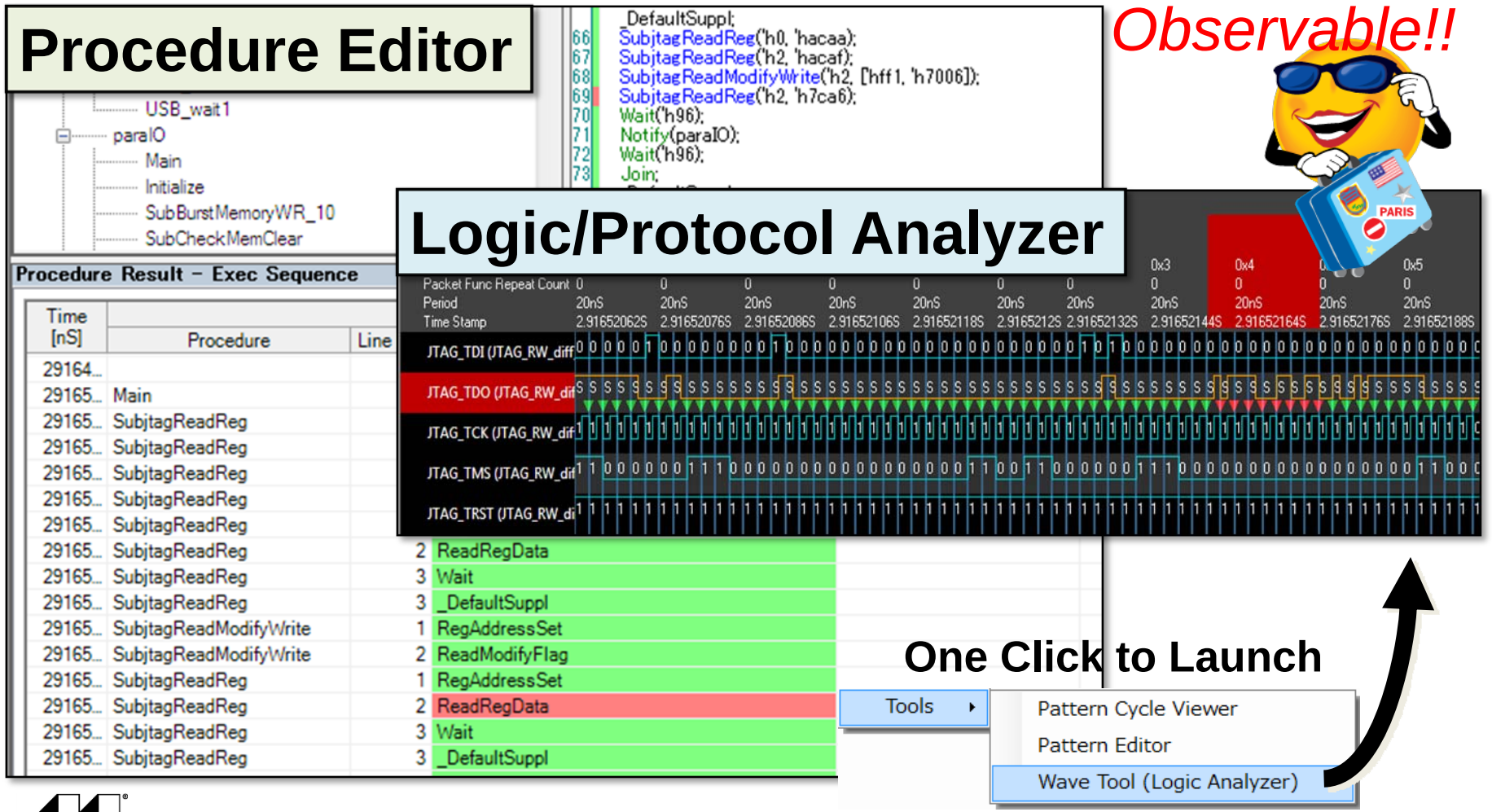
Conversion Tool by FTA E-Link

FTA Test

(Verilog-Like code)

```
xbist.proc
  Main {
    test_start;
    jtag_loadir ( $XBIST_CTL, 9'h001 );
    jtag_loaddr ( 36'h1, 36'h0, 36 );
    (snip)
    #Wait for XBIST done
    xbist_status_read;
    test_end;
  }
```

Interactive Verification on ATE



Interactive Verification on ATE

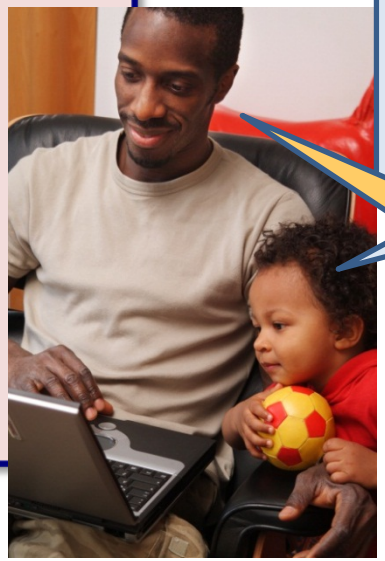
Silicon Valley Test Workshop

You can verify your test easily using device info.

```
xbist.proc
  Main {
    test_start;
    jtag_loadir ( $XBIST_CTL, 9'h001 );
    jtag_loaddr ( 36'h1, 36'h0, 36 );
    (snip)
    #Wait for XBIST done
    Wait(100);
    xbist_status_read;
    test_end;
  }
```

FAIL

Oh… FAIL in xbist_status….
Less of VDD margin!?



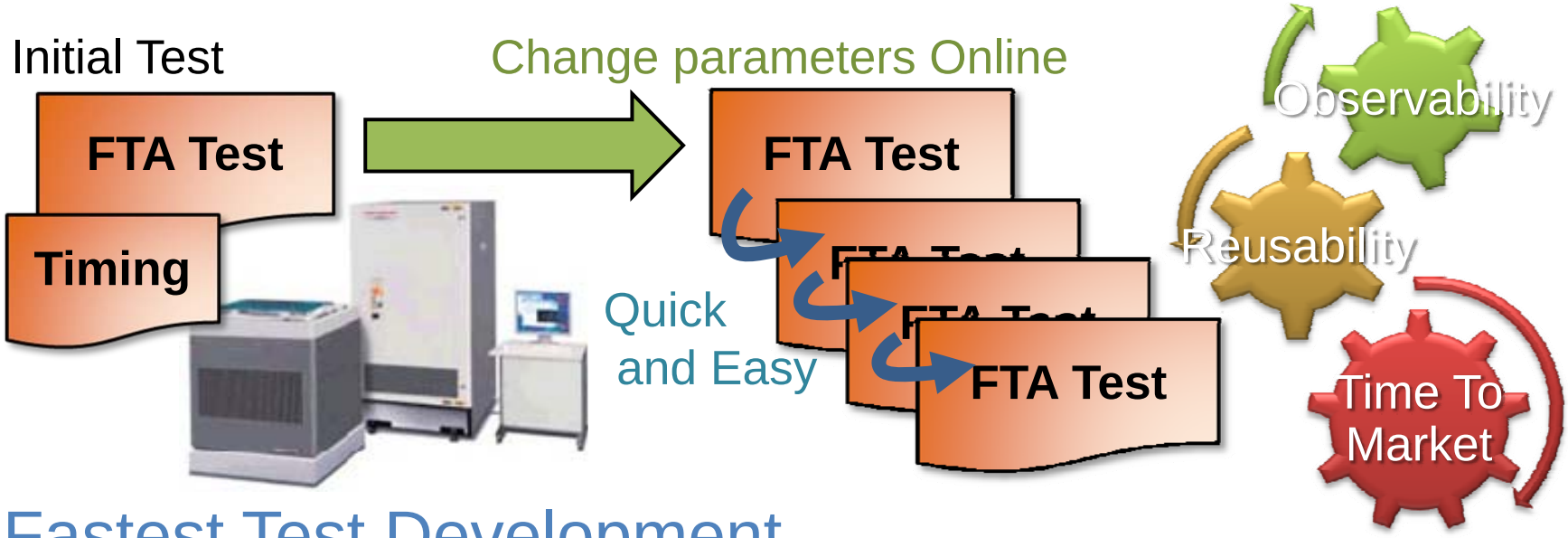
No!!
Add wait time before xbist_status_read.
It's under the limit.

OK. Let me check!!

MARVELL ADVANTEST

No Simulation for Production

Less gap between Pre-/Post-Silicon Environment.
Use Silicon on ATE for Verification.

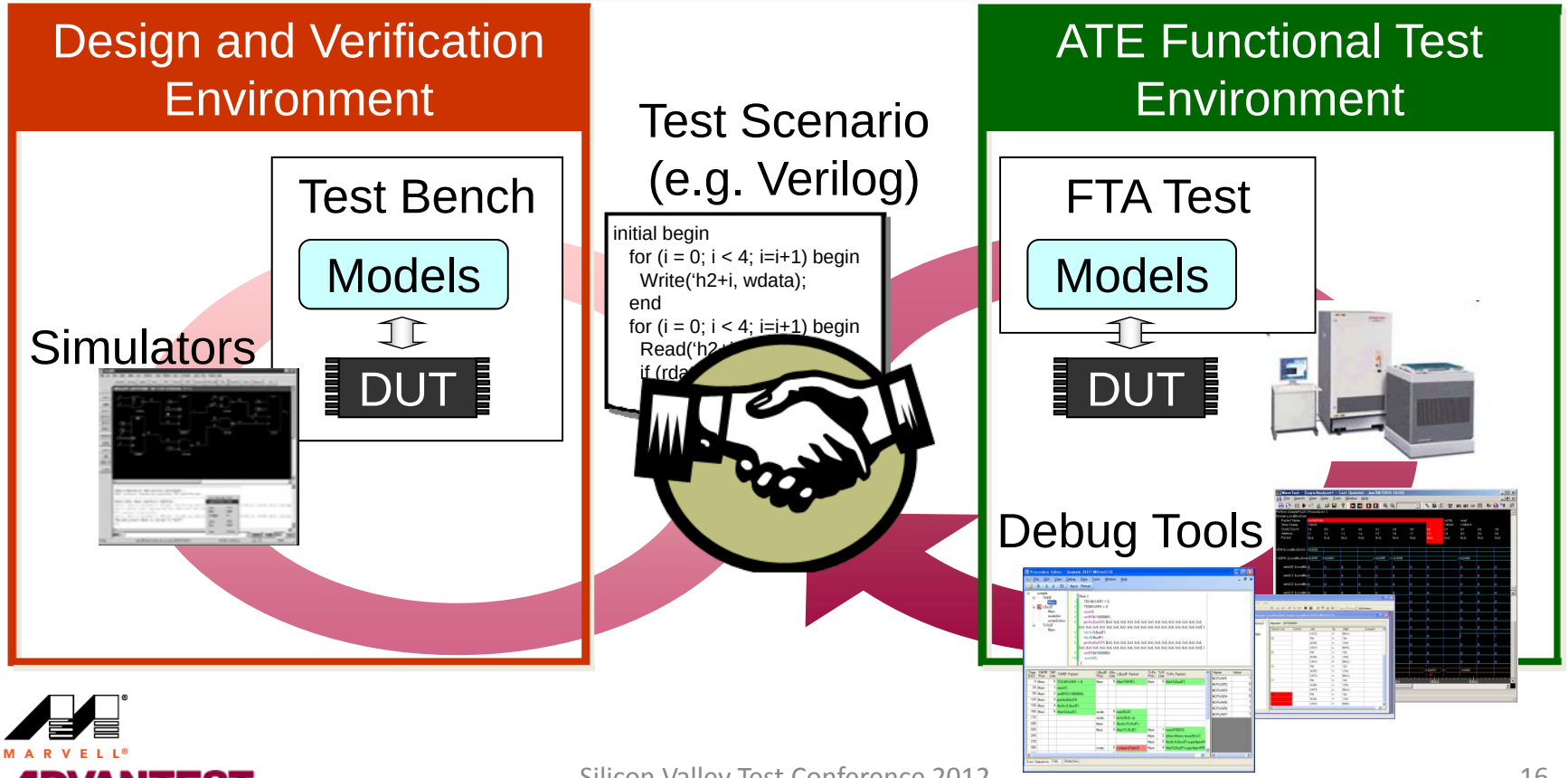


Fastest Test Development

Overall The New Approach

Silicon Valley Test Workshop

Integration of design and verification environment and ATE functional test environment



Post-Silicon verification with FTA: A Case Study

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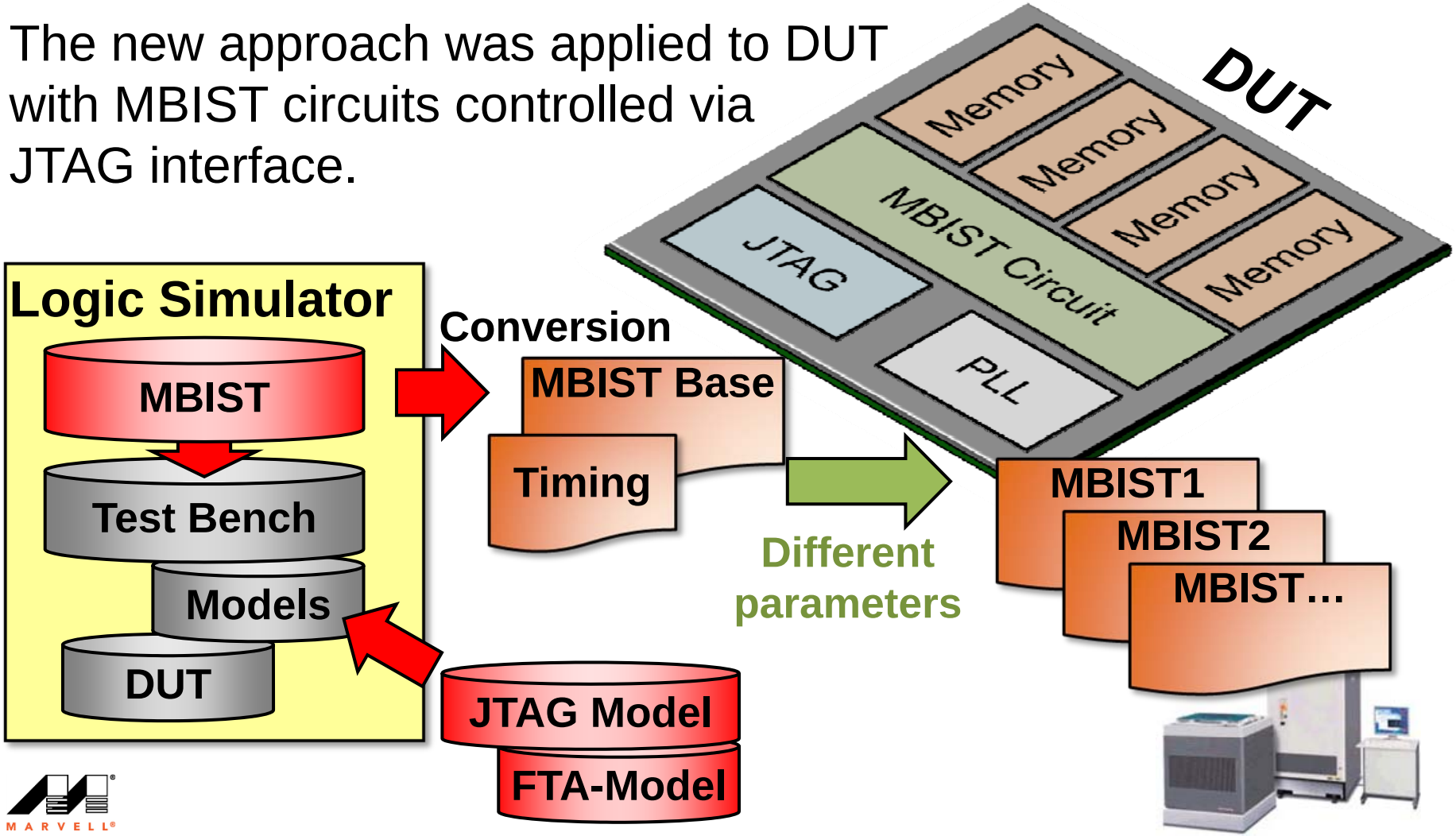
Case Study of FTA

The new approach was applied to DUT with MBIST circuits controlled via JTAG interface.



Comparison Result

Item	Conventional Test Pattern Preparation Time	FTA Test Preparation Time
Test Generation for MBIST Base	4 hours	less than 1 Sec
Test Generation for MBIST1,2,3,..	Over 24 hours	less than 15 minutes (Series of patterns generated online ATE)
Debug Time on ATE	6 hours	1 hours
Overall MBIST Test Preparation Time	**1 Week**	**2 hours**

No difference in Test Execution Time.

Conclusion

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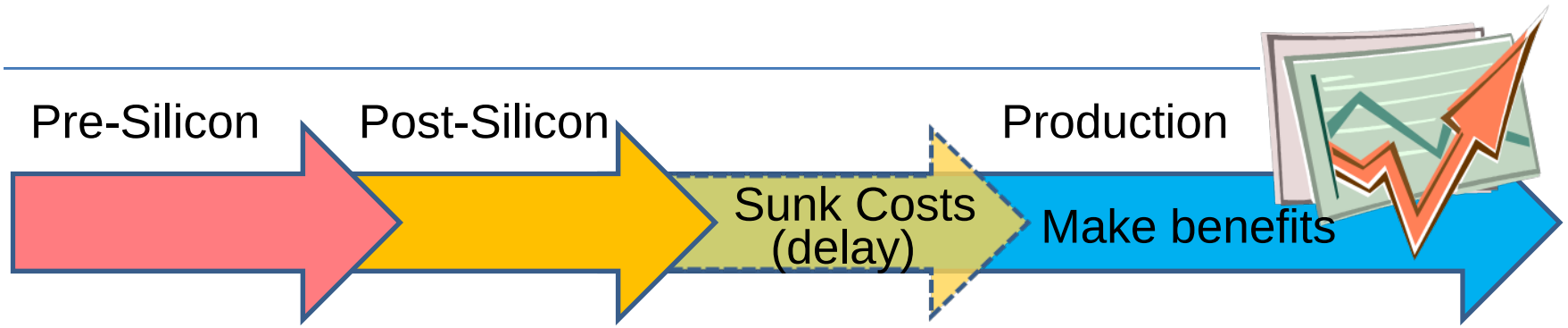
Conclusion



Fast Production Start is the way to make more money in its life time .

Paradigm-shift on ATE !!

ATE is now not only Production Equipment but also **Pre-/Post-Silicon Bridge Tool.**

Memo