New approach for Post-Silicon Verification on Automated Test Equipment

Atsuo Sawara
ADVANTEST Corp., atsuo.sawara@jp.advantest.com

Sujith Karunanayake
Marvell Semiconductor Inc., skarunan@marvell.com

A.T. Sivaram
Advantest America Inc., a.sivaram@advantest.com
Outline

- Issues in Post-Silicon verification
  - Conventional Test Development Flow
- The new approach for Post-Silicon verification
  - Key points of The New Approach
  - Verilog-Like code on ATE / Interactive Verification / Direct EDA Link
- Post-Silicon verification with FTA: A Case Study
- Conclusion
Issues in Post-Silicon verification

- Conventional Test Development Flow
- The new approach for Post-Silicon verification
  - Key points of The New Approach
  - Verilog-Like code on ATE / Interactive Verification / Direct EDA Link
- Post-Silicon verification with FTA: A Case Study
- Conclusion
Conventional test flow

- ATPG/SCAN
- Logic Simulator
- Test Scenario
- Test Bench
- Models
- DUT

Design and Verification Environment (DVE)
- Cyclization Tools
- Data log Analysis Tools
- Test Vector
- Timing
- Optimizing

Automated Test Equipment (ATE)

DUTs
Issue 1
Complicated ATE Vector Generation

Multiple steps required to generate Test Vectors for ATE.

It takes a long time to generate test vectors despite improvements of environment, including specs.
Issue 2
Too many test patterns for production

Pre-Silicon

Post-Silicon

Production

Pre-Silicon Test Scenario Test Scenario Test Scenario Test Scenario

Post-Silicon Test Scenario Test Scenario Test Scenario

Production

How many test cases do you have to check out in time?
The market cannot wait for your job completion.

Post-Silicon verification is the last step in the Silicon Development. Get up, get up, and just do it anyway…
Issue 3

No observability on ATE

What's going on?
zero, one, zero, one, one, …

Need to analyze fail data log.
The new approach for Post-Silicon verification

Issues in Post-Silicon verification
- Conventional Test Development Flow

The new approach for Post-Silicon verification
- Key points of The New Approach
- Verilog-Like code on ATE / Interactive Verification / Direct EDA Link

Post-Silicon verification with FTA: A Case Study
Conclusion
Key points of The New Approach

Issue1: Complicated ATE vector generation

Issue2: Easy to reuse tests across devices.

Issue3: Test is easily understood by all engineers

No observability on ATE

Too many test patterns for production

Faster program development.

Observability

Reusability

Time To Market
Verilog-Like code on ATE

The New Approach is Functional Test Abstraction (FTA). Test is expressed by transaction level similar to Verilog code.

**Conventional Test Pattern**

| NOP     | 01110000100000101 |
| NOP     | 000000000XXXXXXXXX |
| :      | :                  |
| NOP     | 010000000XXXXXXXXX |
| NOP     | 000000000XXXXXXXXX |
| NOP     | 01100001LLLLLHHLH  |
| NOP     | 000000000XXXXXXXXX |

**FTA Test**

**Procedure definition**

Write(4'h1, 8'h05);
Wait(10);
Read(4'h1, 8'h05);

**Function definition**

Func Write ( adrs, wdat ) {
  Cmd<=2'b11,
  Adrs<=adrs, Dat<=wdat;
};
Direct EDA Link

Design and Verification Environment (DVE)

**FTA-Model** is Verilog based model which represents FTA hardware on your DVE.

Directly converted from Verilog code

FTA-Elink provides minimum transfer time to ATE.

One step preparation

Automated Test Equipment (ATE)
Before/After Conversion

Original Test Bench

module xbist ();
    initial begin
        test_start;
        jtag_loadir ( XBIST_CTL, 9'h001 );
        jtag_loaddr ( 36'h1, 36'h0, 36 );
        //Wait for XBIST done
        xbist_status_read;
        test_end;
    end
endmodule

FTA Test

xbist.proc
    Main {
        test_start;
        jtag_loadir ( $XBIST_CTL, 9'h001 );
        jtag_loaddr ( 36'h1, 36'h0, 36 );
        //Wait for XBIST done
        xbist_status_read;
        test_end;
    }
Interactive Verification on ATE

Procedure Editor

Logic/Protocol Analyzer

Observable!!

One Click to Launch
Interactive Verification on ATE

You can verify your test easily using device info.

```vbnet
xbist.proc
Main {
    test_start;
    jtag_loadir ( $XBIST_CTL, 9\'h001 );
    jtag_loadadr ( 36\'h1, 36\'h0, 36 );
    (snip)
    #Wait for XBIST done
    Wait(100);
    xbist_status_read;  \rightarrow  FAIL
    test_end;
}
```

Oh… FAIL in xbist_status…. Less of VDD margin!?

No!! Add wait time before xbist_status_read. It's under the limit.

OK. Let me check!!
No Simulation for Production

Less gap between Pre-/Post-Silicon Environment. Use Silicon on ATE for Verification.

Initial Test

FTA Test

Timing

Change parameters Online

Reusability

Observability

Quick and Easy

Fastest Test Development

Pre-Silicon

Conventional Way

Post-Silicon

The New Approach

Production

Start earlier than before

Silicon Valley Test Conference 2012
Overall The New Approach

Integration of design and verification environment and ATE functional test environment

Design and Verification Environment

Test Bench Models

Simulators

DUT

Test Scenario (e.g. Verilog)

initial begin
for (i = 0; i < 4; i=i+1) begin
Write('h2+i, wdata);
end
for (i = 0; i < 4; i=i+1) begin
Read('h2+i, rdata);
if (rdata == wdata) begin
end

ATE Functional Test Environment

FTA Test Models

DUT

Debug Tools

Silicon Valley Test Conference 2012
Post-Silicon verification with FTA: A Case Study

Issues in Post-Silicon verification
- Conventional Test Development Flow
- The new approach for Post-Silicon verification
- Key points of The New Approach
- Verilog-Like code on ATE / Interactive Verification / Direct EDA Link

Post-Silicon verification with FTA: A Case Study

Conclusion
Case Study of FTA

The new approach was applied to DUT with MBIST circuits controlled via JTAG interface.
## Comparison Result

<table>
<thead>
<tr>
<th>Item</th>
<th>Conventional Test Pattern Preparation Time</th>
<th>FTA Test Preparation Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test Generation for MBIST Base</td>
<td>4 hours</td>
<td>less than 1 Sec</td>
</tr>
<tr>
<td>Test Generation for MBIST1,2,3,..</td>
<td>Over 24 hours</td>
<td>less than 15 minutes (Series of patterns generated online ATE)</td>
</tr>
<tr>
<td>Debug Time on ATE</td>
<td>6 hours</td>
<td>1 hours</td>
</tr>
<tr>
<td>Overall MBIST Test Preparation Time</td>
<td>1 Week</td>
<td>2 hours</td>
</tr>
</tbody>
</table>

No difference in Test Execution Time.
Conclusion

Issues in Post-Silicon verification
- Conventional Test Development Flow

The new approach for Post-Silicon verification
- Key points of The New Approach
- Verilog-Like code on ATE / Interactive Verification / Direct EDA Link

Post-Silicon verification with FTA: A Case Study

Conclusion
Conclusion

Fast Production Start is the way to make more money in its life time.

Paradigm-shift on ATE!!

ATE is now not only Production Equipment but also Pre-/Post-Silicon Bridge Tool.