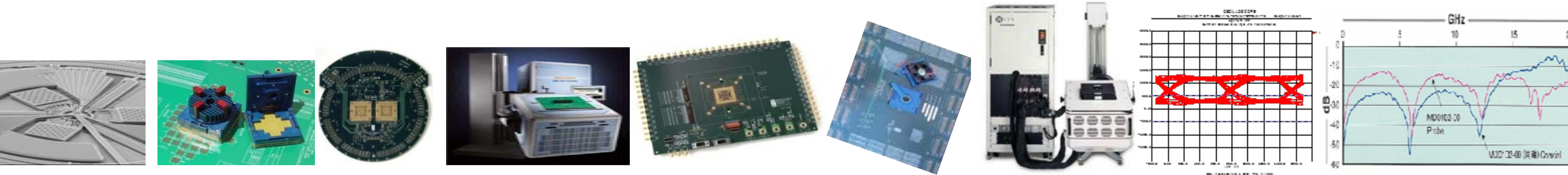

VRT:
The Test Escape You Cannot Escape From!

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Overview

What is VRT(7)
- Define the Behavior
- Literature with timeline
- Root cause

Practical Implications(5)
- Implications for manufacturing
- Implications for systems
- Paradigm change for test?

Conclusion(1)

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What is VRT?

Variable Retention Time (VRT) is the behavior of a storage cell that exhibits more than one data retention value.

It was first noted in a paper presented at the 1987 IEDM conference.

"A Meta-Stable Leakage Phenomenon In DRAM Charge Storage - Variable Hold Time"
(Yaney et al, AT&T Bell Laboratories)

"A new leakage phenomenon called Variable Hold Time(VHT) is reported which can compromise the data retention performance of modern DRAMs. Careful observations of retention(Hold) time on many devices with planar cells and grounded field plates has uncovered a very small portion of the bit population which exhibits multi-valued and metastable leakage current at room temperature. "

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Mysterious VRT

1992 Paper presented at IEDM:

DRAM Variable Retention Time
(Restle et al.;IBM)

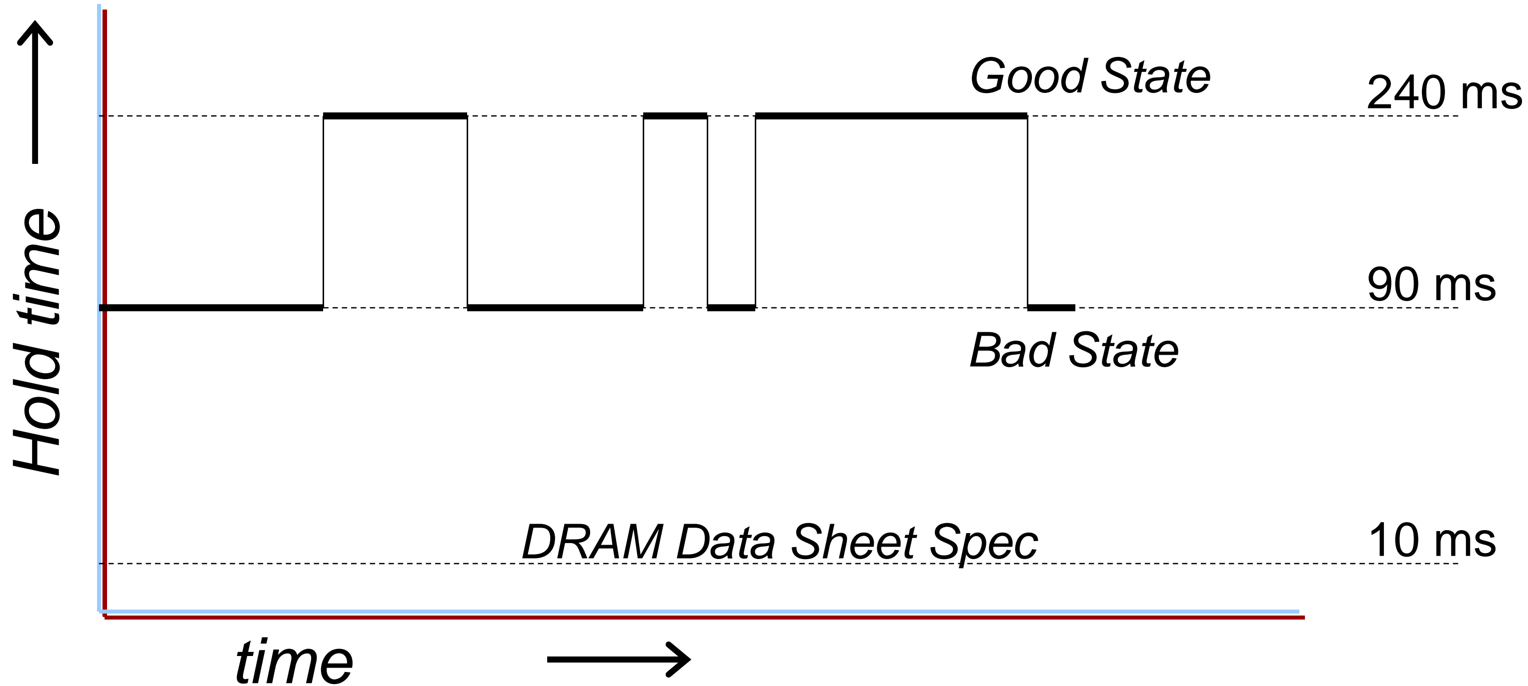
Paper reported on study that looked at DRAMs from multiple manufacturer's with multiple technologies(trench capacitor and stacked capacitor cells).

VRT was found on all chips!!!

Both papers indicate the locations of VRT are associated with observed silicon anomalies but some cells in these areas exhibited VRT and some didn't.

VRT- So What?

After 1992 there were no significant papers presented on the subject until 2004.



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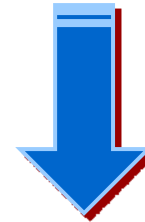
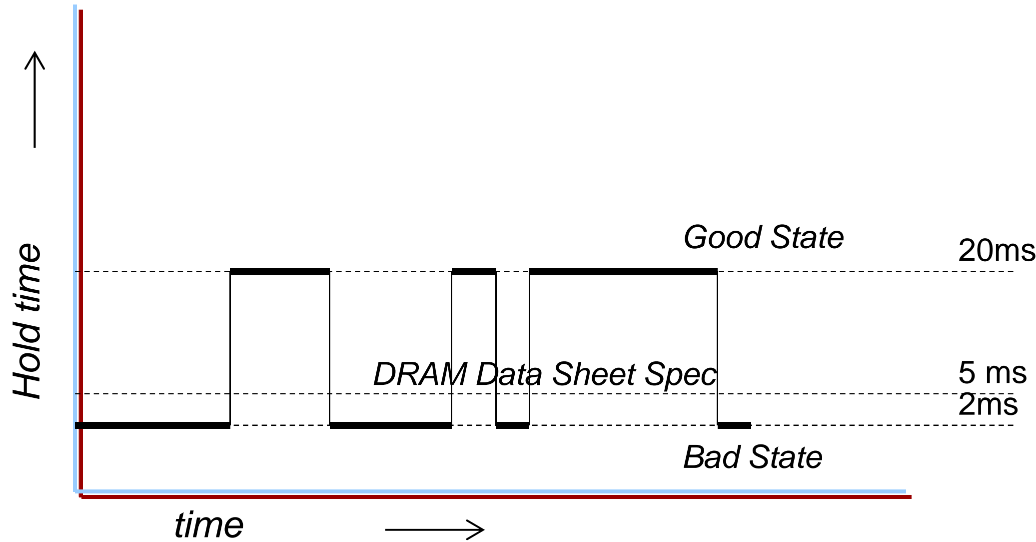
VRT: Catching Up With the Trend

Trends since 1992
-Smaller Geometries
-Smaller Chip Voltages

Smaller Cell Storage Capacitance





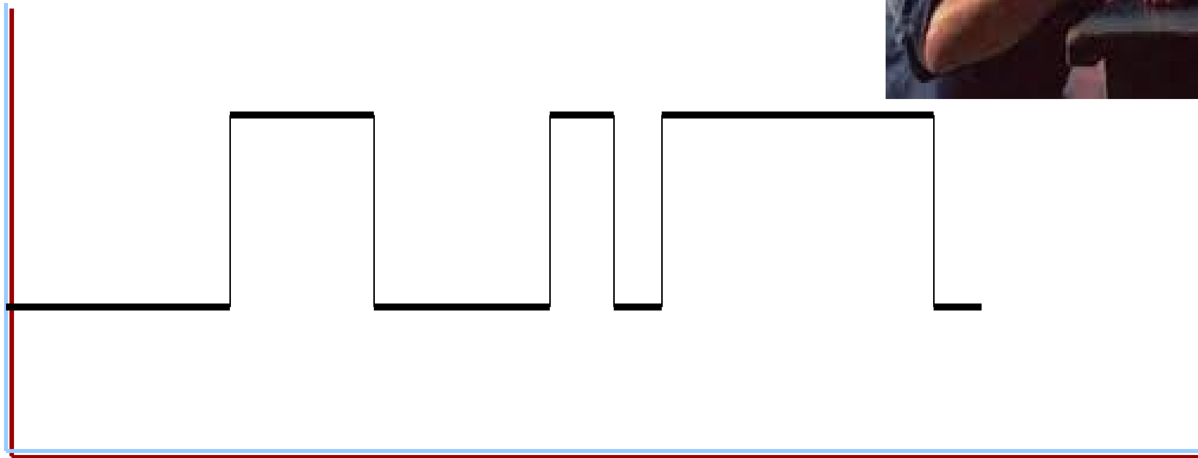
Smaller Hold Times

No Headroom

VRT: Modeling

VRT has now become one of the most important issues in dynamic random access memory (DRAM)

2 Part Model Needed
- Explain Retention State Values
- Explain Transition Times



Transition events occur with a random telegraph signal(RTS)-like fluctuation

VRT: Looking for the Smoking Gun

2005: The Origin of Variable Retention Time in DRAM (Mori et al; Hitachi/Elpida)
Using junction leakage analysis test structure the authors conclusively link VRT to fluctuations in the cell's leakage current(VJL) through its RTS behavior.

Conclusions from test structure measurements

VJL:
- is not a fluctuation of subthreshold leakage or punchthrough
- is a fluctuation of p-n junction leakage which is composed of diffusion current and generation-recombination (G-R) current.

Diffusion current does not fluctuate like a RTS

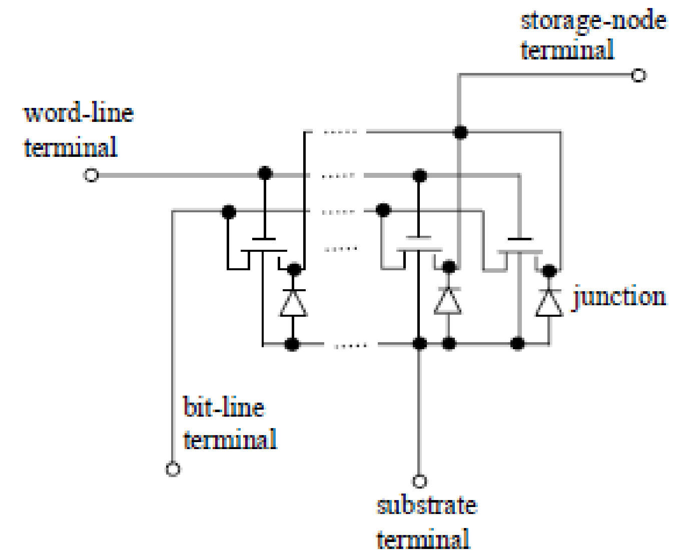


Figure 2. Equivalent circuit of "junction leakage analysis test structure (JAST)".

∴ Fluctuation in G-R current is considered to be an origin of VJL (Variable Junction Leakage).

VRT: Modeling and Mitigation

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2004: Thermal Degradation of DRAM Retention Time: Characterization and Improving Techniques (Kim et al; Samsung)
- Reported on results from experimental fabrication process steps taken to minimize VRT.

2006: Quantitative identification for the physical origin of variable retention time: A vacancy-oxygen complex defect model (Ohyu et al; Elpida/NEC)
-Experimental and theoretical analyses illustrate a vacancy-oxygen complex defect model correlation.

2007: Microscopic aspects of the variations in the retention times of dynamic random access memory (Tuttle/Meade Univ. of Penn/Micron)
-Paper presents a microscopic theory for important aspects of DRAM VRT leakage.

2011: Study of Trap Models Related to the Variable Retention Time Phenomenon in DRAM (Kim et al; Hynix)
- Correlates VRT activation energy to two trap models.

VRT: Why is it a Test Escape?

There are two reasons why VRT represents a test escape.

1. VRT transitions between a Good and Bad Hold time are random.

Random failures can be screened for given a long enough test time

- Increased test time adds cost to a product.
- Even with increased test time random appearance of the behavior means you never know for sure if you have screened the defect.

VRT: Why is it Really Really a Test Escape?

The second reason why VRT represents a test escape.

2. A Good or Bad hold time state can stay stable randomly for seconds or hours.

2006: Single vacancy-oxygen complex defect and variable retention time phenomenon in silicon LSI (Umeda et al; Elpida/NEC)

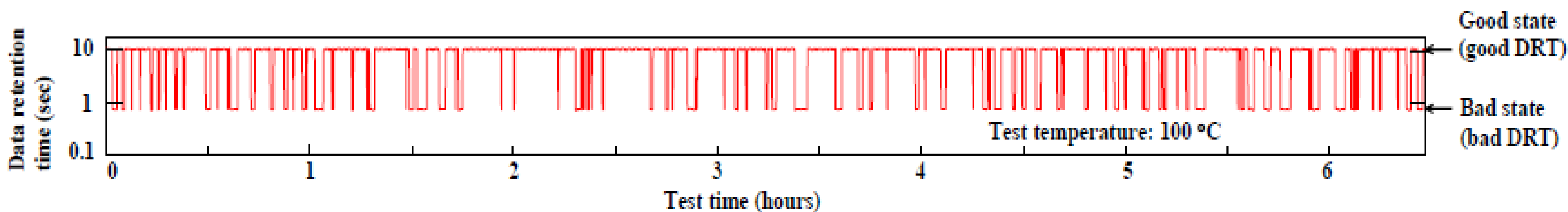

Fig. 1 Two-state variable retention time (VRT) in a DRAM bit.

The cost of testing for this defect is (at the least) cost prohibitive if not impossible!!

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VRT: Abatement Strategies

VRT has been strongly linked to silicon defects.

Research and investigations have moved from recognizing the behavior to understanding the defect that causes VRT.

There are several likely strategies to deal with VRT

- Increase the retention time of the storage cell to add the margins back
- Decrease defects. Keeping in mind there are some process steps that by nature induce defects (i.e. ion implantation and dry etching)
- Make the passivation of the defect more thermally stable

VRT: System Design Considerations

Initial 1987 seminal paper concluded with the following statement

"VHT is random, bad bits may remain hidden during any screening test. These parts can then escape into the "good" population only to later exhibit what very much appears to be a soft error in the system application. We therefore recommend that no application of DRAM be made without error correction in some form."

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Paradigm Change for Test?

How do you deal with a “Test Escape You Cannot Escape From”?

Is it acceptable to ship devices that have suspected but undiscovered defects?

Is there value in a test solution that finds SOME defects?

If you detect a VRT cell and repair it how do you know the repair is free from VRT defects?

Conclusion

VRT is becoming an intractable problem for the industry

- It's behavior makes it elusive to 100% detection.
- It is pervasive in all devices that have storage cells that use a pn junction.
- Ten years ago VRT could be considered an interesting behavior today it has become a costly if not a fatal behavior.
- To date there has been no cure to remove the root cause of VRT only mitigation methods to reduce the occurrence of the behavior.
- There is no viable test strategy to effectively deal with detecting and screening VRT defects.

Abstract

Variable Retention Time(VRT) is a behavior first documented in DRAMs in 1987. Though VRT is better understood today no strategies have come forward to eliminate the flaws in the silicon gate structures which cause the VRT behavior or reliably screen for the behavior in production. This presentation will introduce VRT and review it's repercussions. The presentation will share test considerations that rise from the desire to Escape from the Test Escape.