ADVANTEST

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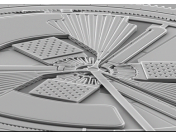
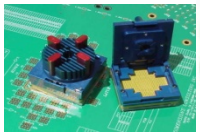
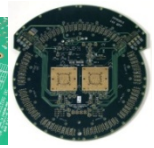


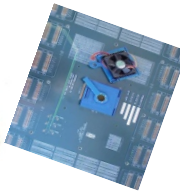

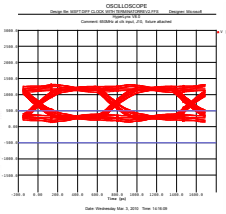
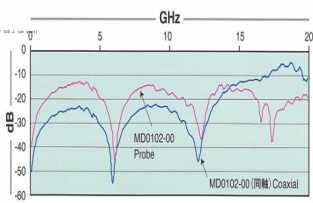

Getting to Known Good Stack

Gary Fleeman
Director, Marketing and Bus Development
Advantest Corporation
g.fleeman@advantest.com

Accumulated Yield

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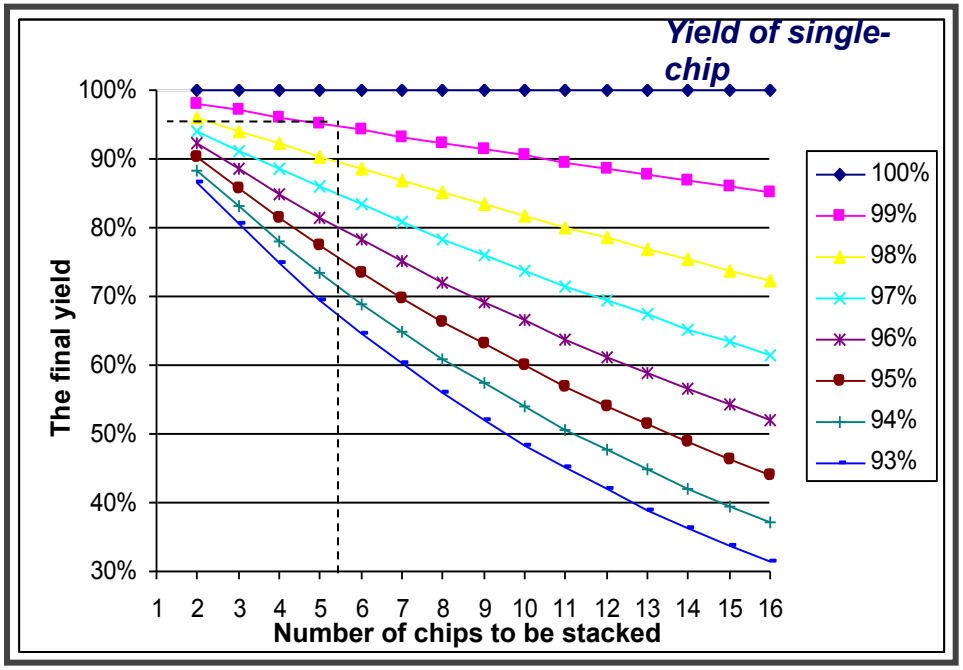
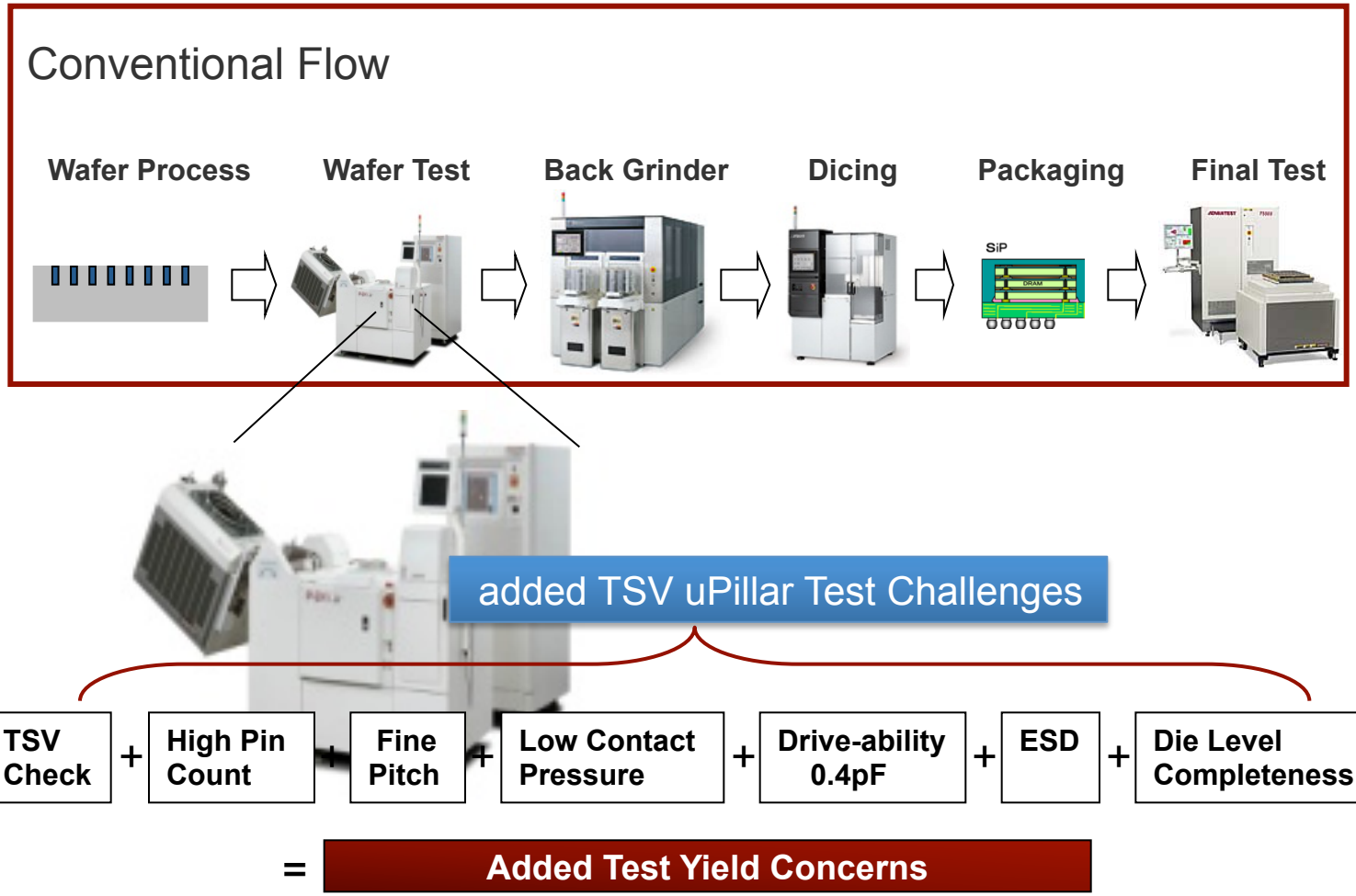
Assume Test Can Provide 99% Die Coverage…..



Even assuming a perfect interposer –

5 die stack could have 4-5% final yield loss

Conventional Challenges



The Via Itself: Interposer

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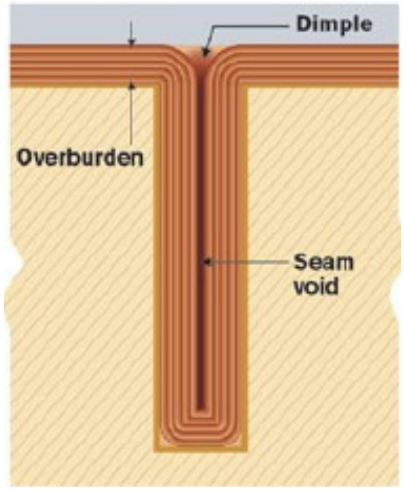
TSV Check + High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness



Source: Optimized TSV Filling Process Reduces Cost, Nexx Systems

Limitation: - Lowest cost device(can't afford to test); no access until after thin.

Countermeasures: - Very good yields; parametric samples, visual & Xray inspections.

Issues: - PPM can have big effect. And … Active interposers are coming.

= **Added Test Yield Concerns**

Access through TSVs or Test Pads?

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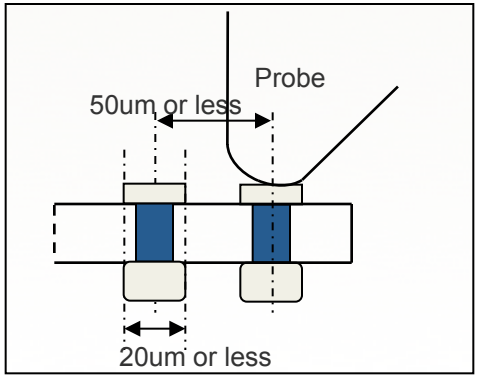
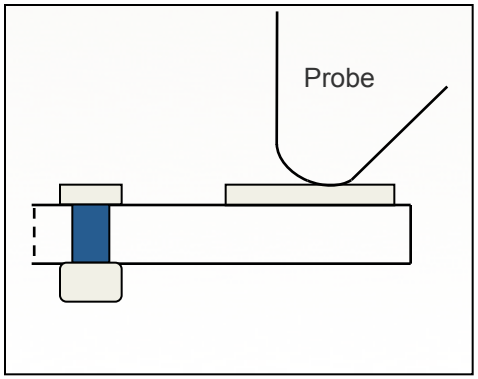
TSV Check + **High Pin Count** + **Fine Pitch** + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness





Limitation: - Probe Cards have architectural limitations for contacting uPillar

Countermeasures: - Use Test Pads and IEEE Standards (1149.7/1149.1/1500/P1687)
- Use Non-Contact Probing

Issues: - Will Test Pads + Structural Test give **enough** coverage?
- Non-Contact Probing requires transmitters/receivers, power delivery still requires physical contact.

Thin Wafers

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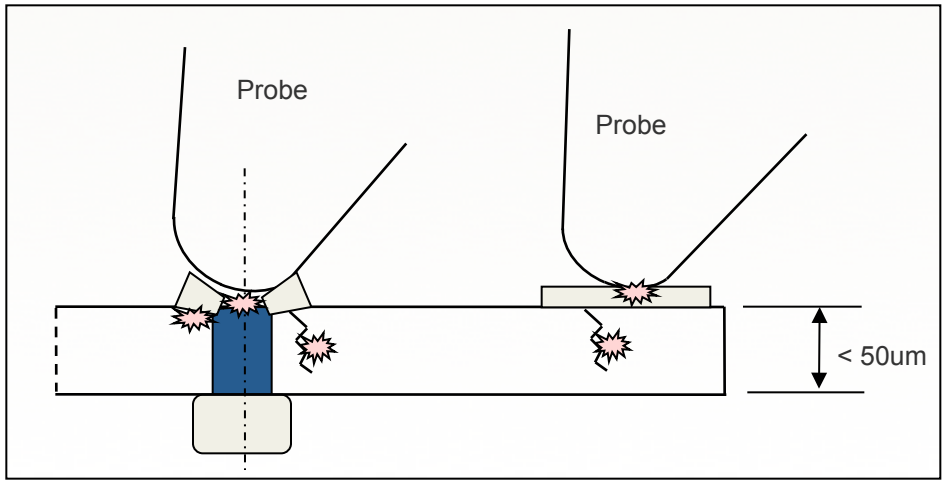
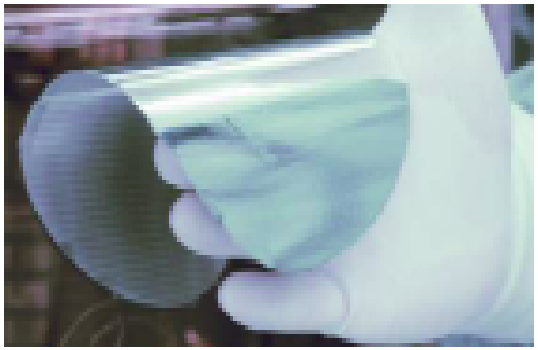
TSV Check + High Pin Count + Fine Pitch + **Low Contact Pressure** + Drive-ability + ESD + Die Level Completeness





Thin Handling and Chip Stacking for 3D Integration
Semicon West 2009, T. Matthia,s EV Group

Limitation:
- Advanced Probe Card lowest contact forces ~ 2g per contact
- Thin Die probably requires <1g

Countermeasures:
- Probe before backside processes (BG, CMP, Etch)
- Use Non-contact probing? Film Frame? Backside Probe on Carrier?

Issues:
- Backside processes **induce defects** that go untested until System.
- Many Questions with Alternatives or substrates

No Driver (TSV I/O)

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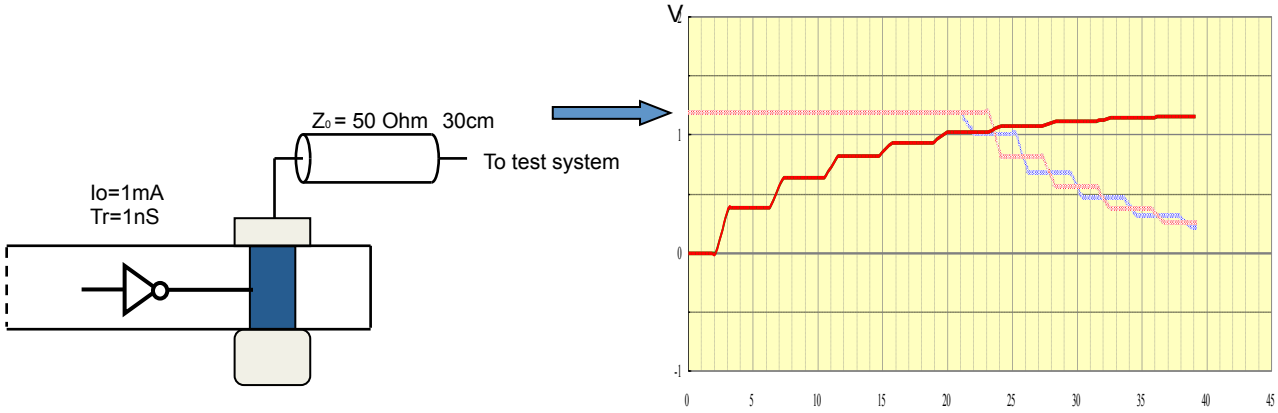
TSV Check + High Pin Count + Fine Pitch + Low Contact Pressure + **Drive-ability** + ESD + Die Level Completeness



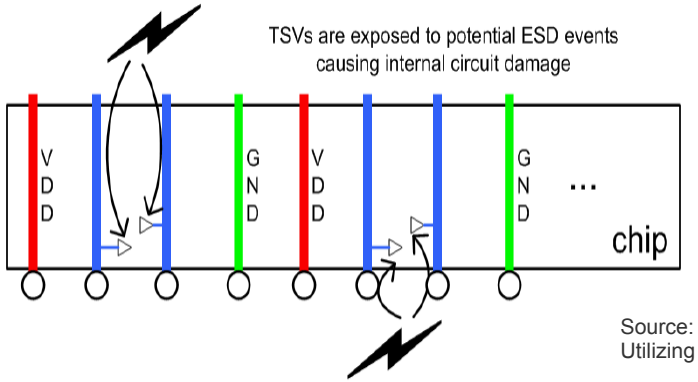
Limitation: - Lack of buffers in device creates drivability problem to ATE.

Countermeasures: - Active probe cards with supplemented buffer amp circuitry.
- Dedicated Test Pads with weak but “ok” drivers

Issues: - Probe cards require high density circuitry, unproven architecture.
- Design and Power requirements for drivers (6mm distance)

ESD

TSV Check + High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + **ESD** + Die Level Completeness



Source: ESD Protection of Through Silicon Via Signals Utilizing Temporary Backside Metallization, IBM

Figure 1 - a chip with TSVs without ESD protection on TSVs

Limitation: - TSVs create paths to internal nodes of IC not previously exposed.
- Circuit loading may be issue with ESD structures.

Countermeasures: - Limit ESD in < machine model
- Weak, small size ESD flip-flop circuits on IC
- Other: Current trigger and Source Pumping,

Issues: - No redundant signal TSVs, very small leakage test

Incomplete Stuff!

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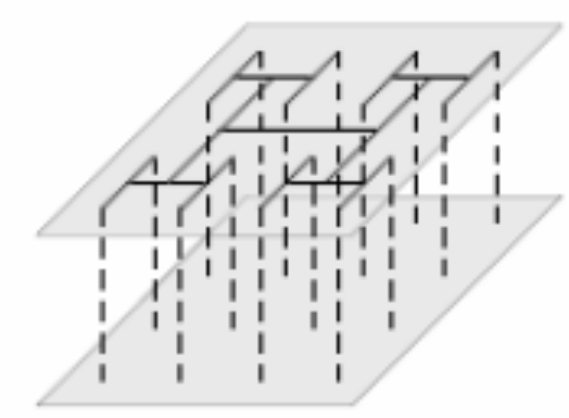
TSV Check + High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness



- 3D clock tree for optimized length and power (example)

- Utilization of different process nodes/different suppliers with truly heterogeneous die.

Source: Test Strategies for 3D Die-Stacked Integrated Circuits
Lewis & Lee, Georgia Institute of Technology

Limitation: - If logic is partitioned on different layers, single die may not be fully testable. If Homogeneous memory – treated as multi-bank die.

Countermeasures: - Design recommendations; GSA and IEEE Standards
- Comment: IDMs can go this route, but will fabless design model support with software & design complexities? EDA/IP issue.

Sample Test/Pkg Flow

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TSV Check + High Pin Count + Fine Pitch + Low Contact Pressure + Drive-ability + ESD + Die Level Completeness

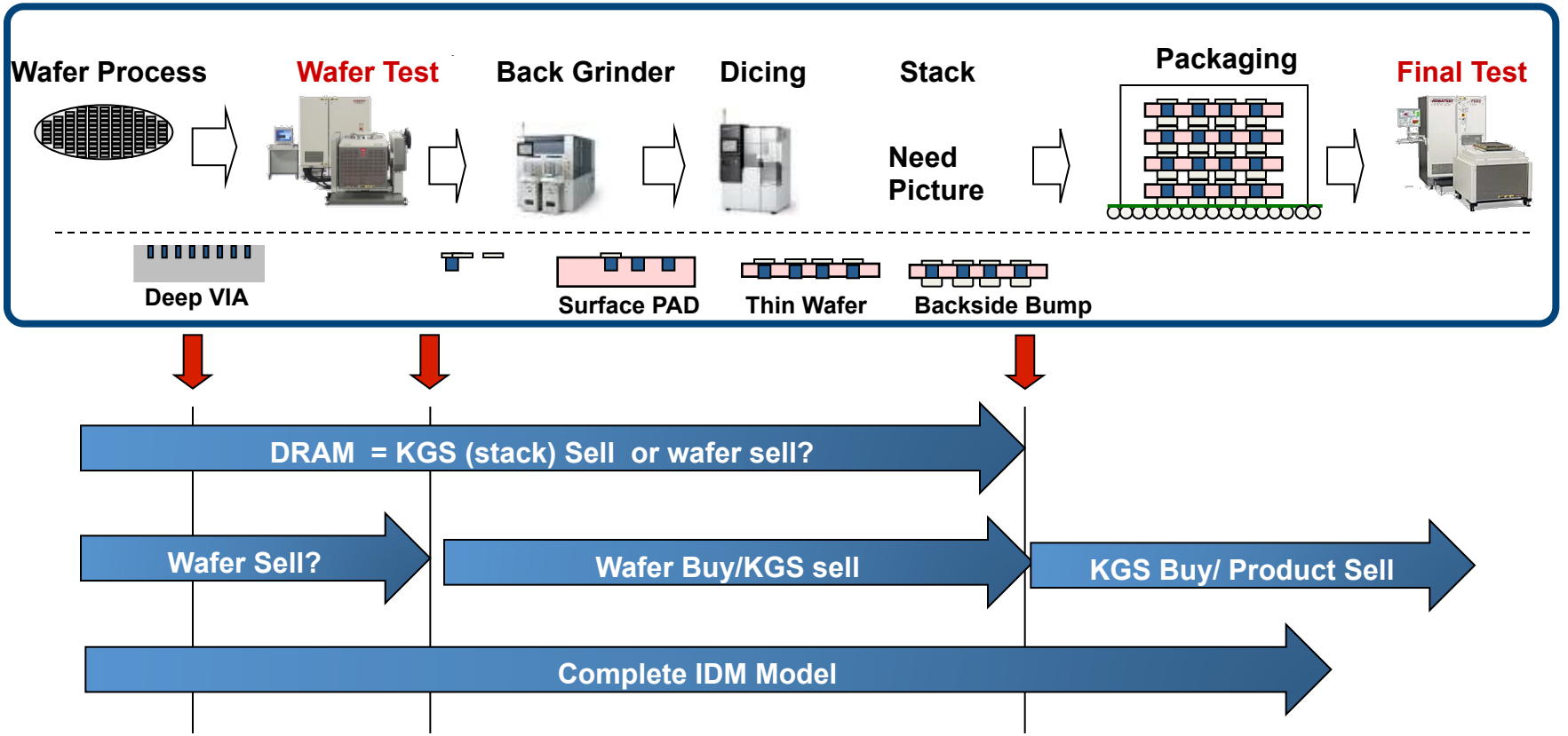
There are possible solutions to allow continued use of conventional wafer test architecture. They mostly require:

- Silicon Solutions (Test Access Ports, Direct Access & DFT)
- Direct Docking & improved coverage at wafer sort
- New Probe/Contact Solutions

These may come at a Test Yield penalty. "Probably Good Die" could become "Maybe Good Die" and unacceptable yield loss at stack, especially with very expensive components value added.

!! There is limited thermal coverage and no die interaction coverage

Mfg Flow differences



Each Interim Product must be "Known Good" Product

Must consider all options for Suppliers vs OSAT vs IDM

Partial Assembly

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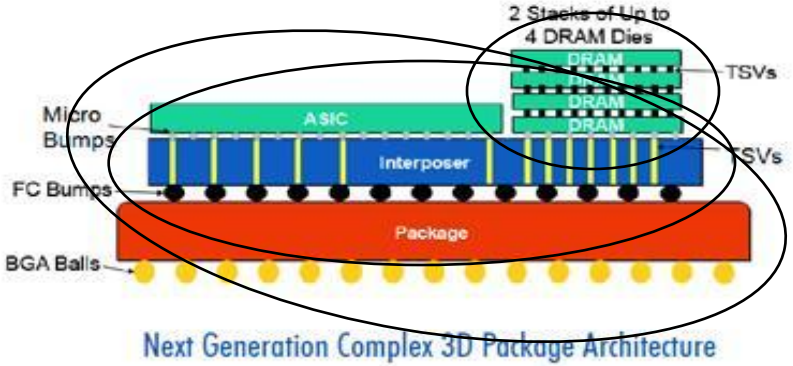
downstream integration



Source: TSV Stacked BGA, Amkor Technologies, Inc

Limitation - Limited test access from outside; landscape height variations

Countermeasures - IEEE & Jedec test ports; new test insertion points in the flow

Issues - Multiple suppliers; yield loss = scrap

Conclusion for thin, 2.5D & 3D

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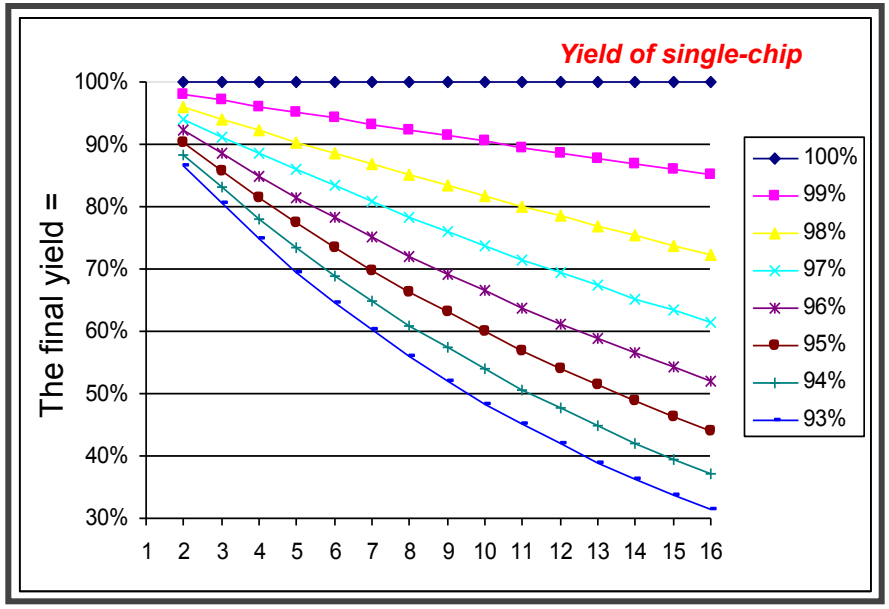
KGD <u>will be essential</u> to making 2.5D *<u>and</u>* 3D stacking cost effective

- Wafer vs. Singulated Die Test
- Zero Force Contacting
- Carrier Technologies
- Combined Electrical & Non-Electrical Test
- TSV Top/Bottom Contacting
- ATE close to the DUT (drive)
- Flexibility for Multi-pass
- <u>Thermal Management</u>

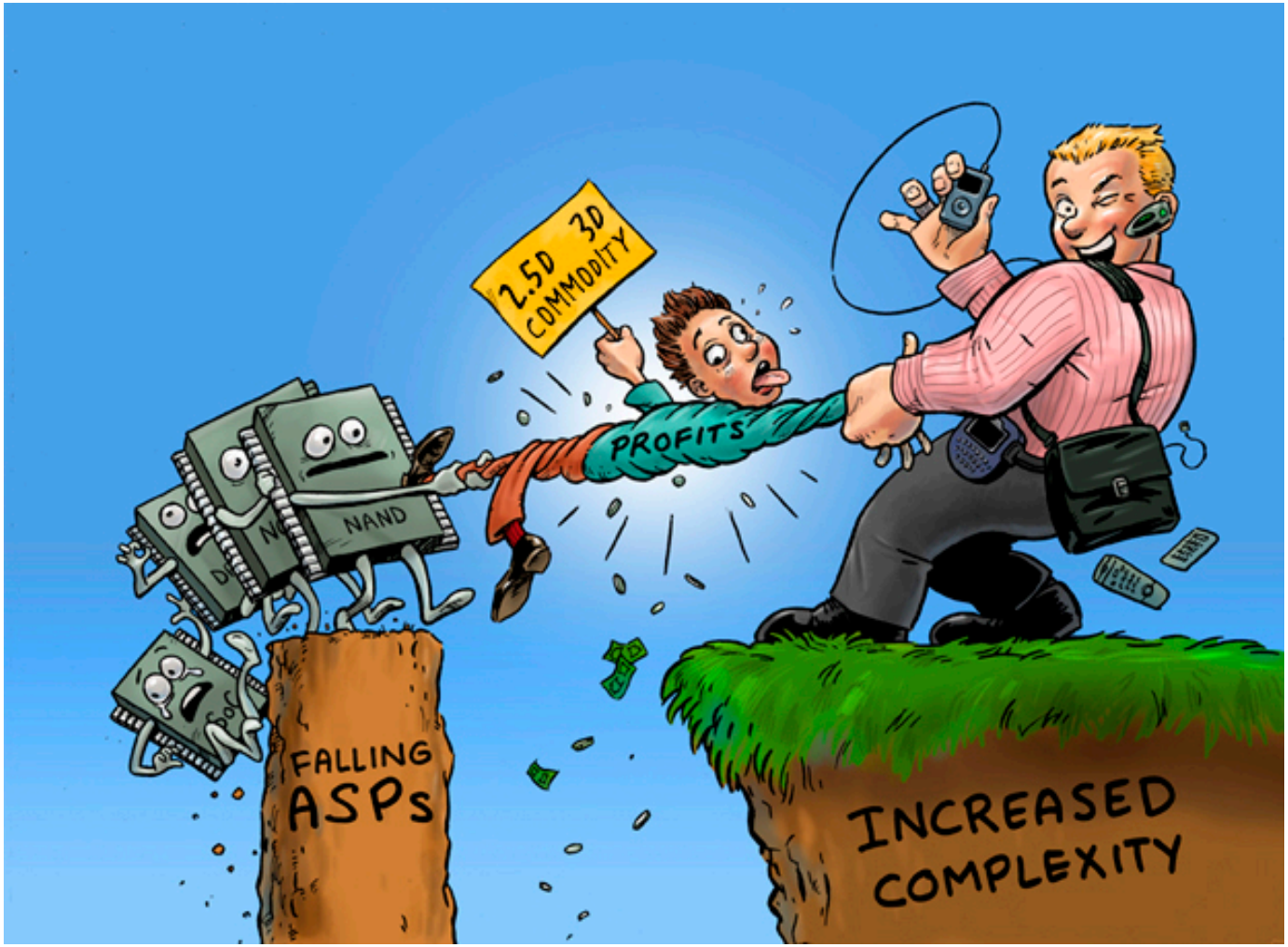
⇒ **<u>A Non-conventional test methodology that enables KGD</u>**



Commodity Success Challenge

Innovation into Commodity:

- Cost
- Risk
- Profit



Solutions Appearing

TSV Parametrics In-line

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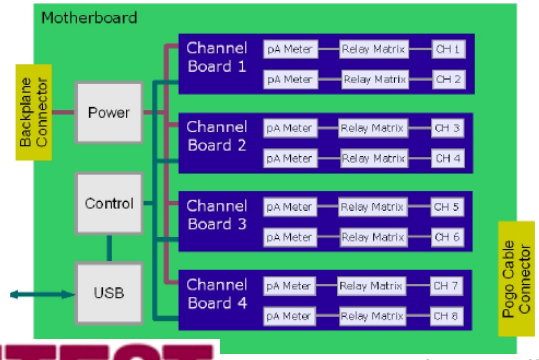
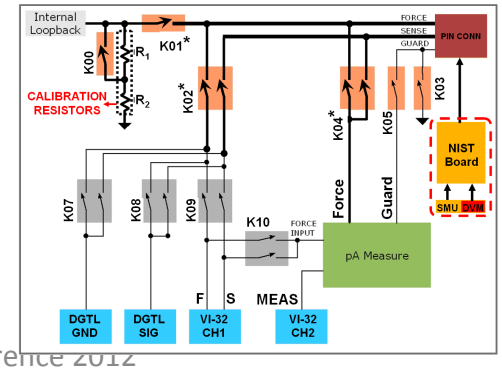
Solution for TSV test and characterization (ITC 2011 paper)

- typ daisy chain yield test + optical

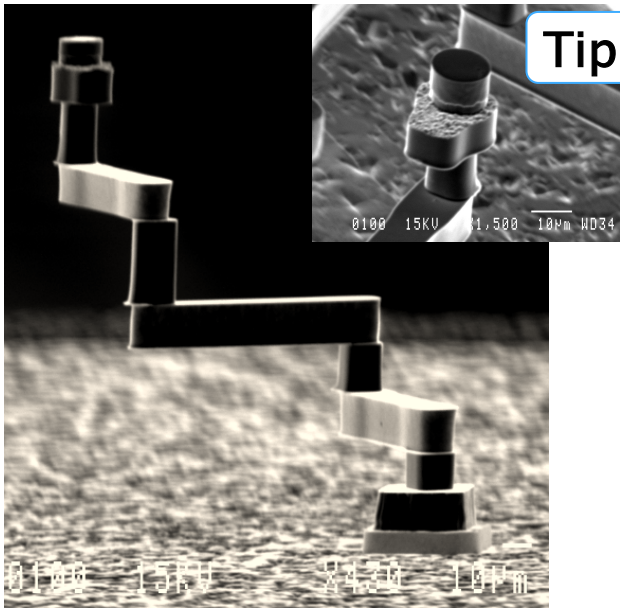
Channels per card	8
Channel Card Size	Single Slot
Multiplexing Capability (Any function to any pin)	pA Measurement VI Measurement Digital Resource Digital Ground
Control	Instrument controlled through workstation USB API for control through SmarTest software
pA Measurement Specs	200nA range: ▪±300pA + 0.25% of reading ▪10 pA resolution 2nA range: ▪±5pA + 0.5% of reading ▪100fA resolution
Digital Capabilities	Frequency measurement up to 50 MHz

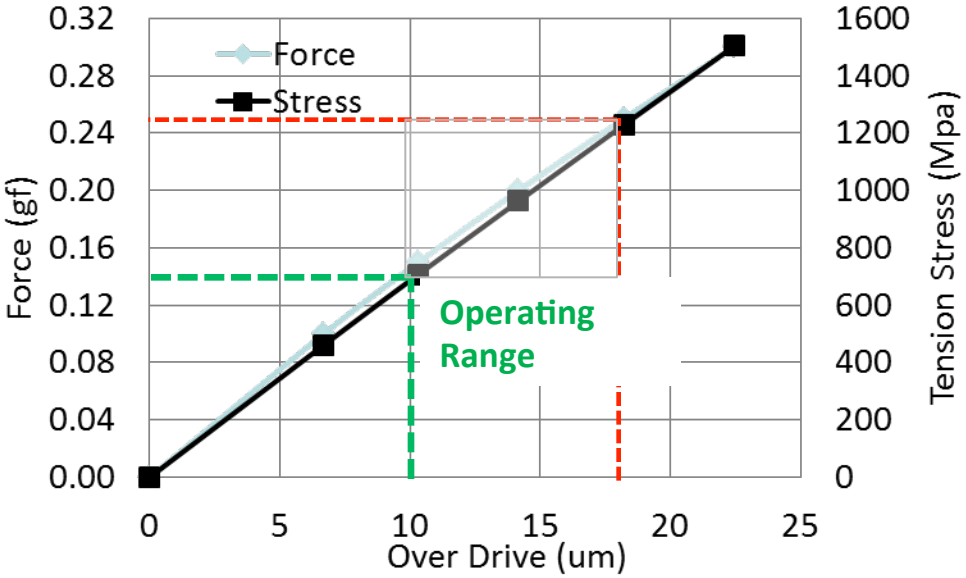


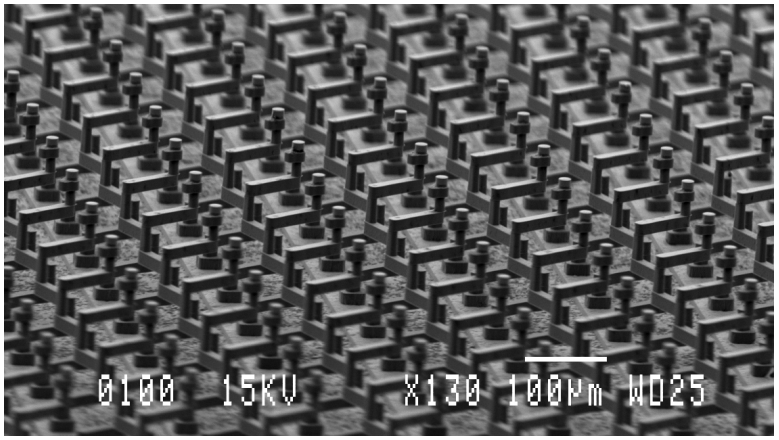


Contact Solutions

- < 1gram force
- 2500 probes
- <50um pitch capable







TOUCHDOWN TECHNOLOGIES
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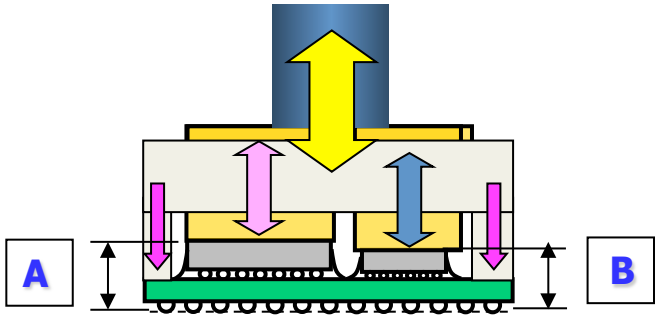
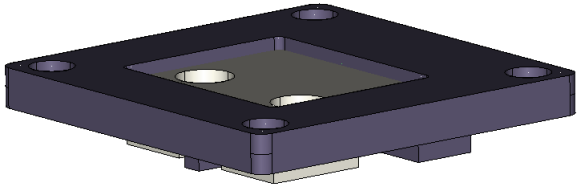
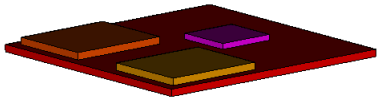
Partial Assy & Landscape

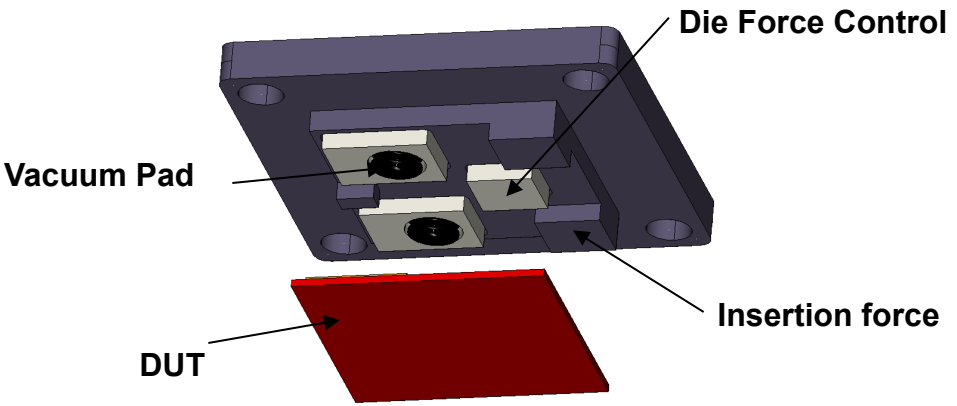
- Separated control for Insertion force and die force
  - –Enables different height control
  - –Die force control enable to avoid edge crack



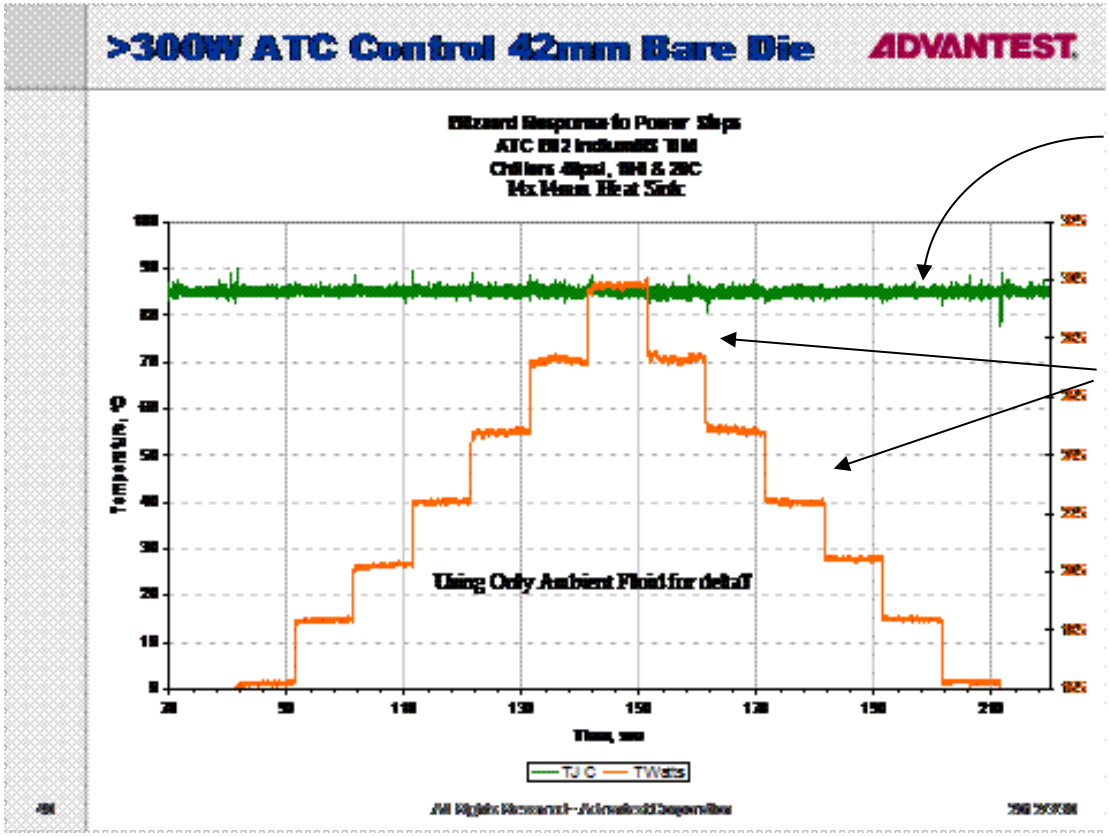
* Die and Memory
- Height A > B
  - Control die force for Die
  - Control balancing force at contact press







Active Thermal

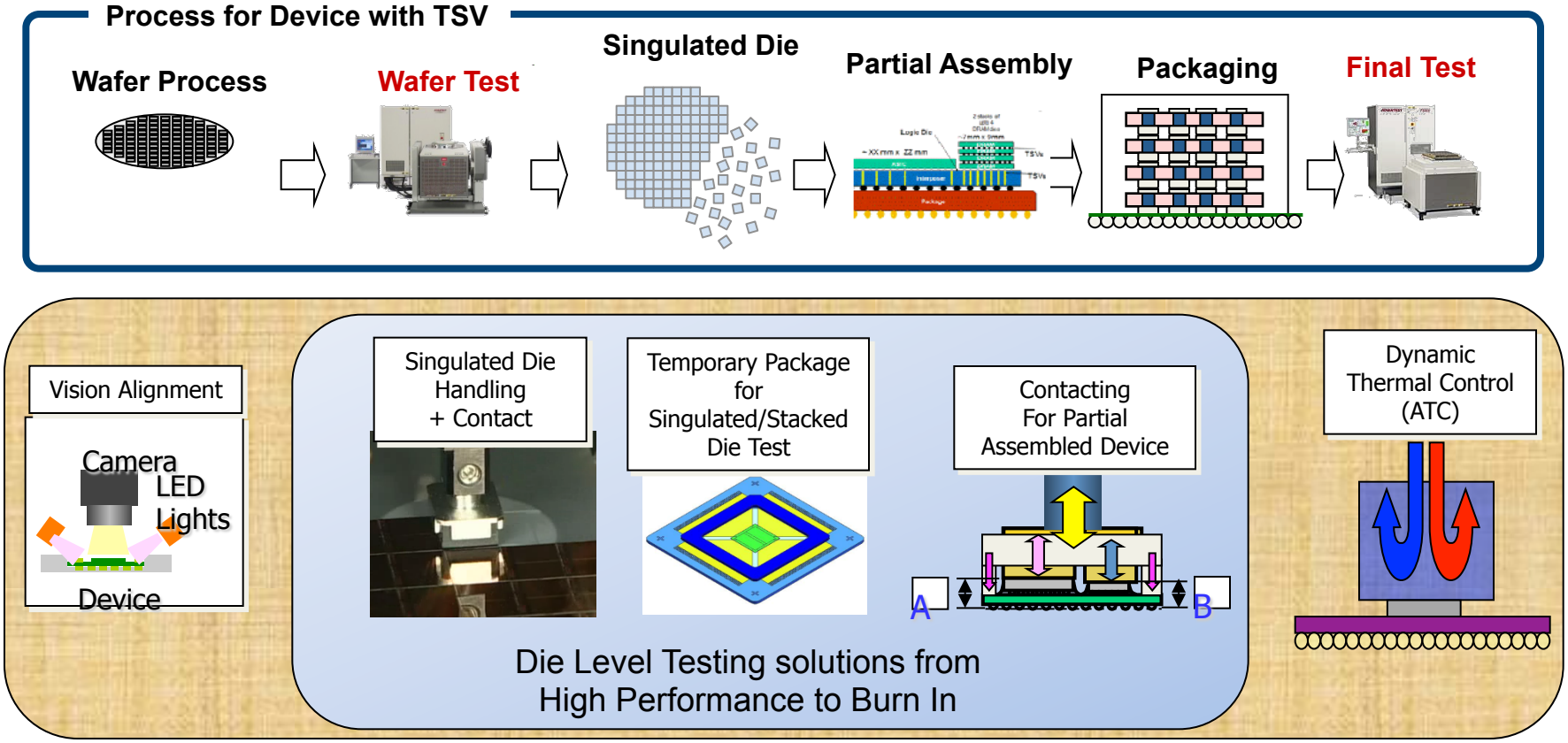


Excursion of Tjc
85C at up to 300W

Stepping the device's power consumption at 30W steps

- **This is scalable: DRAM, DFT, Power CPUs**
  - **Watts. Tens of watts. Hundreds of watts -- in real time**

New insertion points



Integrated solutions for die, partial, sub-assy + real time thermal control

HVM Stacked Devices

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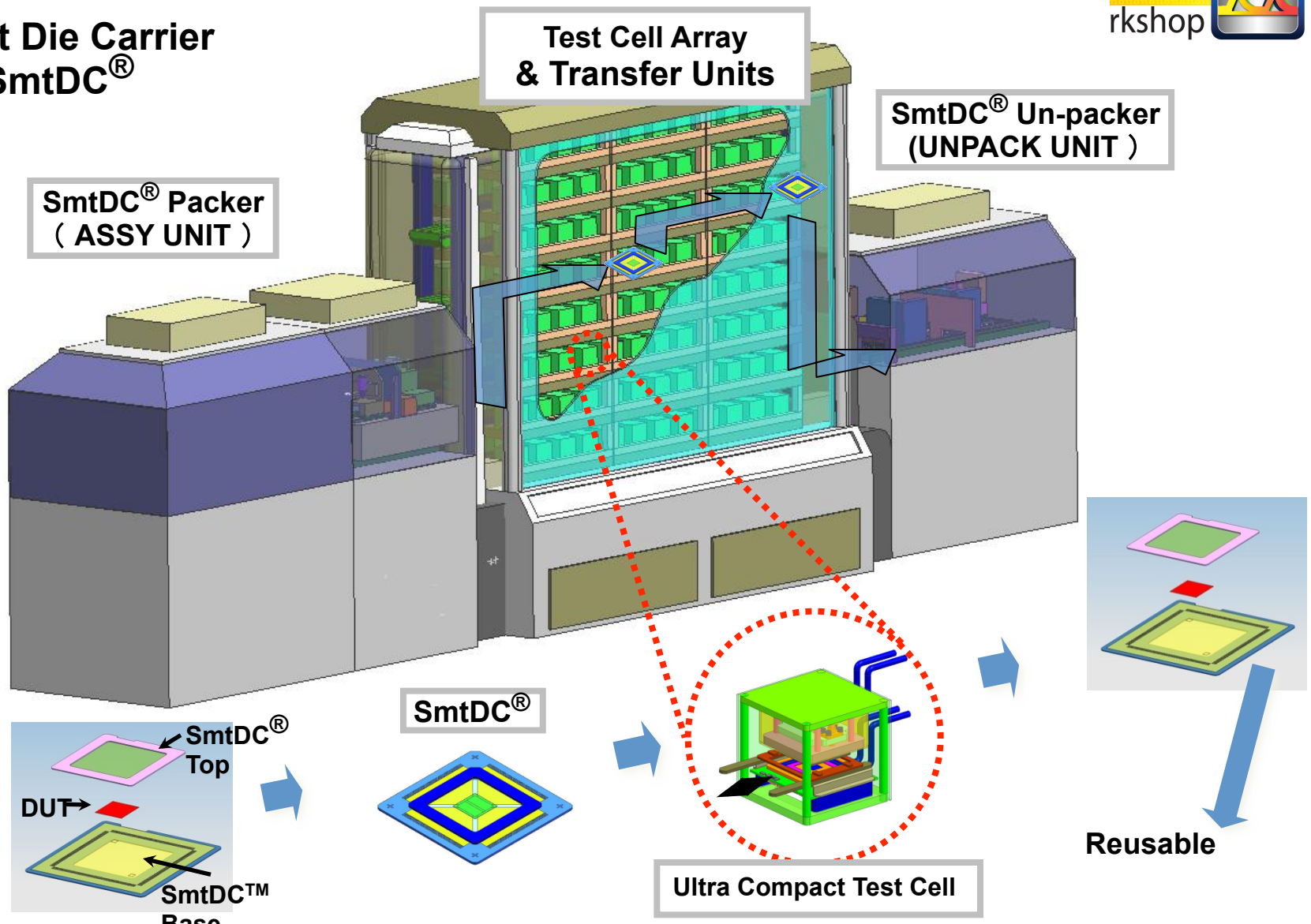
Smart Die Carrier SmtDC®



HVM for 2.5D 3D Stacked Devices

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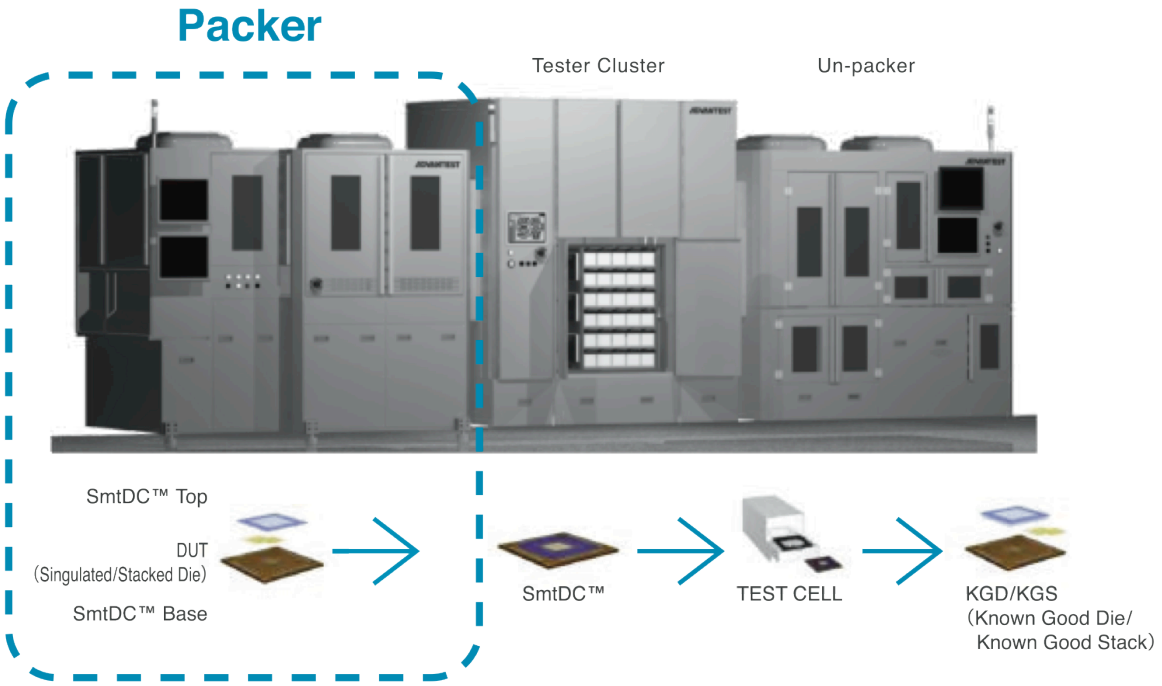
HVM proto unit
High parallel
for WideIO

Shown at
Advantest Expo
June 2012



Enables proprietary redundancy “after stack”
Full or partial stack with thermal, die interaction, retention, quality and long-cycle capability

Known Good Stack / Known Good Die integrated solution

Summary for 2.5D 3D Stacked Devices

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- New test points – IEEE, IMEC, GSA etc
  - Many new test points- but they will be selectively implemented after yield learning
  - Each flow will use different points; ***No*** flow will use all points; solutions will be different for awhile
- Optimized flows and test economy based on yield
- Key is tooling flexibility & integration (esp OSAT)
- Yield, Yield, YIELD

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Thank You