Silicon Valley Test Workshop

Silicon Valley Test Workshop 2012
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Mitigating Test Interconnect Issues for the Next Generation of High Speed, High Power Devices

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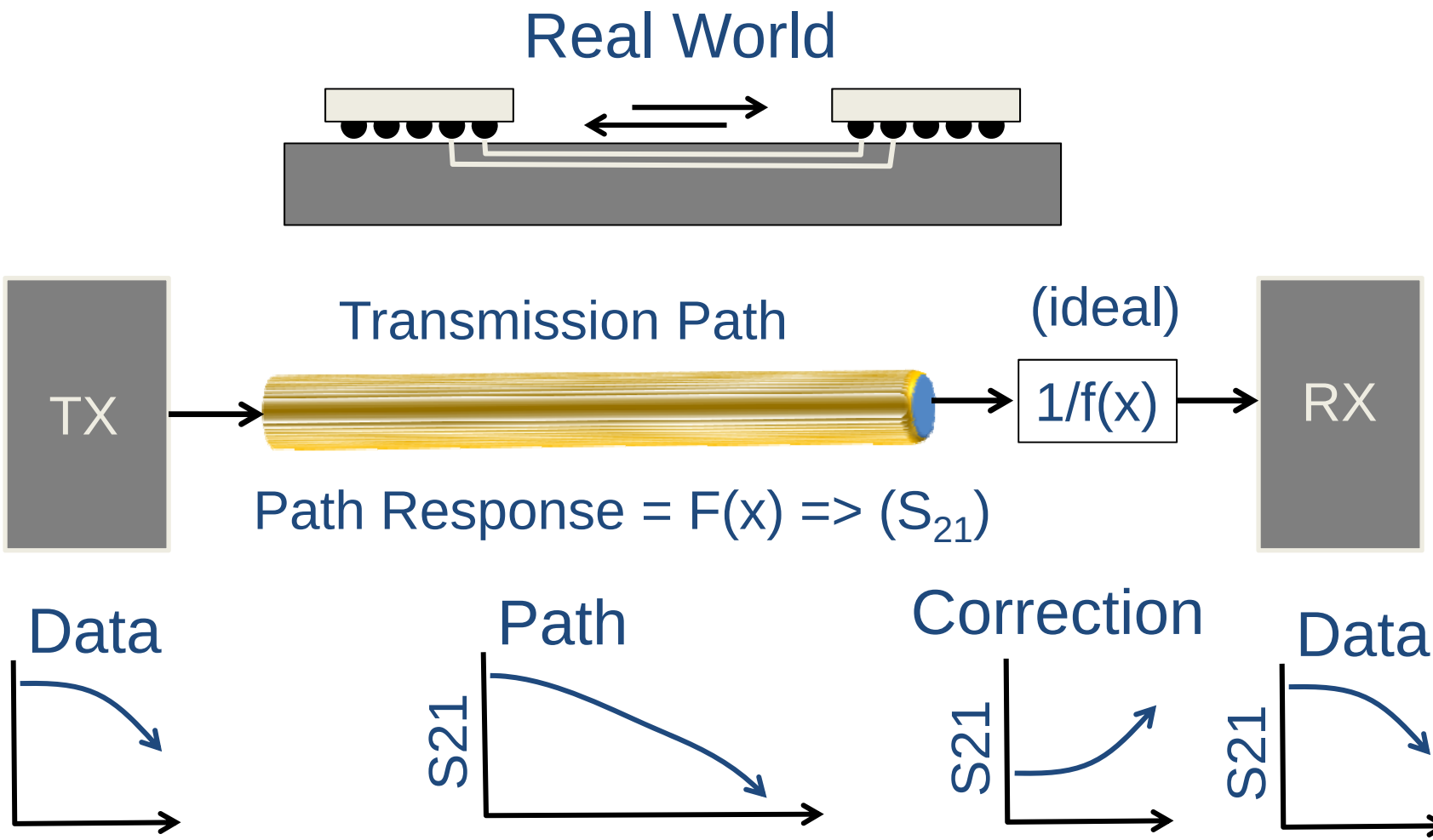
Purpose and Content

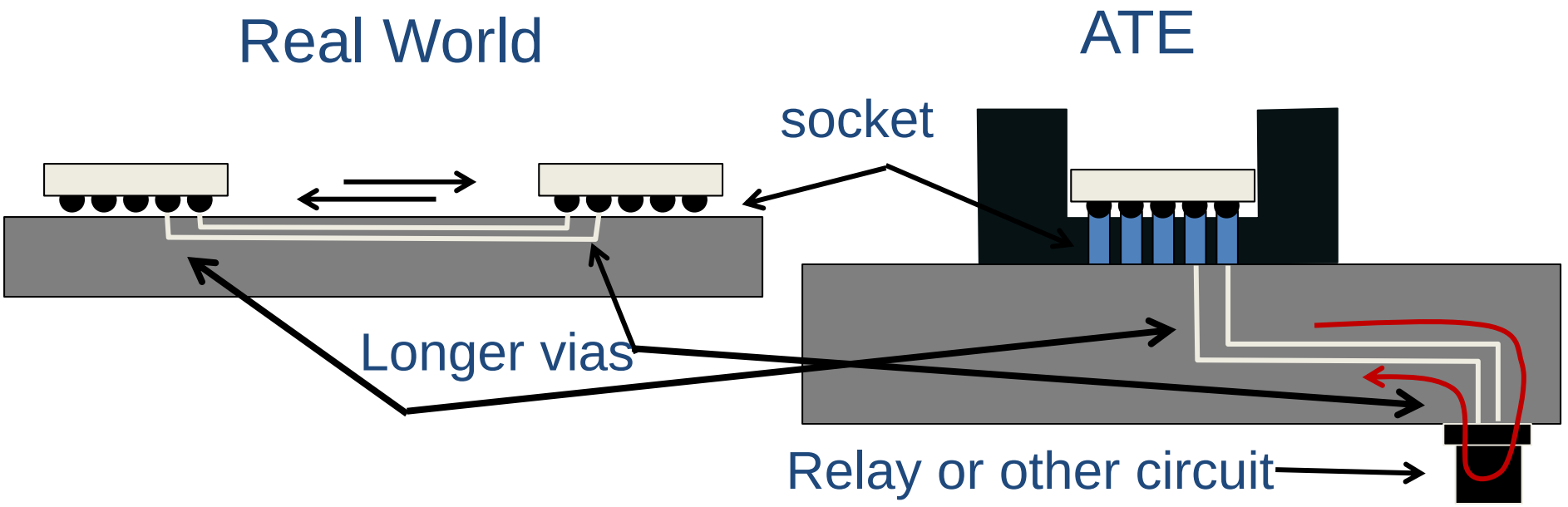
This Presentation discusses ATE-Specific Interface Issues for >25GB/s Devices

- **Comparing ATE to the "Real World"**
- **Signal and Power Integrity Conflicts**
- **Compromises**
- **Concluding Comments**

Comparing ATE to the “Real World”



Comparing ATE to the "Real World"



2 levels of Discontinuity
Package + Via

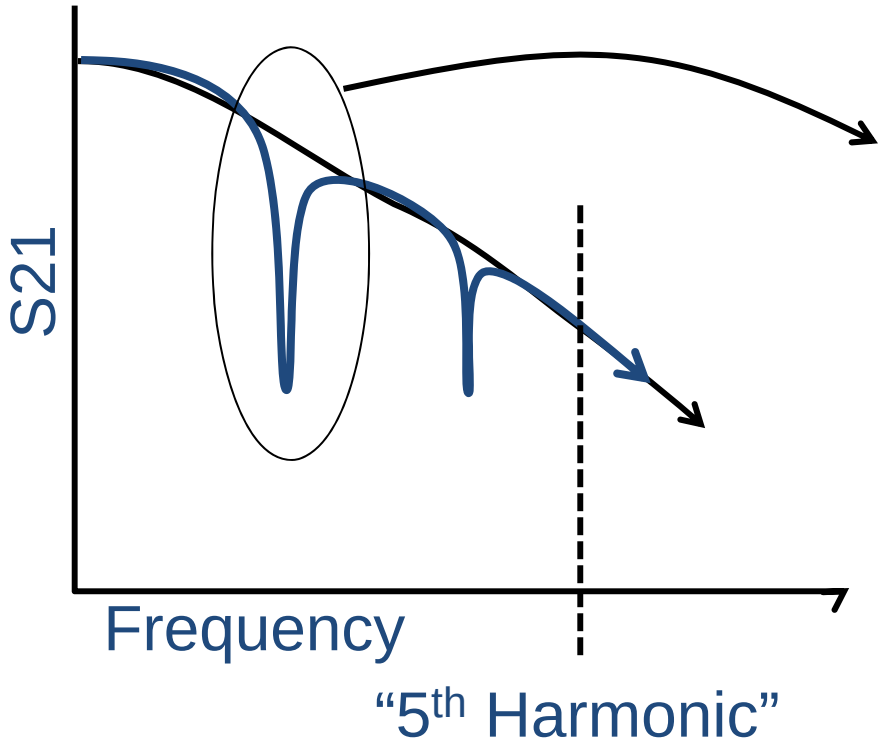
Full Adaptive Training

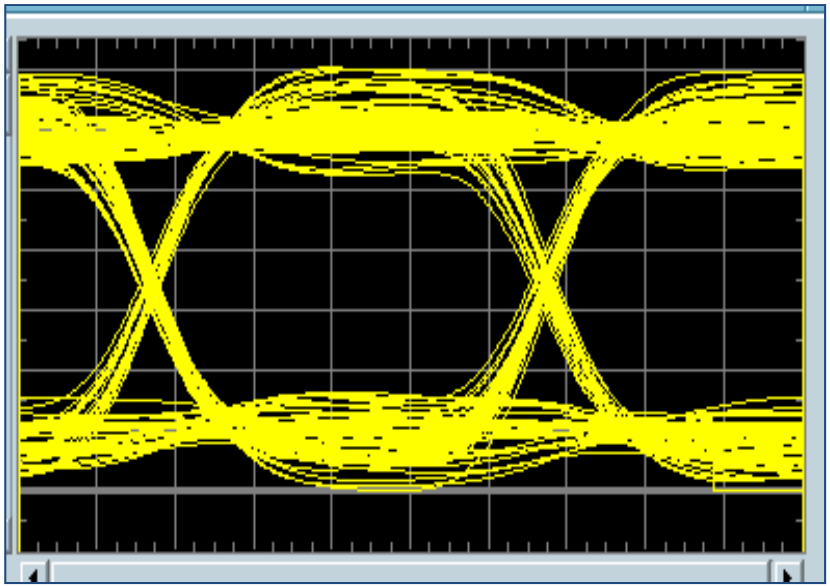
4 levels of Discontinuity
Package + Socket + Via + Relay

DFT Modified Training

Comparing ATE to the “Real World”

A reminder: Digital Pre-emphasis / equalization cannot correct for discontinuities, just monotonic loss.





Low Loss Material Data Eye, Via Discontinuity

Signal and Power Integrity Conflicts

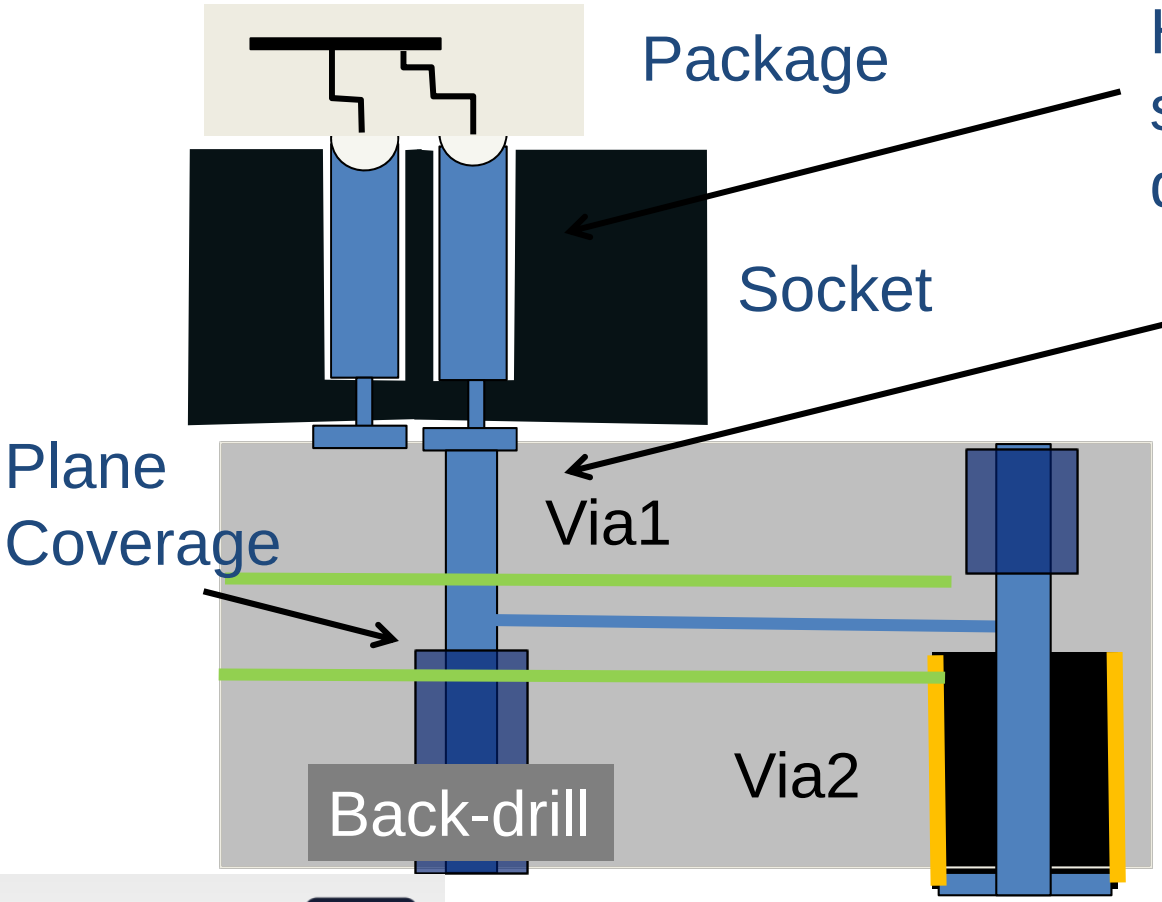
Key Signal Integrity Requirements:

1. Minimize Discontinuities
   a) Socket + Entry Via
   b) Via + Relay or circuitry
   c) Impedance Controlled or Coaxial Vias

2. Improve Isolation / Reduce Crosstalk
   a) Increased Spacing
   b) Better Ground Plane Coverage
   c) Increased Quantity Ground Vias

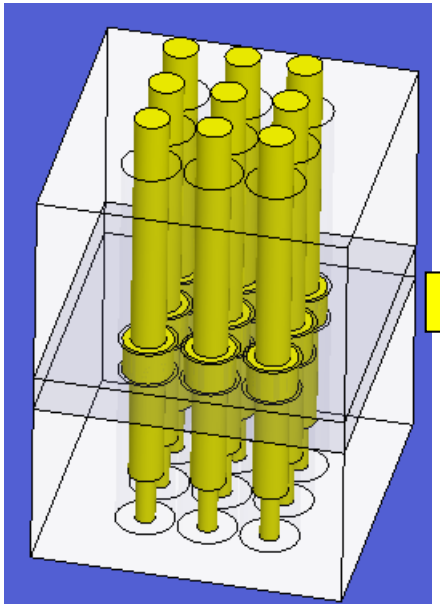
Signal and Power Integrity Conflicts

Key Signal Integrity Design:

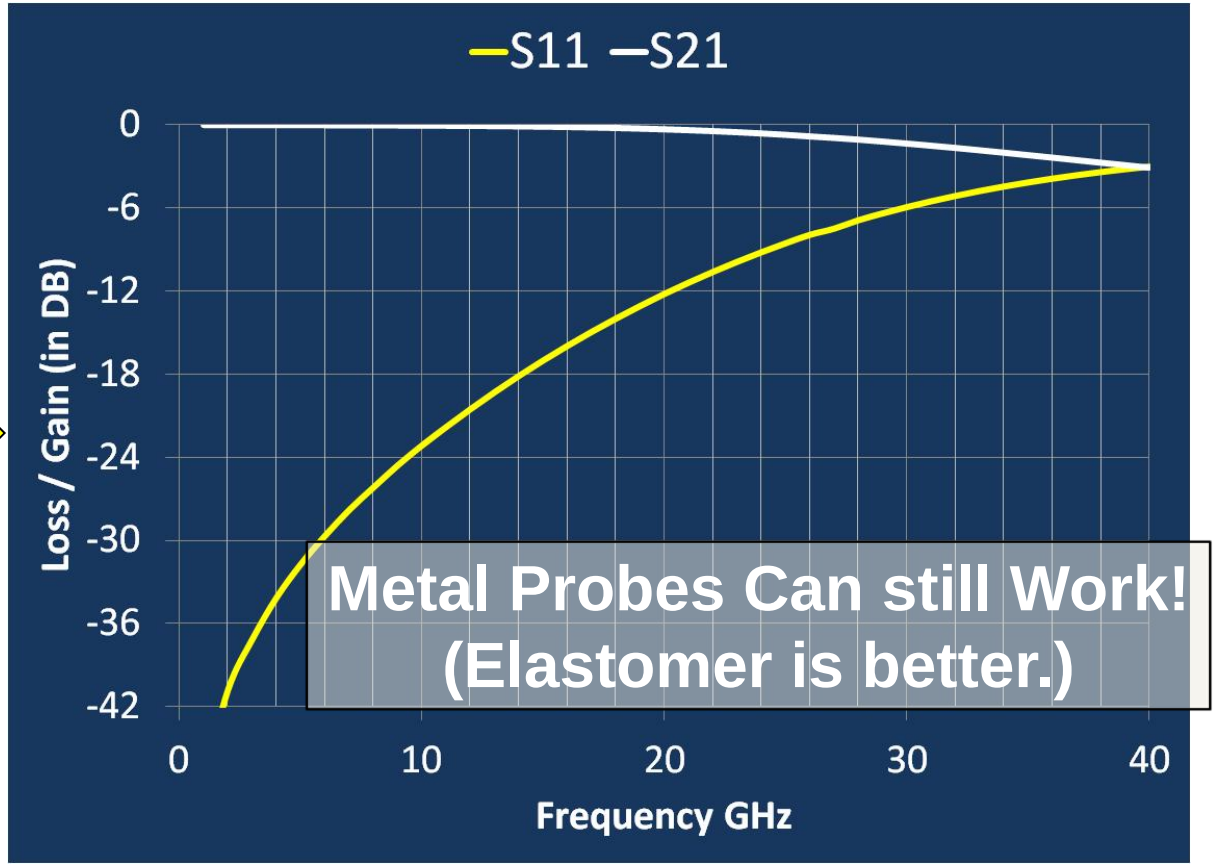


Signal and Power Integrity Conflicts

Key Signal Integrity Design:



Materials Adjusted



Signal and Power Integrity Conflicts

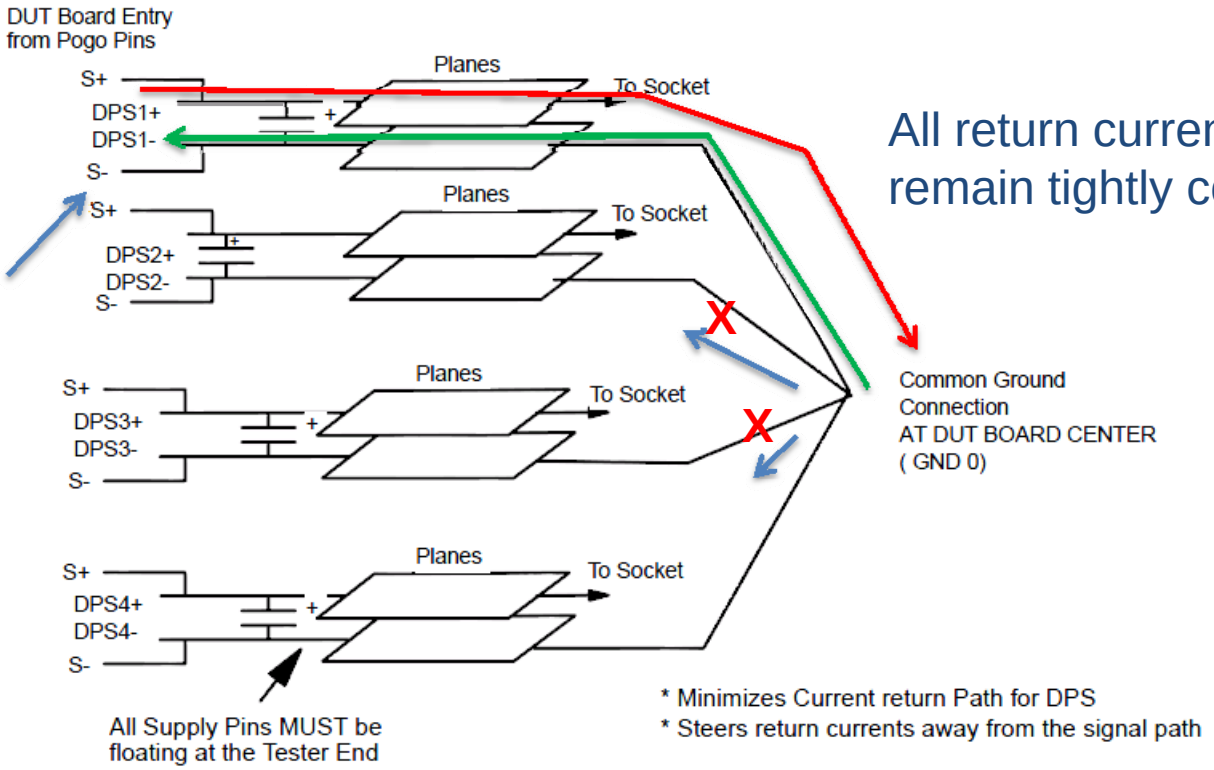
Key Power Integrity Requirements:

1. High Current Power Delivery
   a) Via Size, Plane Thickness, and Plane Redundancy
   b) “Web” or “Swiss Cheese” Effect
   c) Power Dissipation in the Socket pin

2. Transient Suppression
   a) Via and Socket Inductance
   b) Cres and ESR

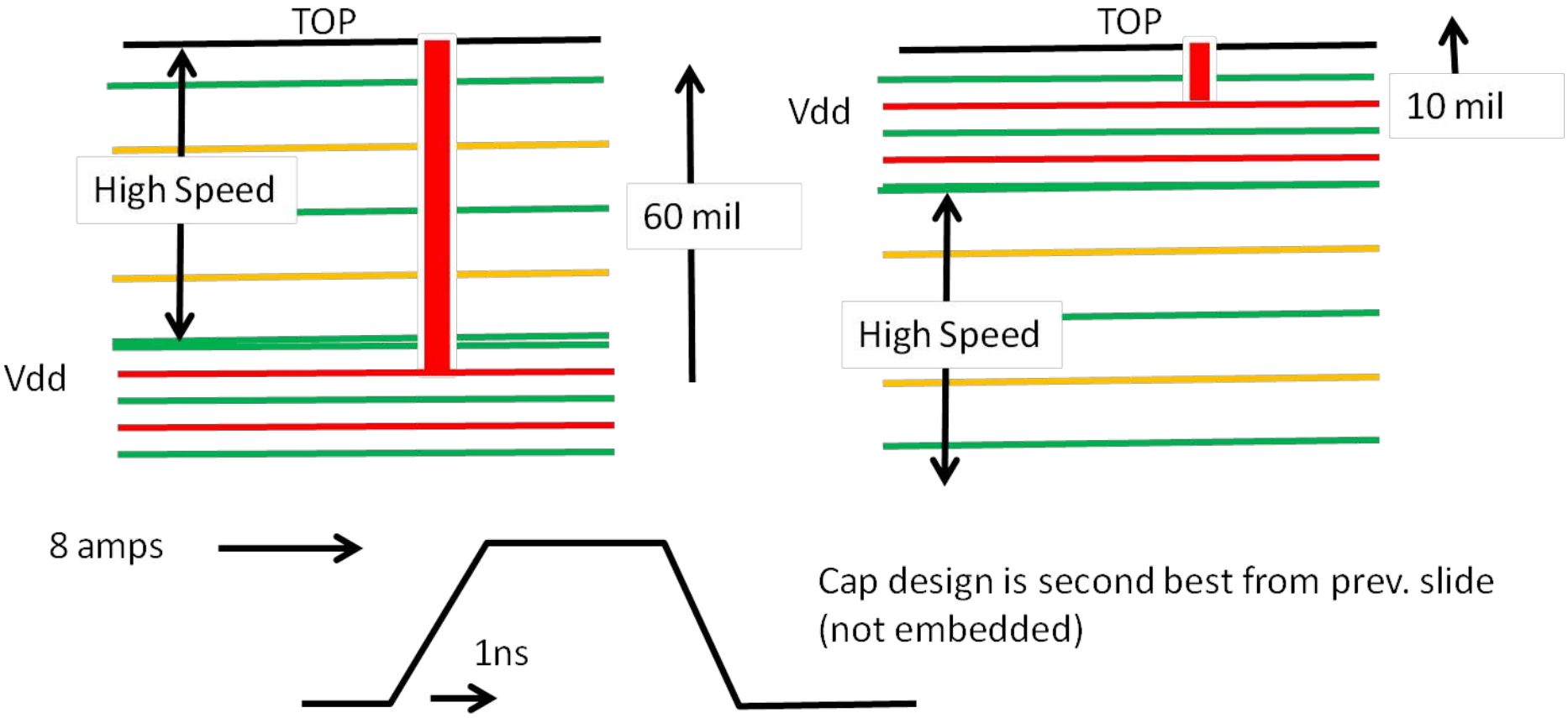
Differential Supply Concept

Route sense lines as tightly couple differential pair



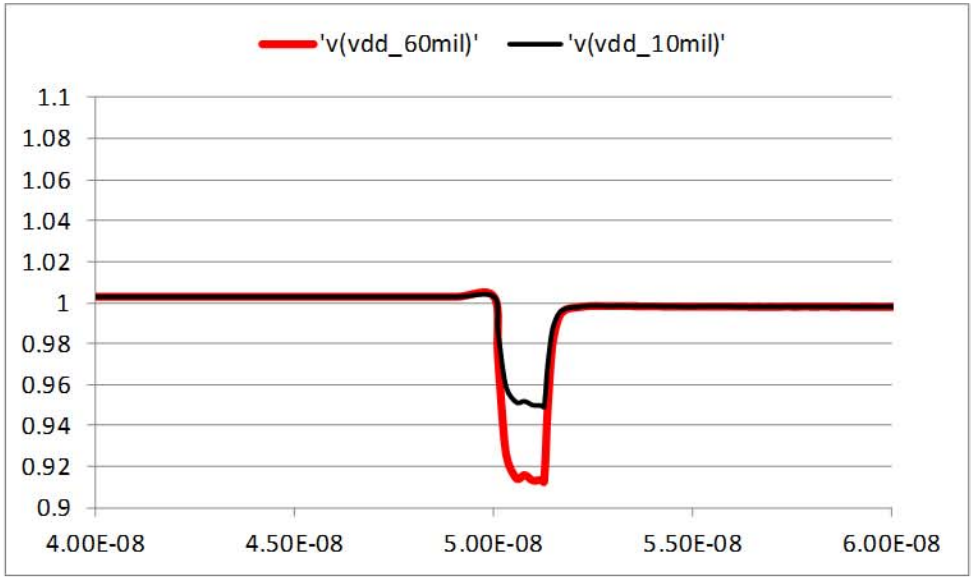
All return currents remain tightly coupled.

Supply Plane Location

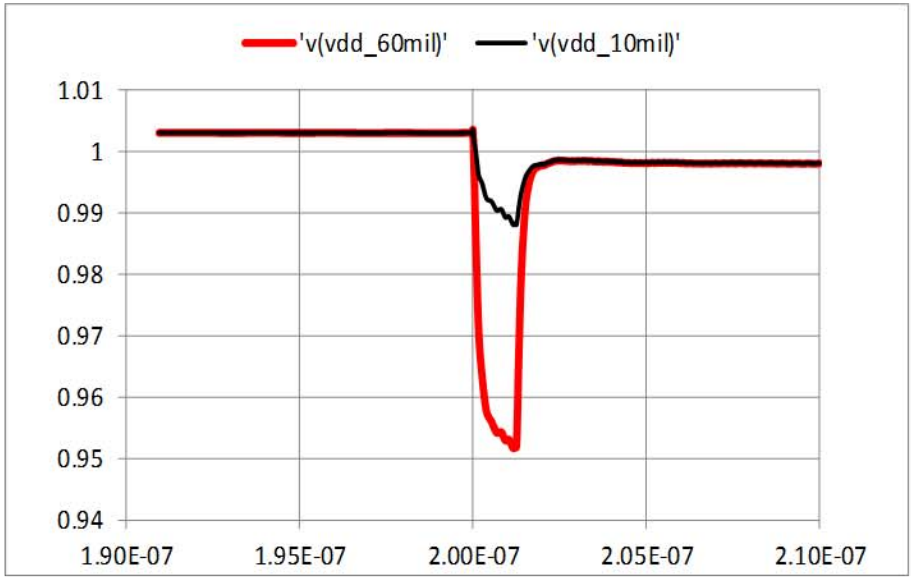


Supply Plane Location

Between Socket and DUT PAD



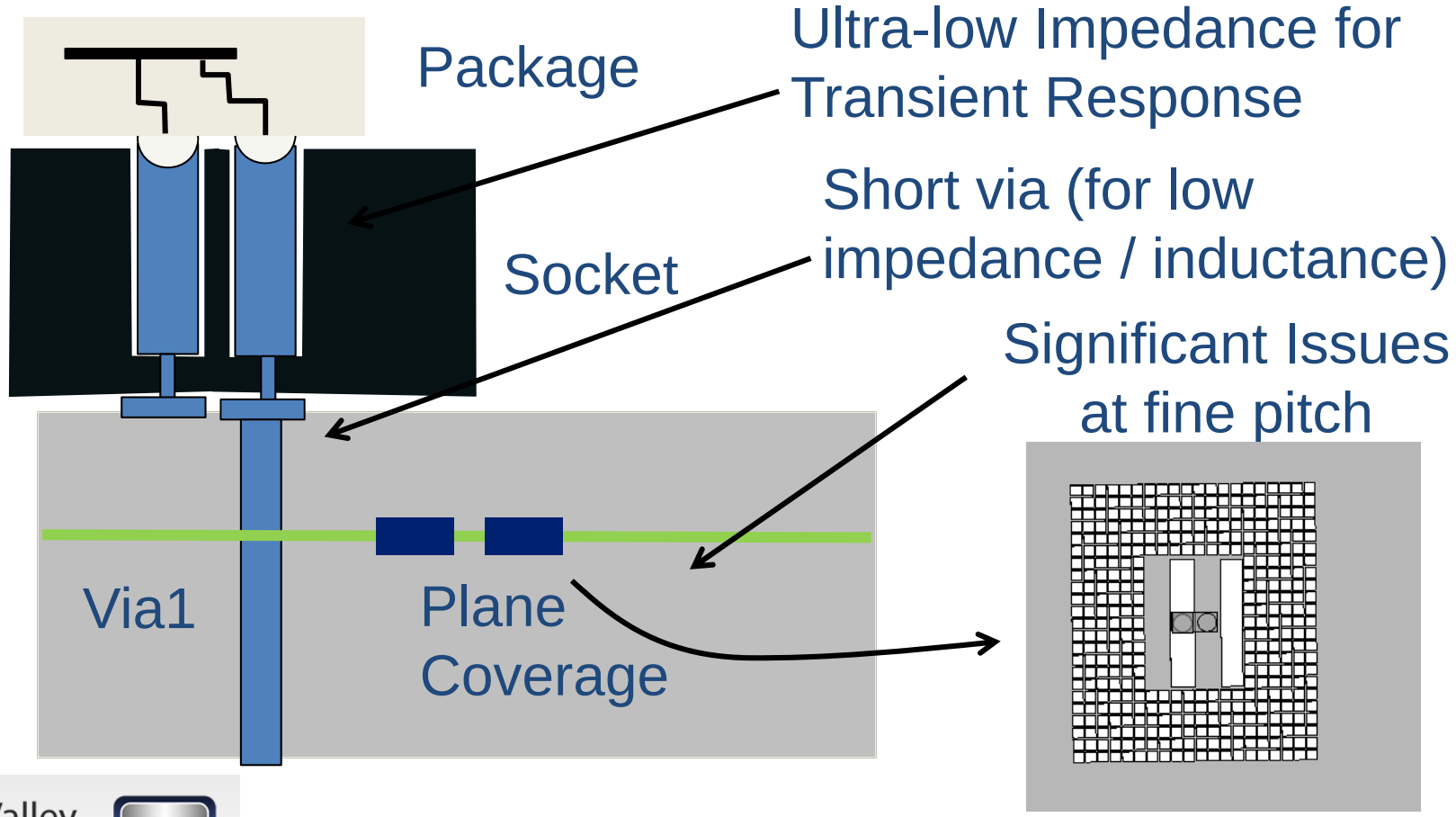
Between Socket and PC Board



The only difference is the plane location!!

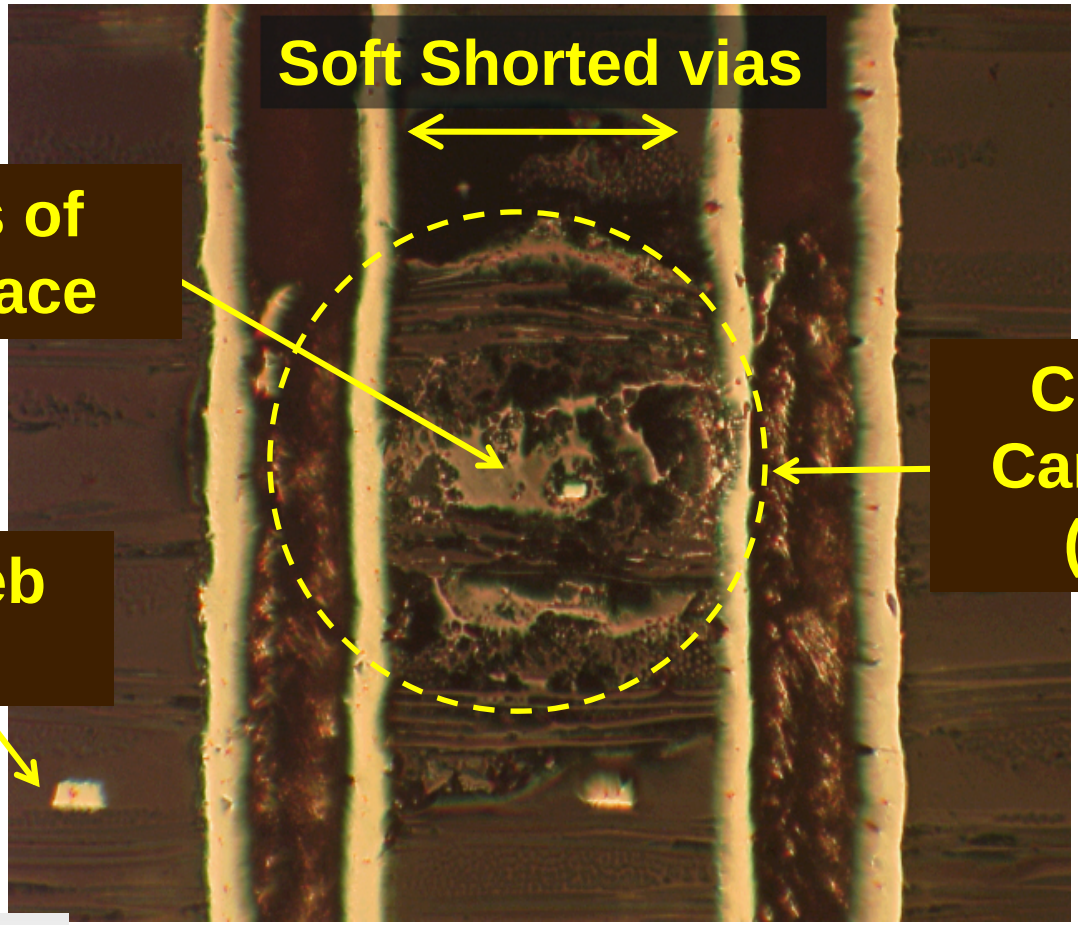
Signal and Power Integrity Conflicts

Key Power Integrity Design:



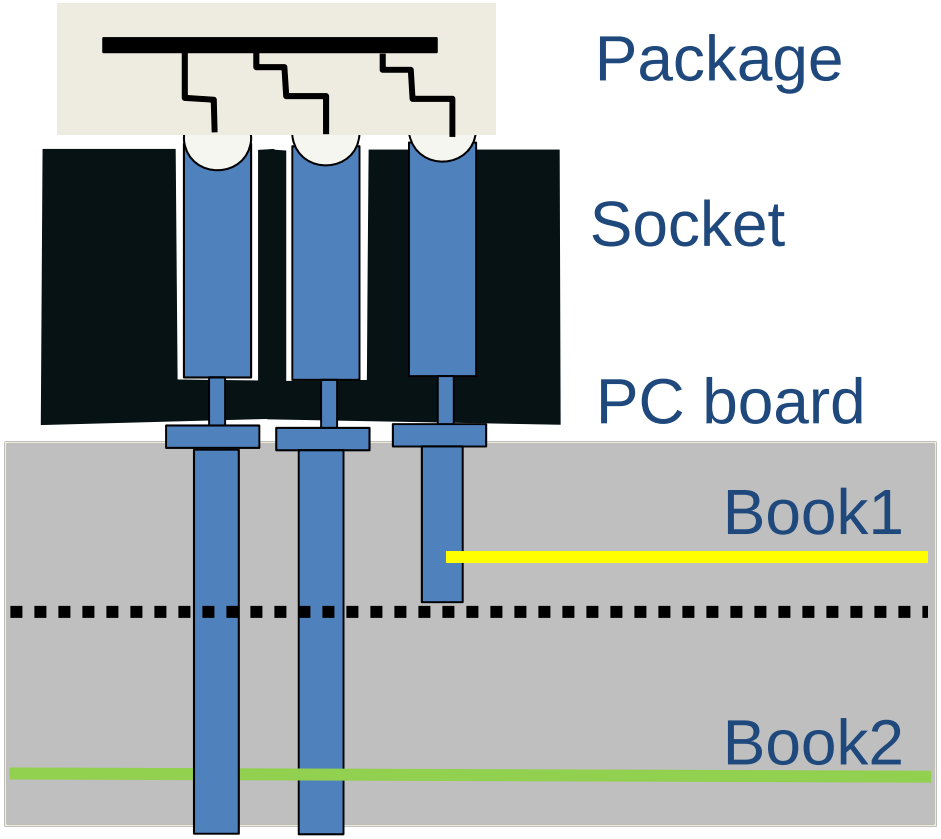
Signal and Power Integrity Conflicts

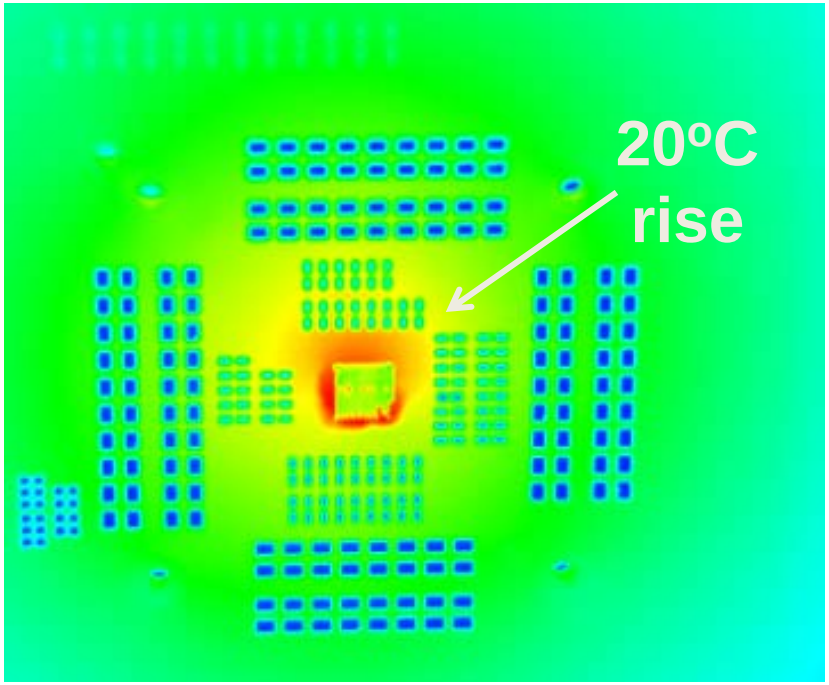
Key Power Delivery Design: (Power Web Issues)



Signal and Power Integrity Conflicts

Key Power Delivery Design: (Redesign for Fine Pitch)





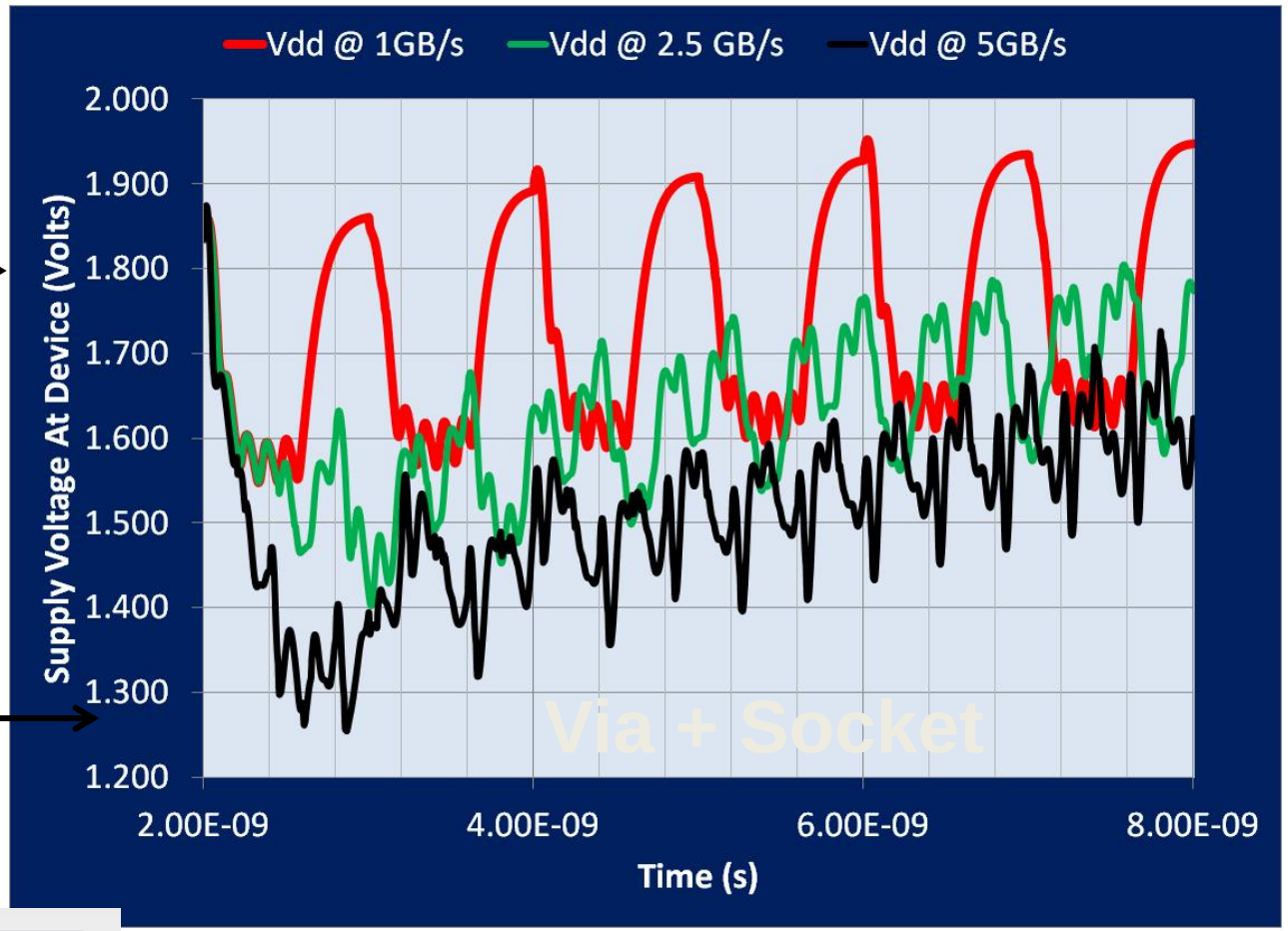
Thermal Image of 174 amps in 0.4mm pitch @ 115ºC

Signal and Power Integrity Conflicts

Key Power Integrity Design for Transients:

Vdd →

Droop →



Signal and Power Integrity Conflicts

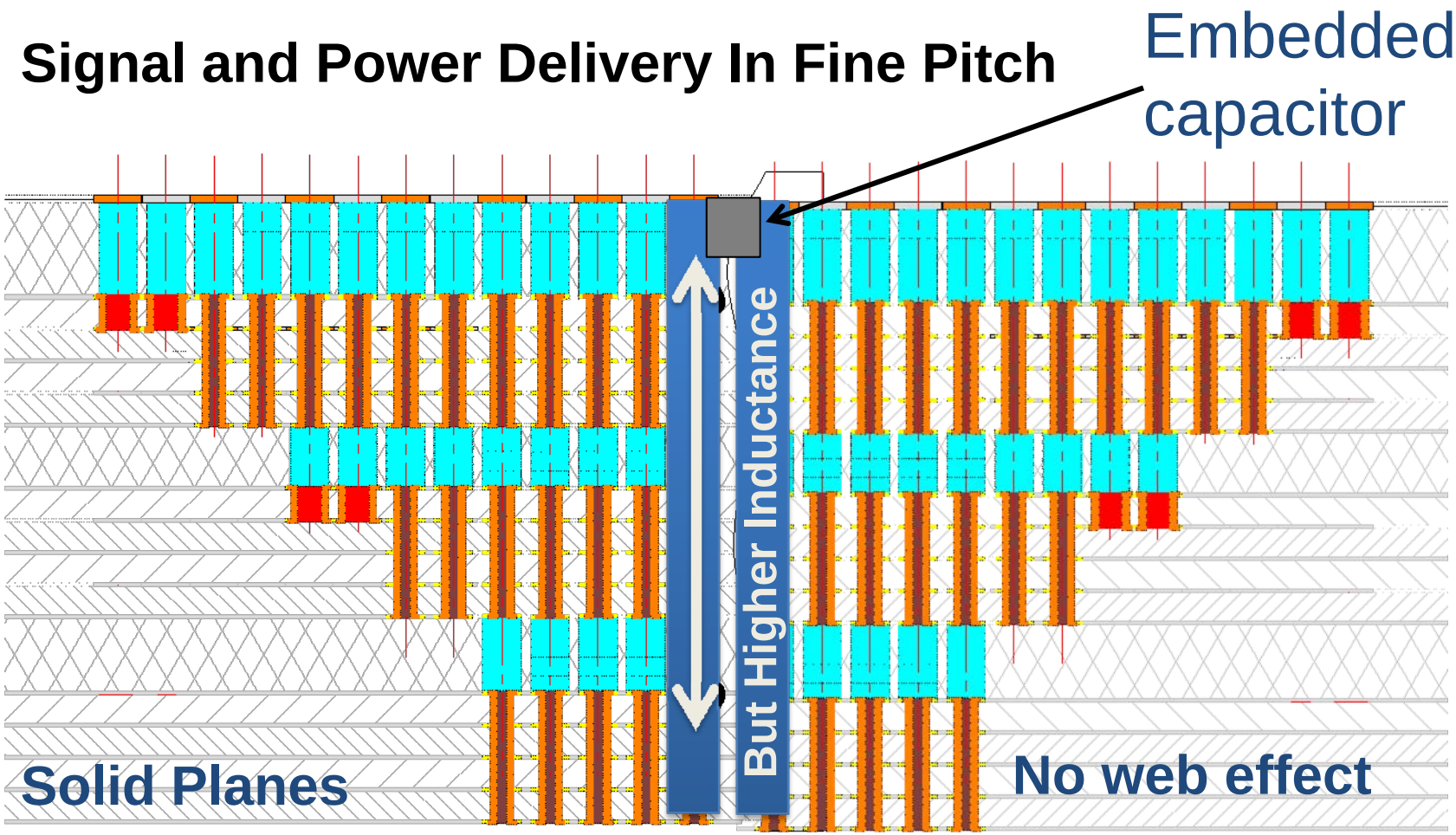
Summary of Critical Conflicts:

- Both PI and SI requirements want respective routing stacked high in the board.
- Fine pitch and back-drilling cause power delivery issues (“Web” or “Swiss cheese” effect).
- PI is far more sensitive to ESR – “equivalent series resistance”; Cres is a component of ESR.
- SI can survive longer socket pins; PI cannot.

Compromises

Load board Construction:

Signal and Power Delivery In Fine Pitch

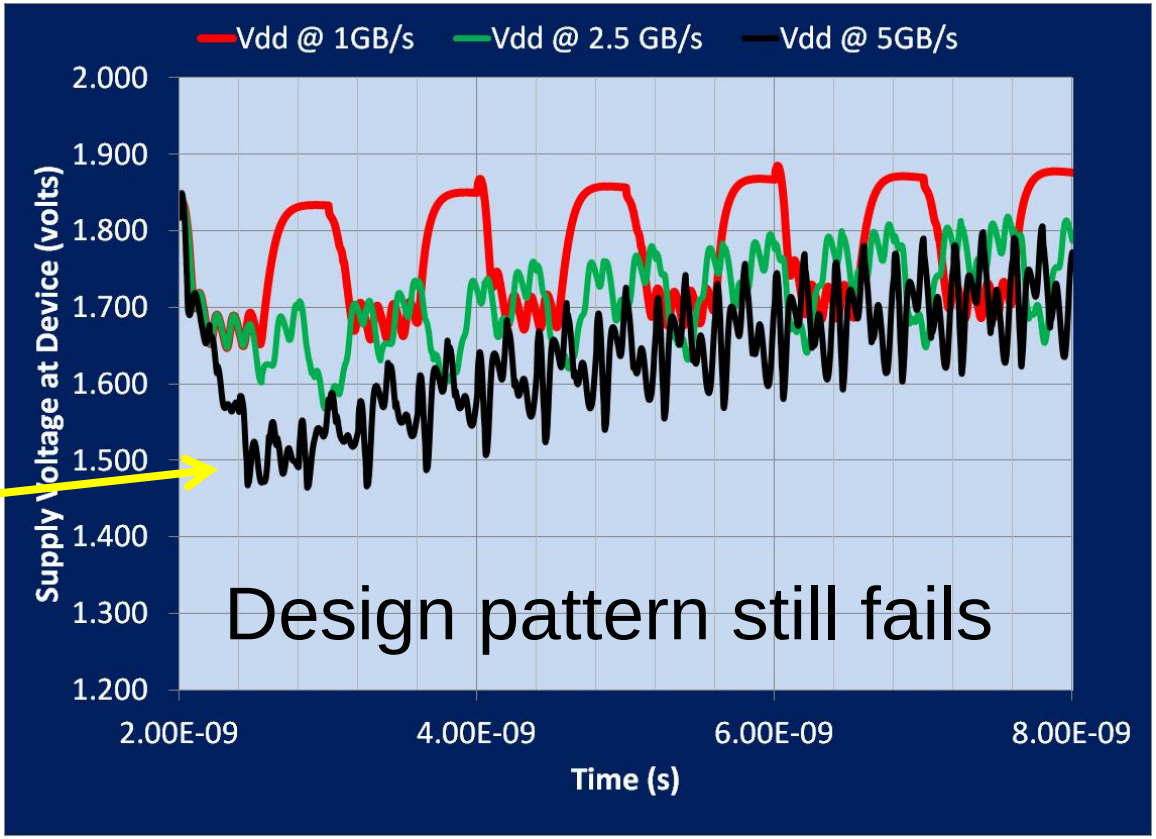


Compromises

Improved Power Delivery with Embedded Cap:

Vdd →

Socket causes droop

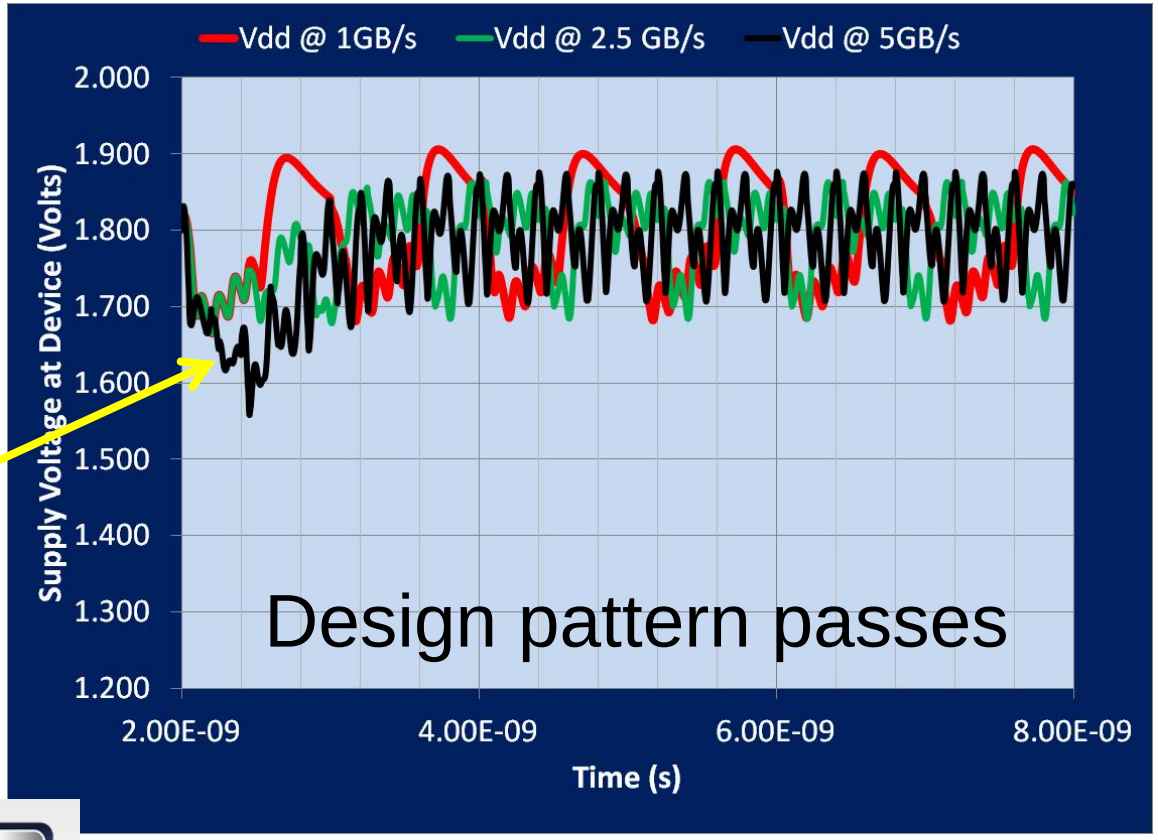


Compromises

Improved Power Delivery with Elastomer Socket And Embedded Capacitor:

Vdd →

Socket still causes droop



Concluding Comments

- Test will likely always compromise relative to any "real world" environment.
- Attention to Signal integrity issues over the past few years make ultra high data rates possible in pinned sockets.
- Power remains a challenge both for the PC board, especially in high power and fine pitch.
- Elastomer contactors, while not "production worthy", remain the best choice for transient power management.