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The Inductance Loop

Power Distribution in the Semiconductor Test Interface

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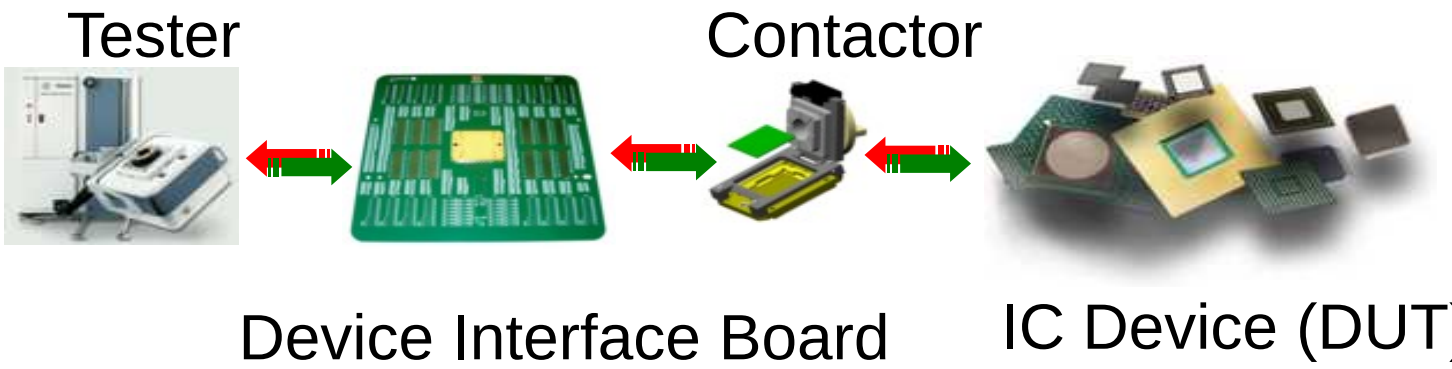
Agenda

- Introduction to Power Delivery Network (PDN)
- Defining the Required Impedance
- Optimizing the Contactor
- Contactor Example

Introduction to the Power Delivery Network

- Goal of Power Delivery Network (PDN)
  - Provide constant voltage to DUT in high dV/dt environment
- Requirement of PDN
  - Maintain low impedance path from tester to DUT across all frequencies

- Challenges of Semiconductor Test Environment
  - Fast switching
  - Dense signals
  - Limited space for decoupling
  - Cost – Capacitors, Material, Contactor



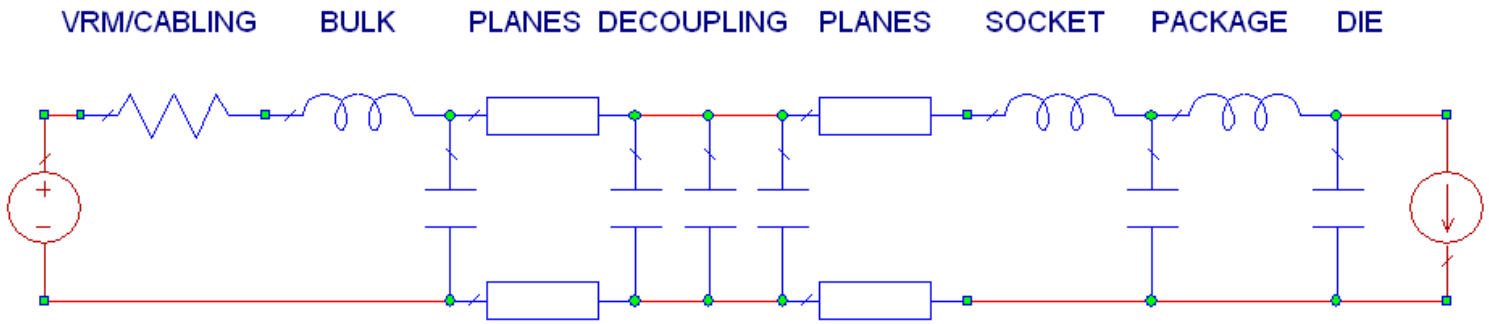
Introduction to the Power Delivery Network

- Power nets are transmission lines similar to signal nets
  - Optimal impedance of power nets is 0 Ω (instead of 50 Ω)
  - Low impedance → constant voltage

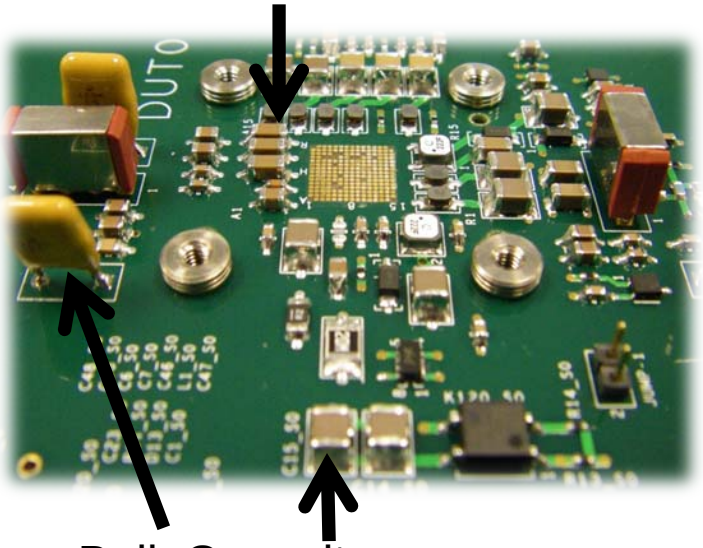
$$Z = \sqrt{(\frac{L}{C})} << 50$$

- Inductance increases impedance and limits response time of power supply
- Capacitance reduces impedance and improves response time of power supply

Path of Power Delivery Network

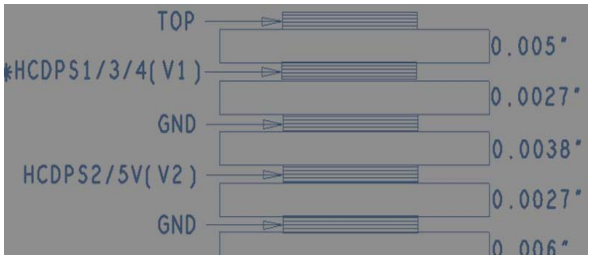


Decoupling Capacitors

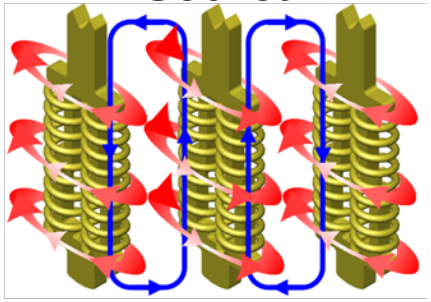


Bulk Capacitors

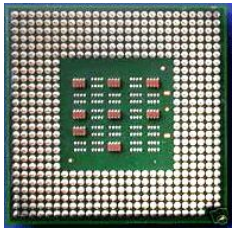
Plane Capacitance



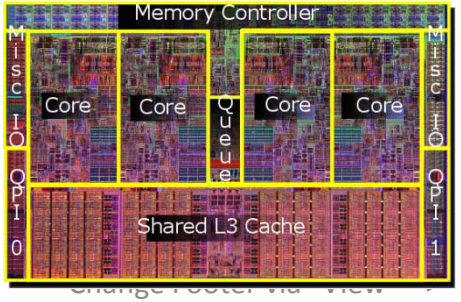
Socket



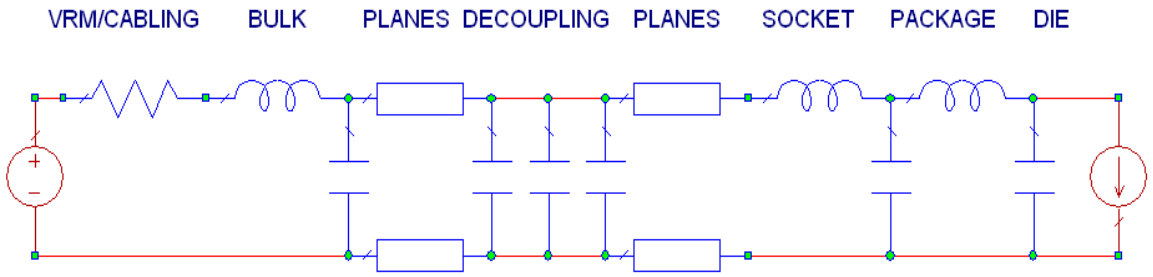
Package Leads/Capacitors



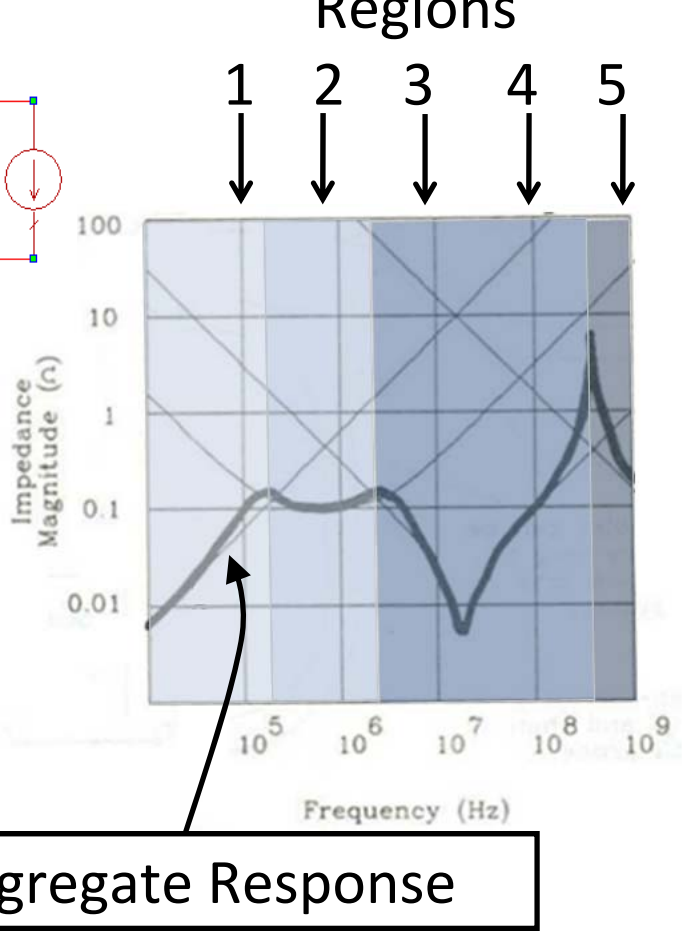
On Die Decoupling



Impedance Profile of PDN



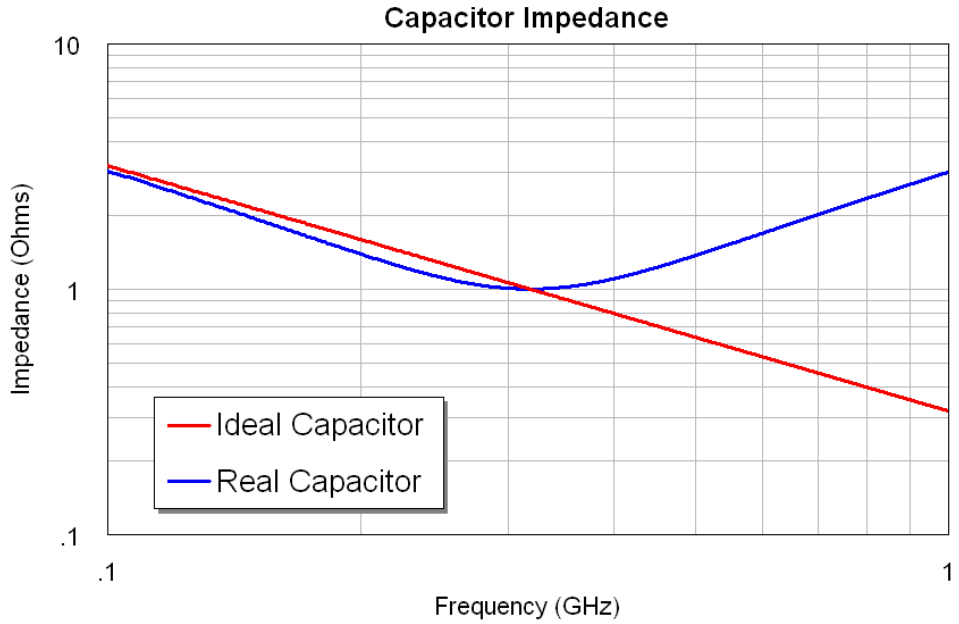
1. Power supply wiring (sub-500kHz)
2. Bulk capacitors (500kHz - 10MHz)
3. Decoupling caps (1MHz - 100MHz)
4. Power planes (100MHz - 300MHz)
5. On die decoupling (300MHz+)



***Adapted from "High-Speed Digital Design", Howard Johnson, 1993, p277.

Real Capacitors and ESL

- Ideal capacitors have no resonance point
- Real capacitors become inductors above resonance point
- Equivalent Series Inductance (ESL) limits the useful frequency range of capacitors

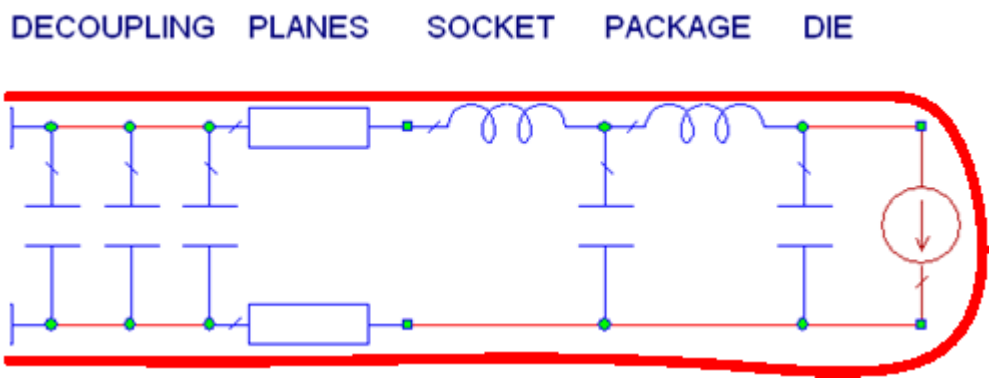


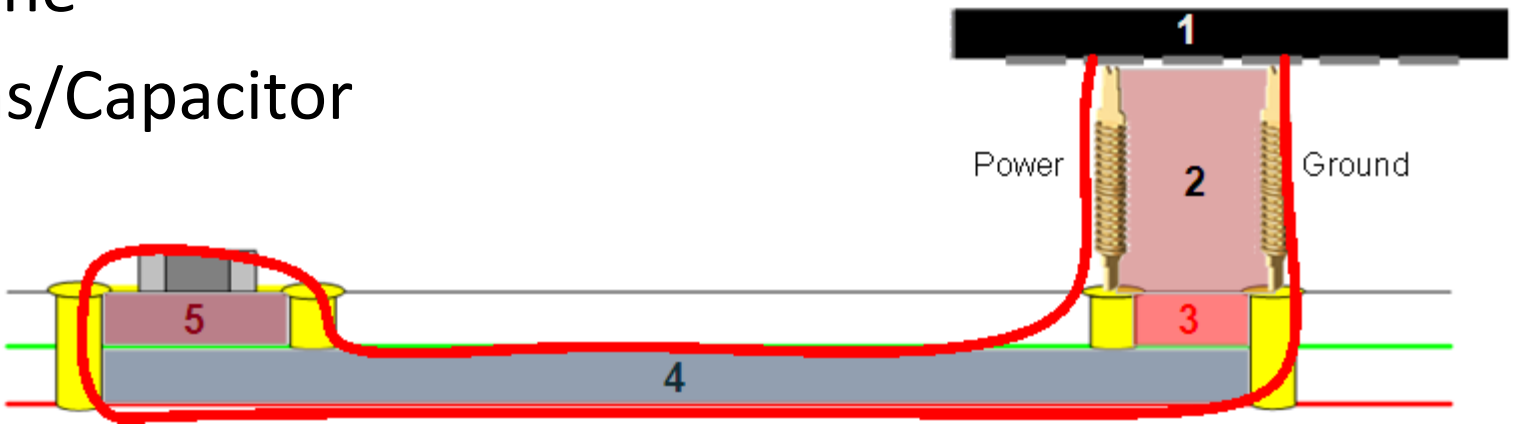
Ideal

Real

Decoupling Capacitor Loop

1. Die/Package
2. Contactor
3. DUT Vias
4. Plane
5. Vias/Capacitor





***Adapted from "Best Board Design Practices for PDN", Eric Bogatin, 2006.

Defining the Required Impedance

- Required impedance is application specific
  - Every device has its own unique current profile
  - Difficult to apply a standard to PDN design
- Device specification dependent
  - Impedance calculated from datasheet specifications
- Various methods based on:
  - Maximum transient currents
  - Maximum power consumption
  - Simulated IC models

Impedance Derivation Method

- Use device datasheet information to derive impedance value
  - Estimate based on maximum transient current
  - $Z_{REQUIRED} = V_{DD} \times RIPPLE(\%) / I_{TRANSIENT}$

    (Assume $I_{TRANSIENT} = 0.5 \times I_{MAX}$)
  - $Z_{REQUIRED} = 5V \times 0.05 / (0.5 \times 0.5A)$
  - $Z_{REQUIRED} = 1\Omega$

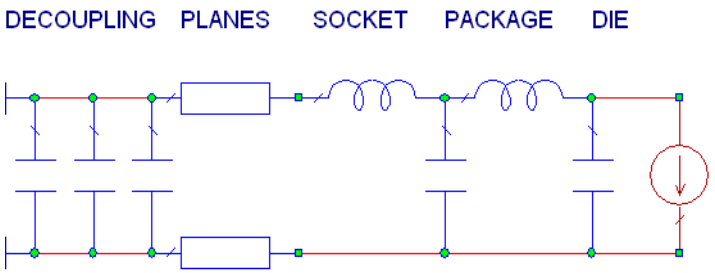
Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	5	V
Power Control Voltage (V_{REG})	3.3	V
DC Supply Current	500	mA
Input RF Power	+5	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	MSL2	

Impedance Derivation Method

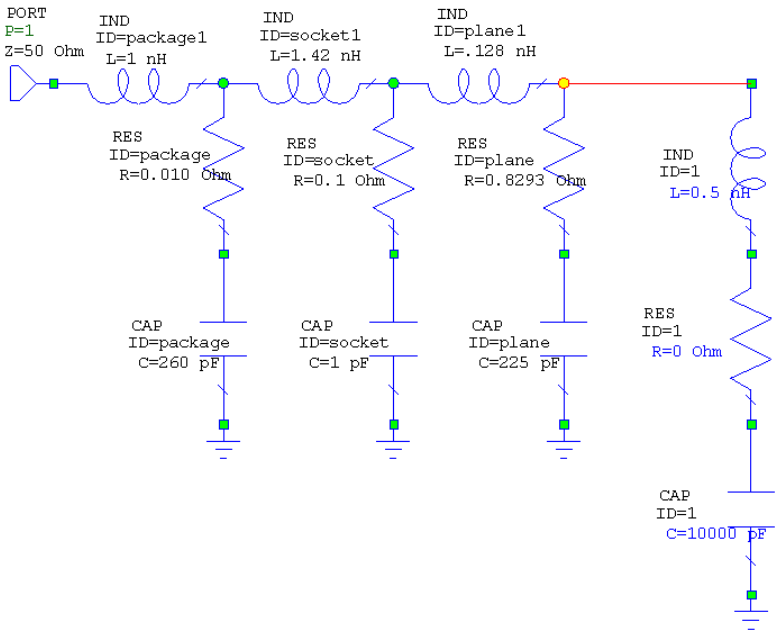
- Decoupling capacitors
  - ~.5nH (14%), 0.01uF
- PCB inductance
  - Power plane ~ 128pH/sqin (3%) , .225nF/sqin
  - DUT Vias ~ 300pH (8%)
  - Capacitor vias ~ 338pH (9%)
- Socket
  - ~ 1.5nH/probe pair (40%), 1pF
- Package
  - ~1nH/lead pair (26%), 250pF

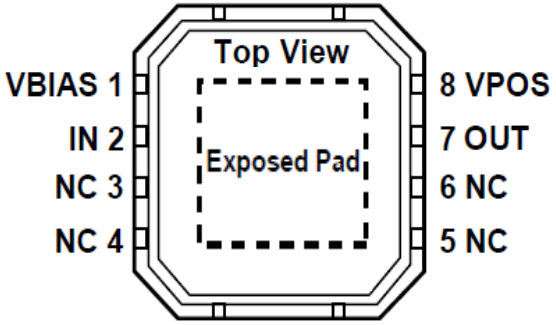
- Number of Caps
  - $N > 2\pi \times F_{MAX} \times (ESL/Z_{REQ})$
  - $N > 2*3.14*.3*(3.75/1) = 7$

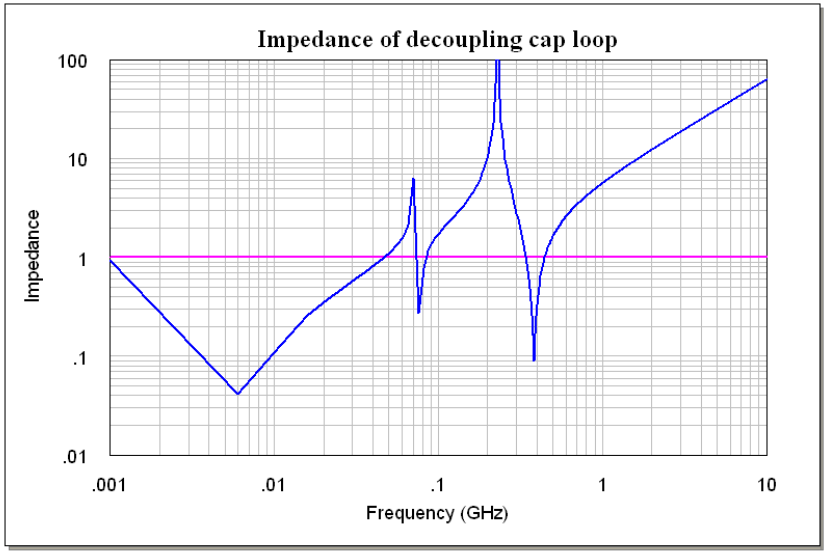


Impedance Profile of Decoupling Loop

- Original impedance profile
- QFN package with one power pin







How to Optimize the Impedance Profile

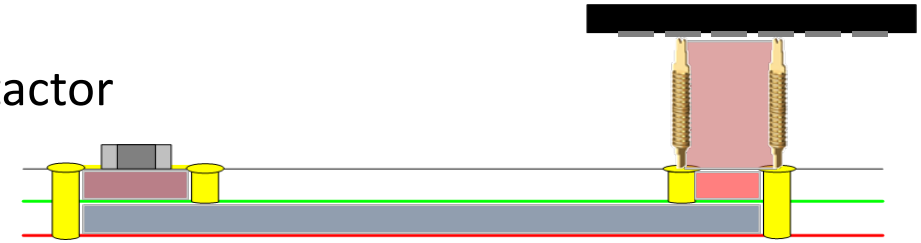
- Must consider physical limitations of semiconductor test environment

- Distance to Cap
- Contactor
- Number of capacitors

- Capacitor via location/quantity
- Via diameter
- Power plane layer

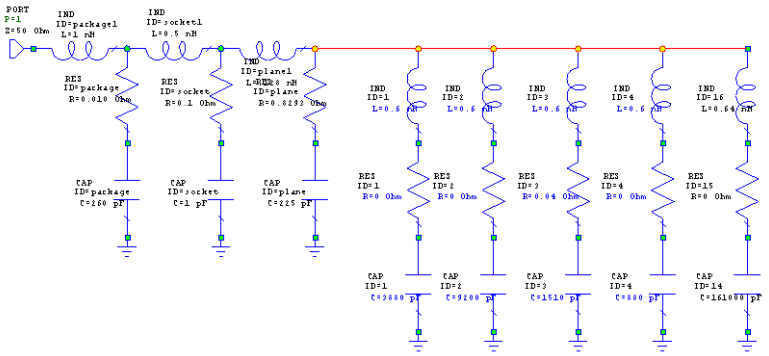
How to Optimize the Impedance Profile

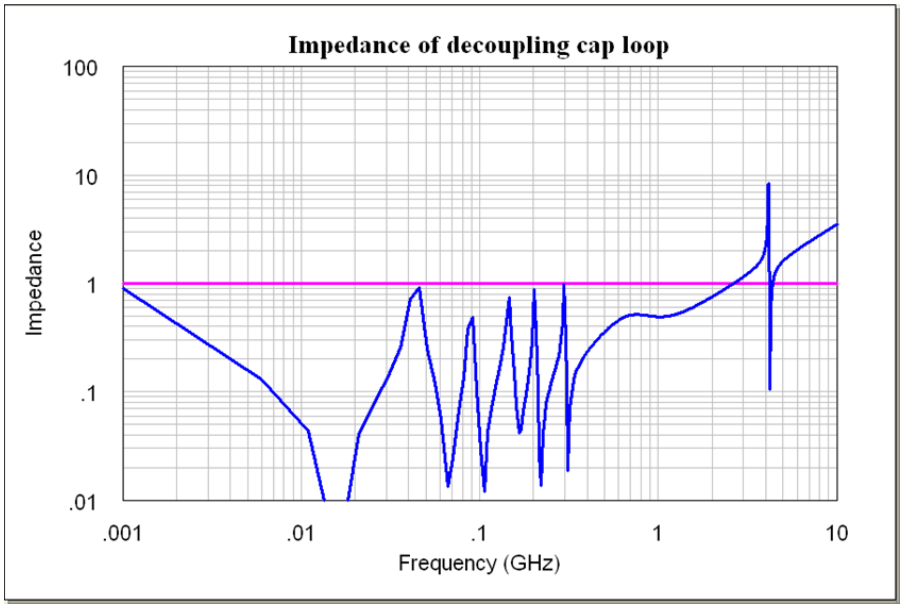
- Minimize loop inductance
  - Use short, low inductance contactor
  - Minimize area of current loops
    - Use low ESL capacitors
    - Place power/ground vias as close to each other as possible
    - Place bypass capacitors as close to DUT as possible
  - Maximize width of conductors
    - Wide traces, wide planes
  - Minimize spacing between ground and power planes
  - Use multiple parallel paths, pairs of vias, pairs of planes
  - Alternate polarity of capacitors



Optimized Impedance Profile

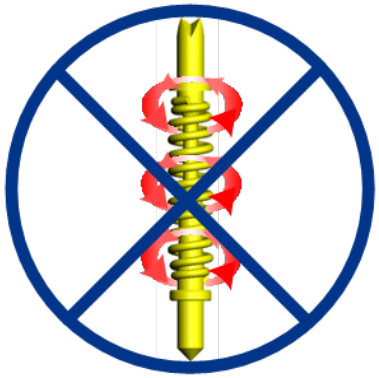
- Modifications
  - Added capacitors
  - Used low inductance contactor

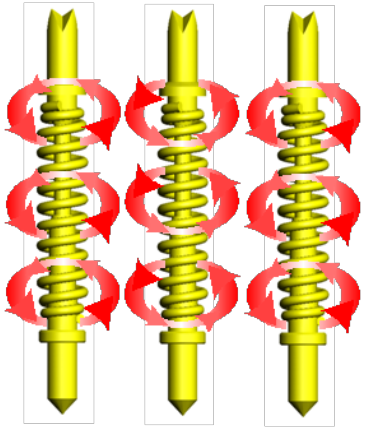




Optimizing the Contactor

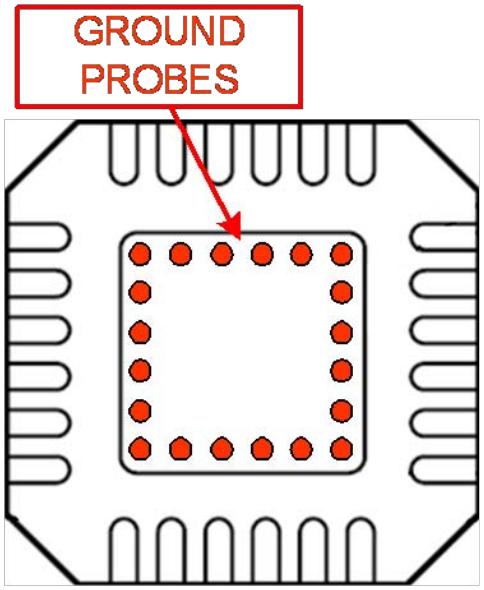
- Contactor impact on the PDN
  - Lifts device from ground plane of PCB
  - Adds inductance to decoupling loop
- Actual contactor inductance values
  - Always use loop inductance, not self inductance
  - Changes with pitch of device, length/width of probe, ground locations
- Reducing contactor inductance
  - Optimize package I/O configuration
  - Use short, fat probes
  - Use coaxial sockets if possible

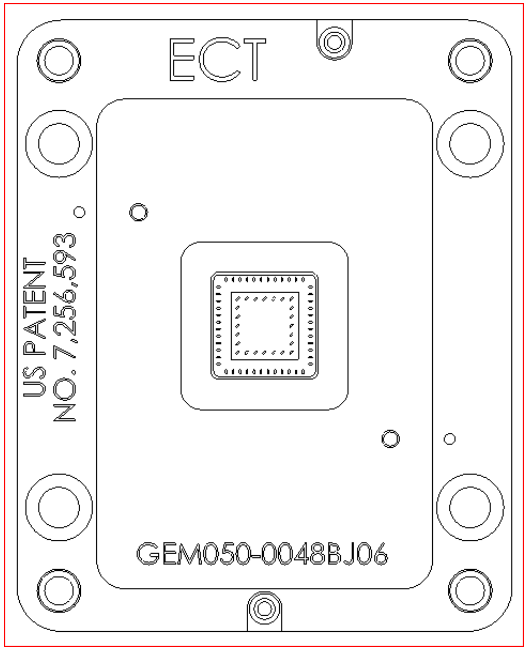




Optimizing the Contactor

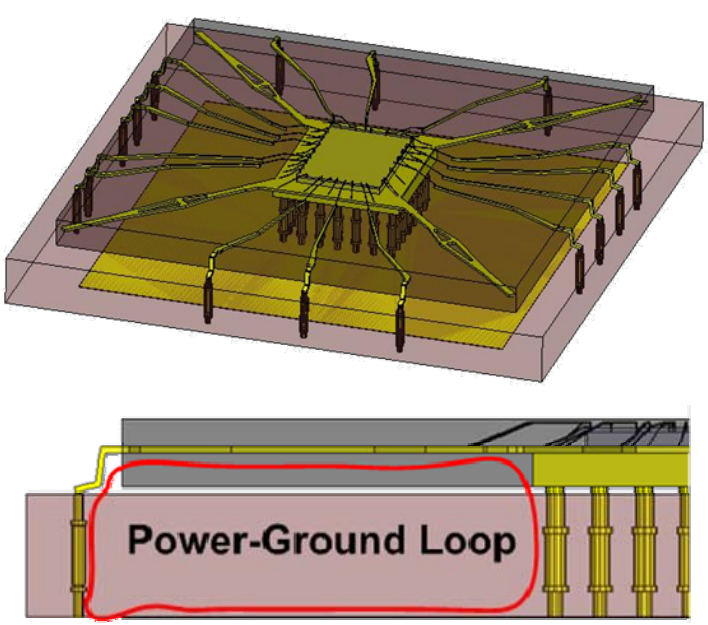
- Reducing contactor inductance (continued…)
  - Place ground pins close to signal pins, on perimeter of ground pad
  - Excessive ground probes in center of ground array will provide little or no benefit to lower loop inductance while adding cost

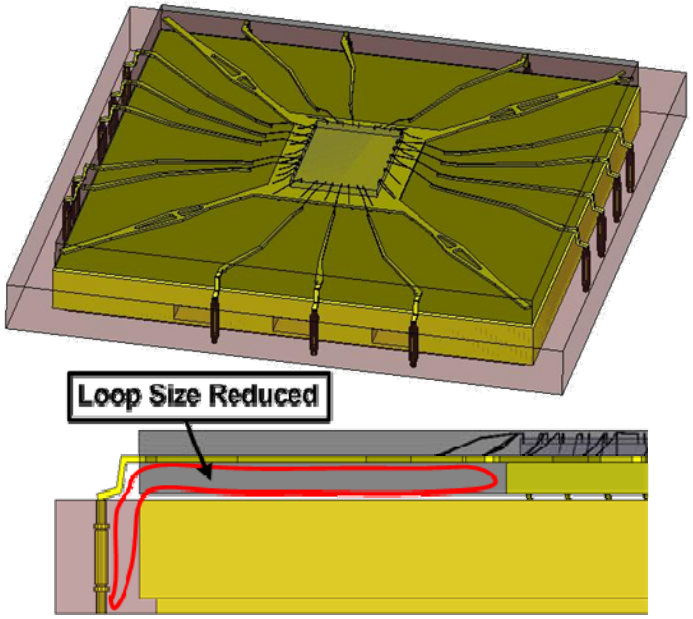




Optimizing the Contactor

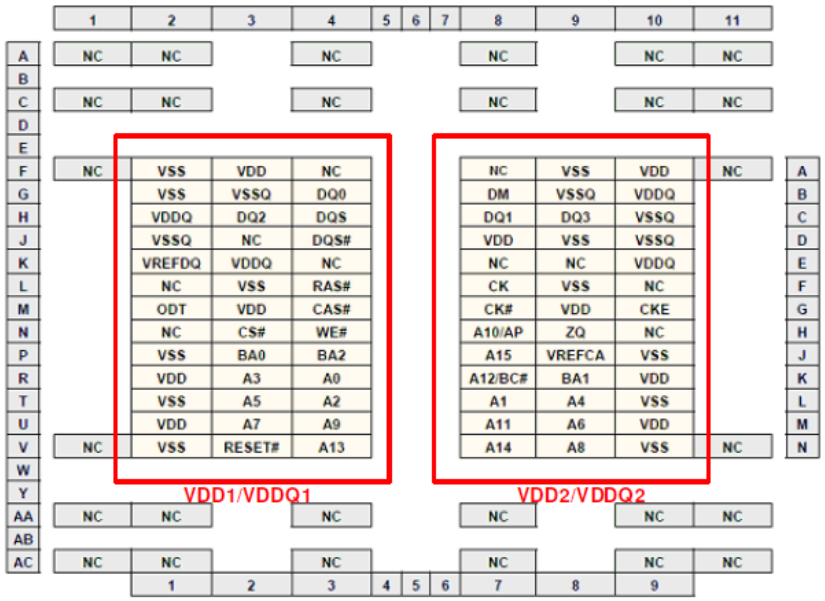
- Reducing contactor inductance (continued…)
  - Use ground slug
    - Signal will couple to nearest conductor
    - Ground slug brings conductor close to lead
    - Improves performance through contactor
    - May also improve performance through device

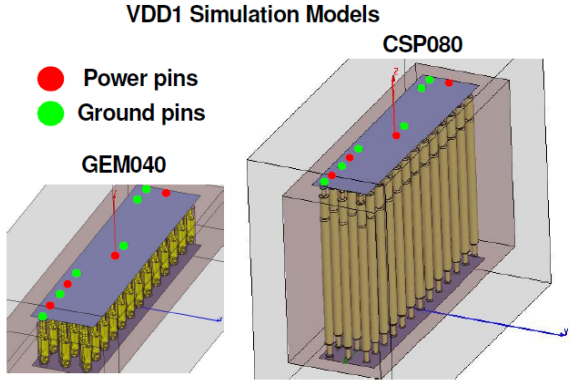


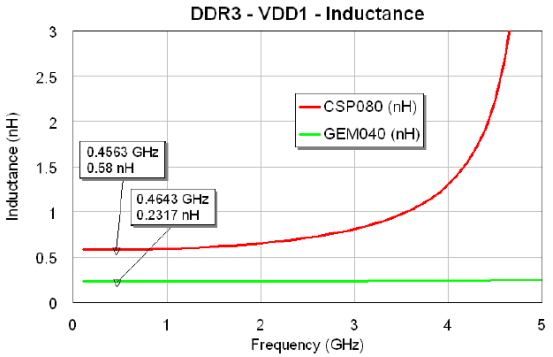


Example: Contactor Inductance

- Impedance environment using different contactor solutions
- Comparing contactor inductance in a BGA



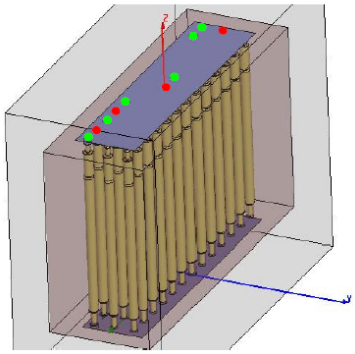


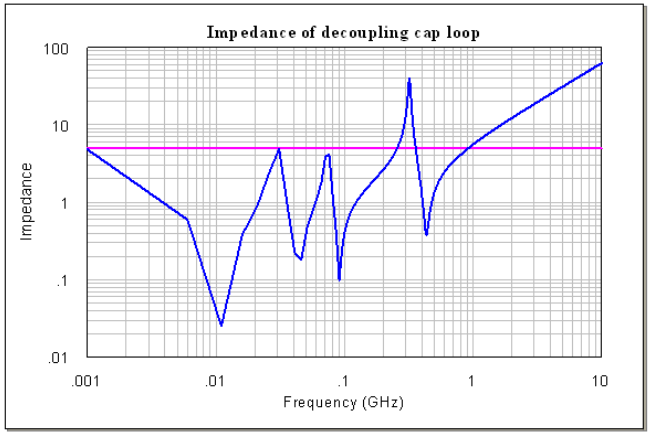


Example: Contactor Inductance

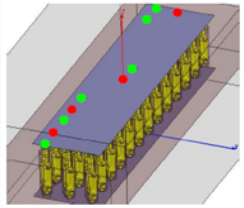
- Voltage
  - 1.5V
- Max Frequency
  - 1066MHz
- Max current
  - 400mA
- Impedance required
  - 5Ω

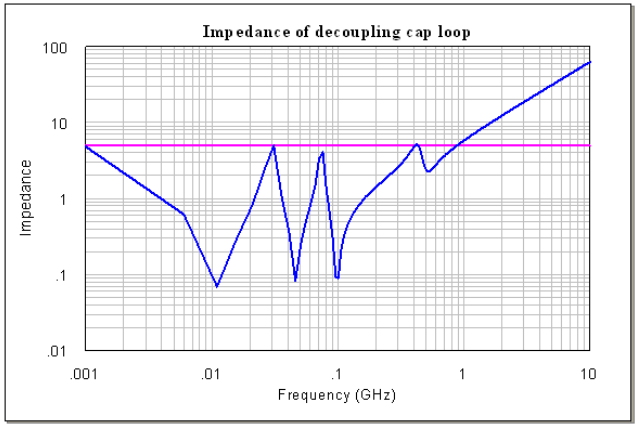
CSP080





GEM040





Conclusions

- Power Delivery Network Design is complicated
- Devices have unique impedance profile requirements
- Most difficult tasks are to define target impedance and model PDN accurately
- Vias, PCB, contactor, package all play a role in the PDN
- Understanding how each component impacts the overall performance of the PDN is required to design a quality system
- With a lot of manual work or high power simulation tools you can save cost by designing your PDN to match the device requirements