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De-embedding and Modeling Device-to-Tester Printed Circuit Board Interface Assemblies

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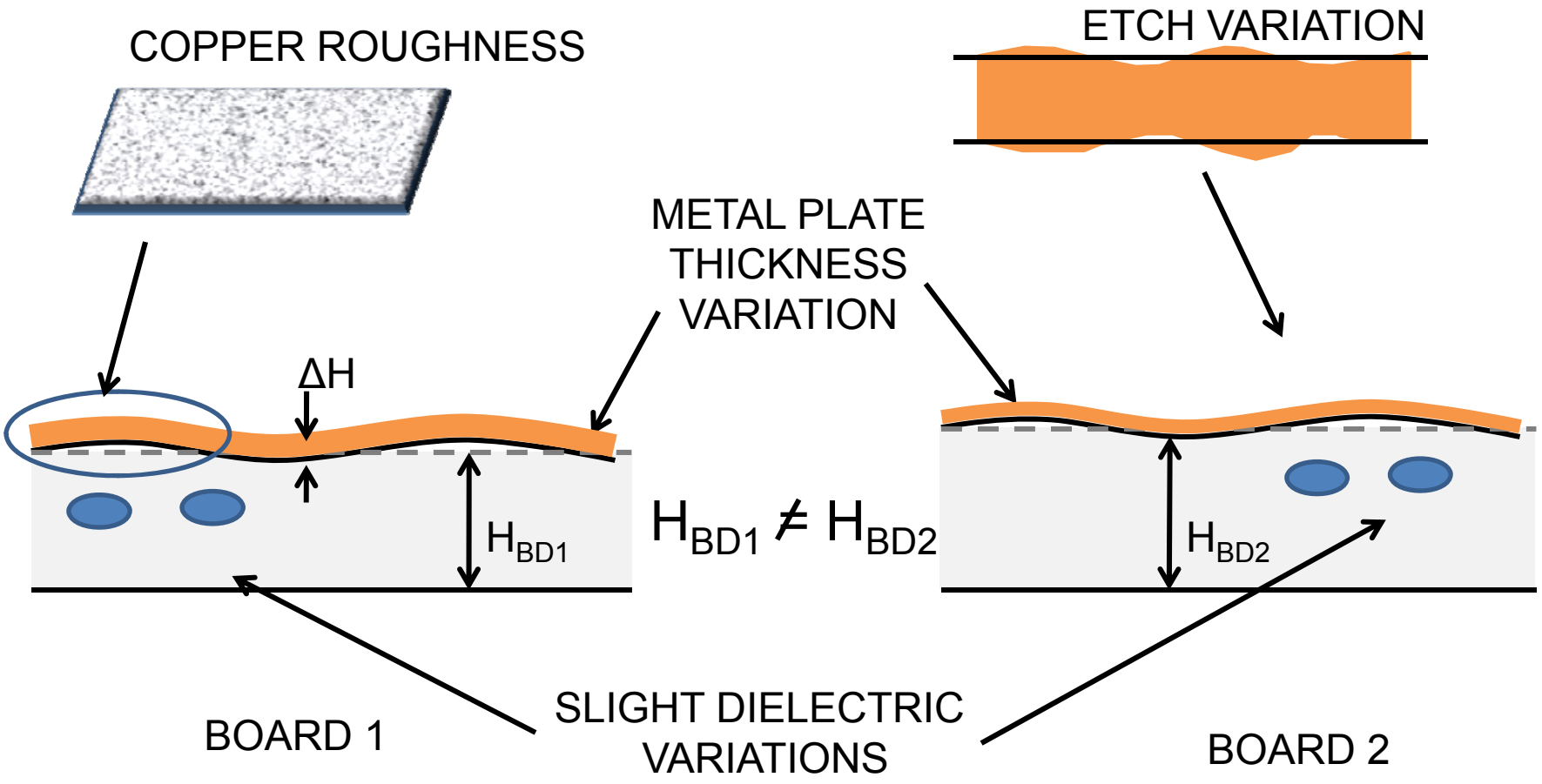
De-embedding Printed Circuit Boards - Purpose and Outline

De-embedding Printed Circuit Boards
1 – Practical Loss Issues



De-embedding Printed Circuit Boards
1 – Practical Loss Issues

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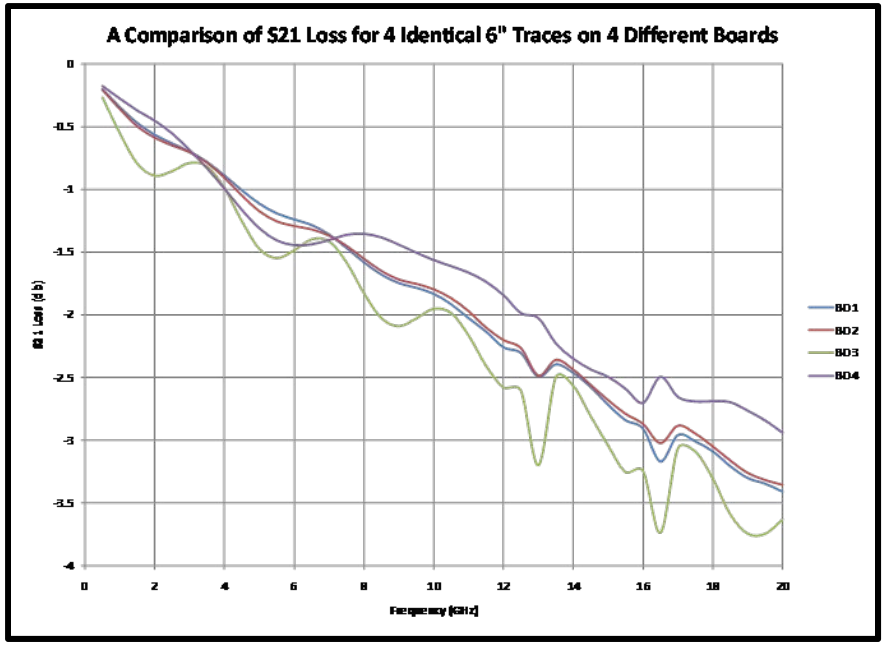
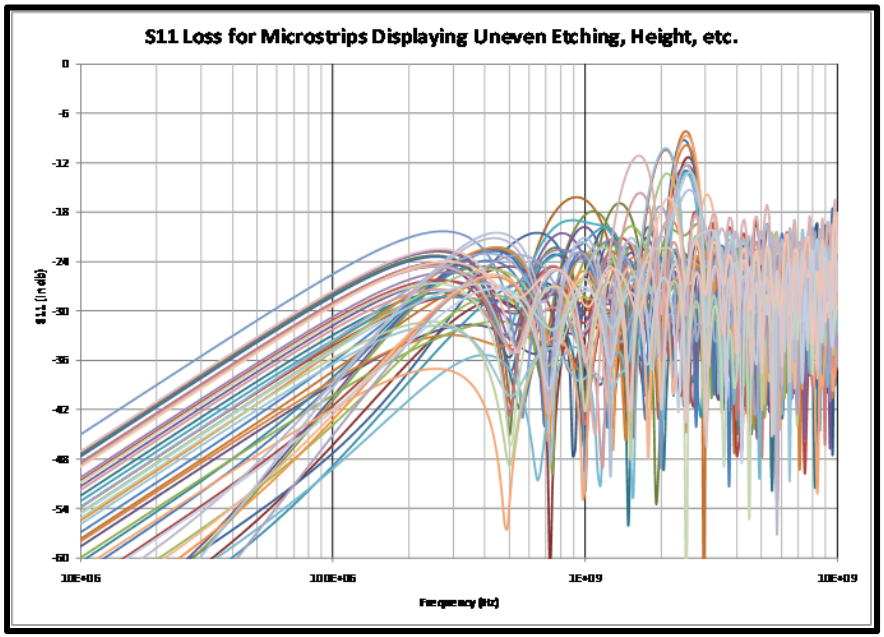
S21 loss over 4 boards



S11 loss over 30 boards



Even with dsp-based equalization in a BERT for ideal losses,
Differences will occur between boards.

De-embedding Printed Circuit Boards
2 – De-embedding Concept and Issues

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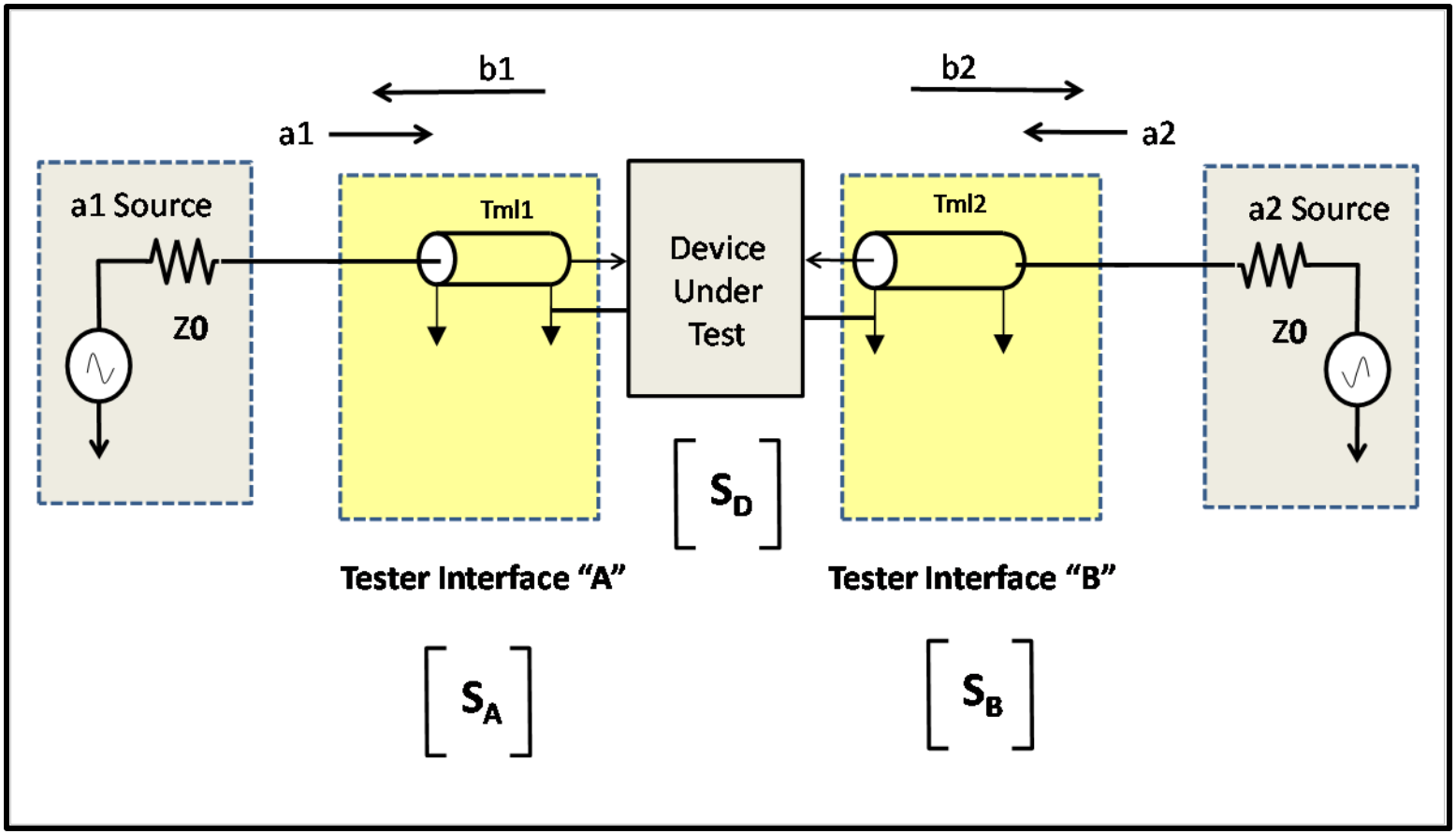

De-embedding Printed Circuit Boards
2 – De-embedding Concept and Issues

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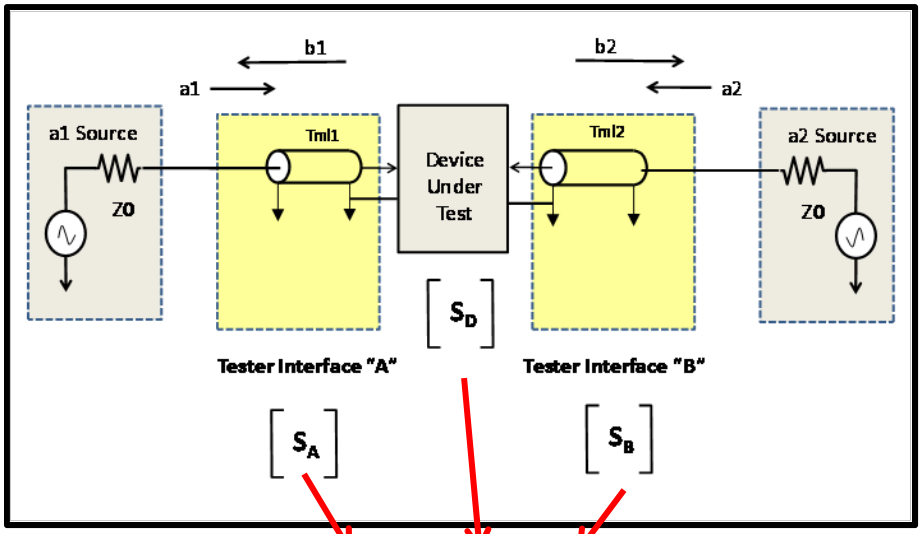
$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

$$\begin{bmatrix} T_T \end{bmatrix} \leftrightarrow \begin{bmatrix} S_T \end{bmatrix}$$

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} t_{11} & t_{12} \\ t_{21} & t_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}$$



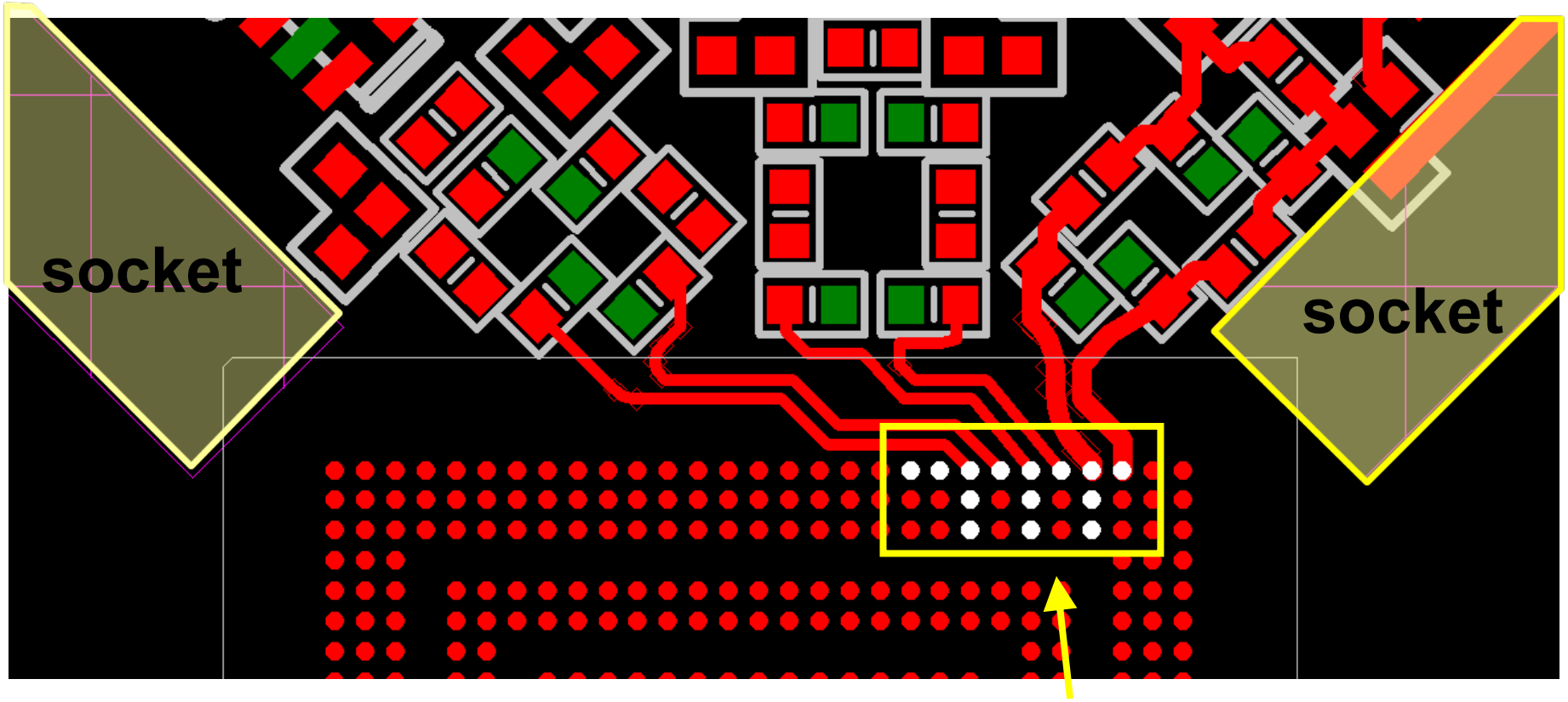
$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_A \end{bmatrix} \begin{bmatrix} T_D \end{bmatrix} \begin{bmatrix} T_B \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix}$$

$$\begin{bmatrix} T_A \end{bmatrix}^{-1} \begin{bmatrix} T_T \end{bmatrix} \begin{bmatrix} T_B \end{bmatrix}^{-1} = \begin{bmatrix} T_D \end{bmatrix}$$

$$\begin{bmatrix} T_D \end{bmatrix} \leftrightarrow \begin{bmatrix} S_D \end{bmatrix}$$

All vector network analyzers work on this principle to calibrate cable connections.

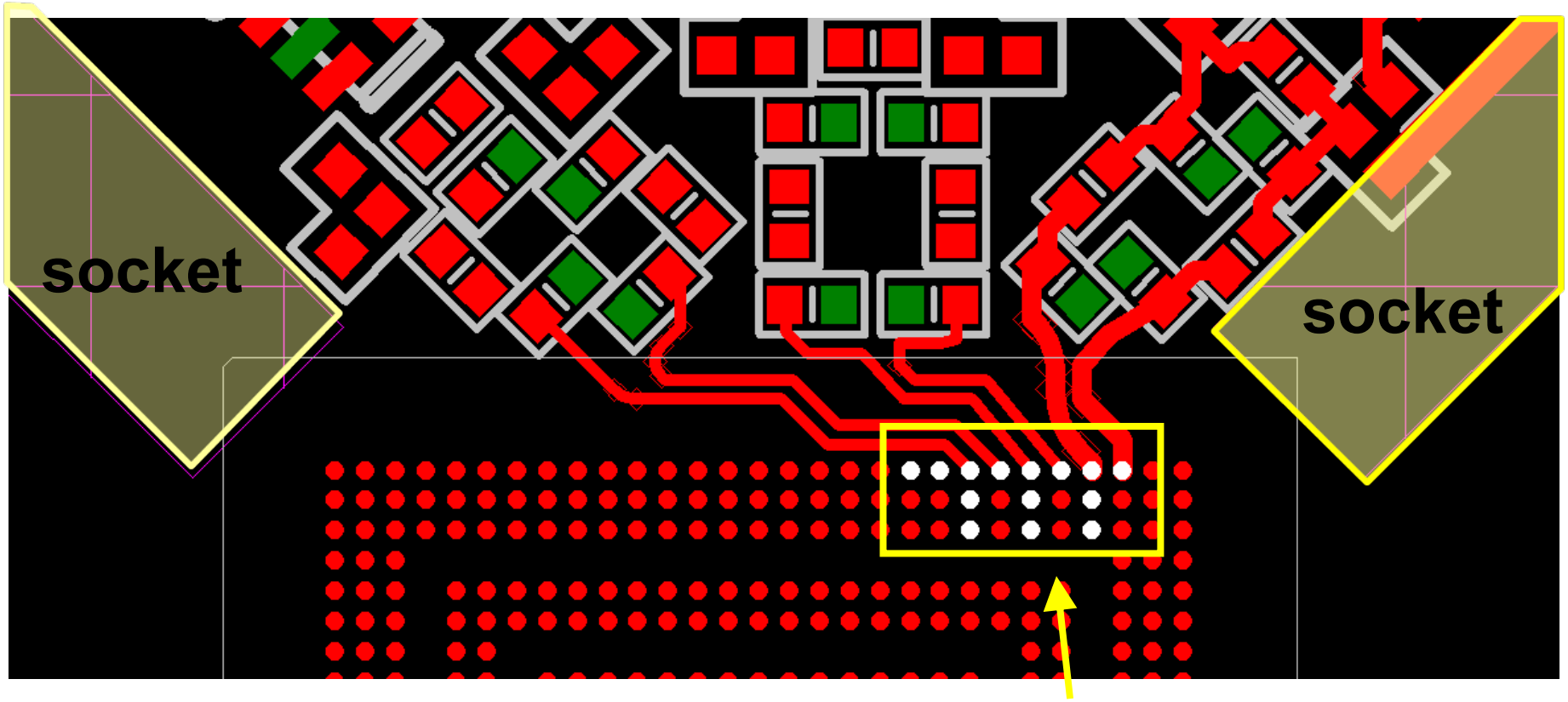
De-embedding Printed Circuit Boards
2 – De-embedding Concept and Issues



How do you accurately probe
so many points here?

De-embedding Printed Circuit Boards
3 – Surrogate Traces De-embedding

De-embedding Printed Circuit Boards
2 – De-embedding Concept and Issues



How do you accurately probe
so many points here?

De-embedding Printed Circuit Boards
3 – Surrogate Traces De-embedding

Layout can Never be identical.

Made for Test Access

De-embedding Printed Circuit Boards
3 – Surrogate Traces De-embedding

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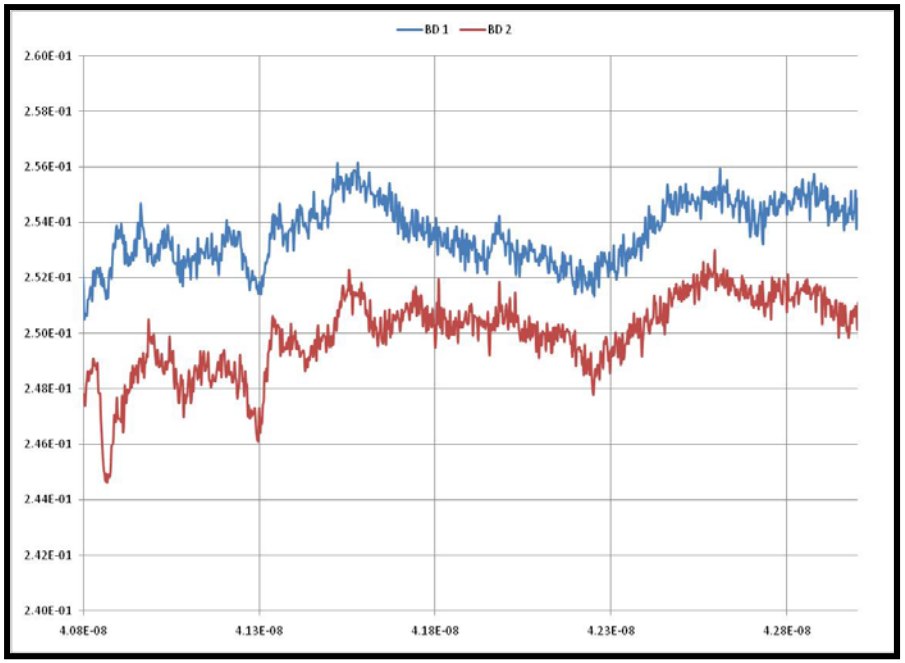
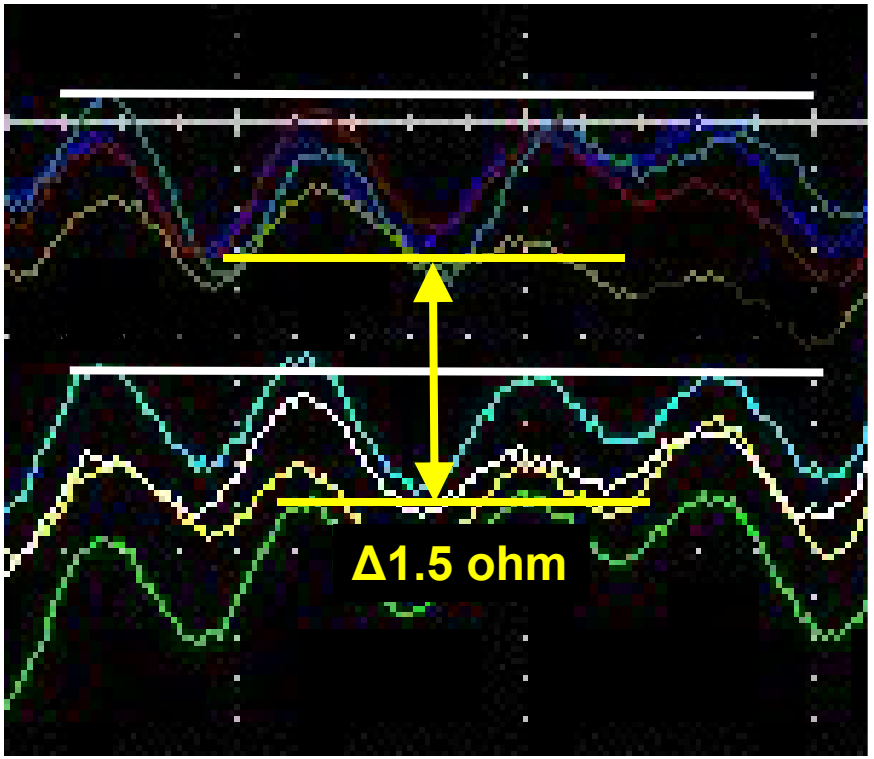
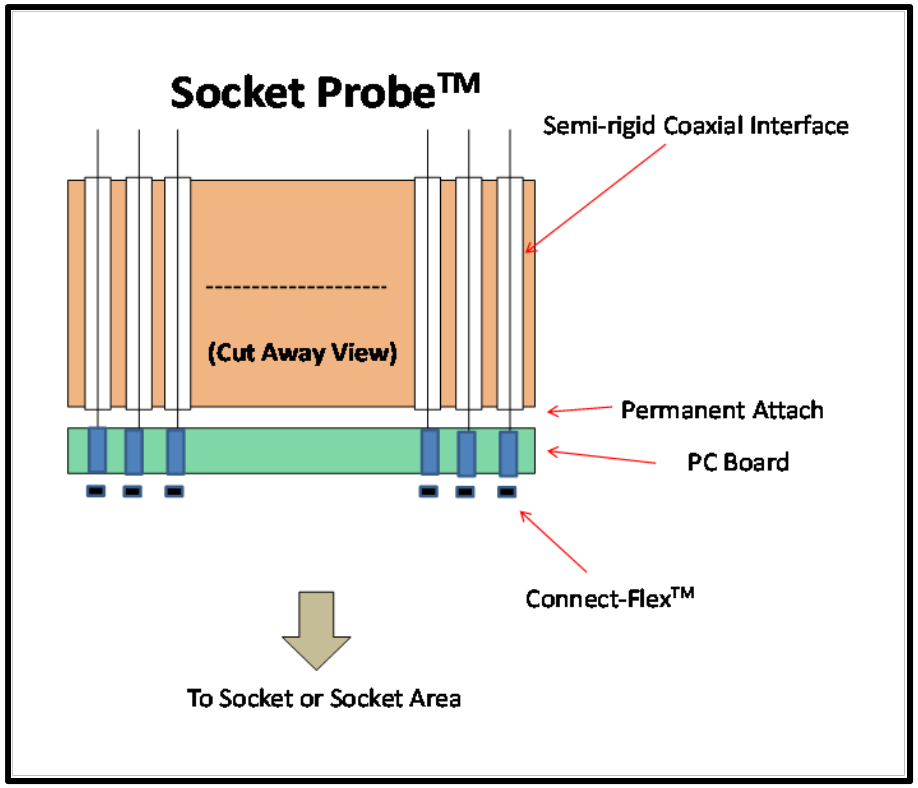


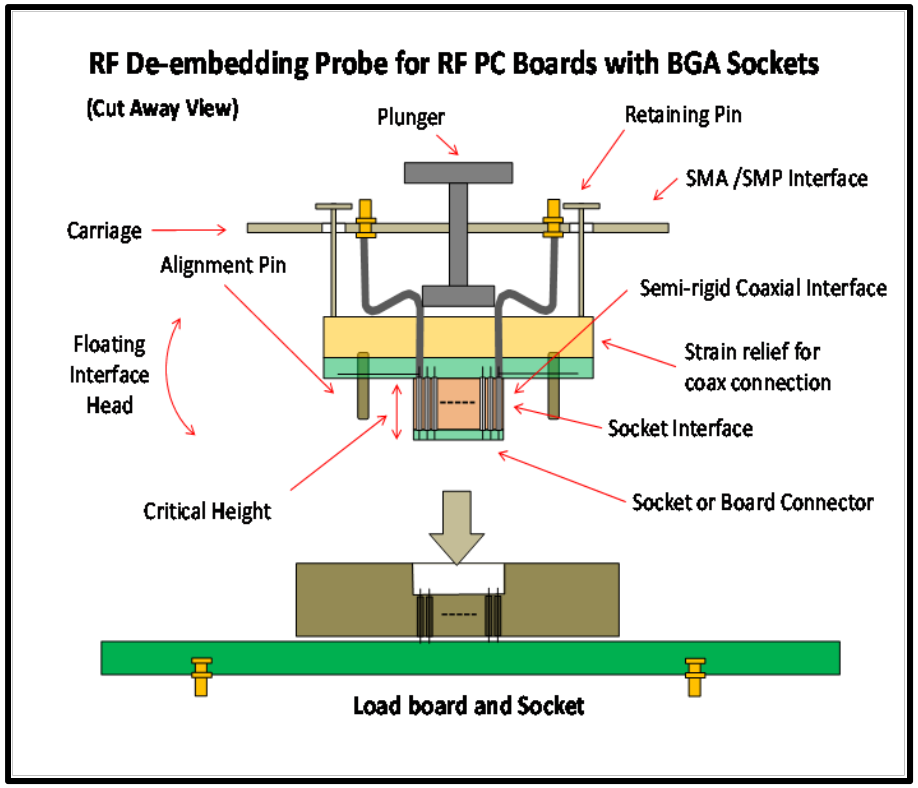
Board to Board
Surrogate Traces Help



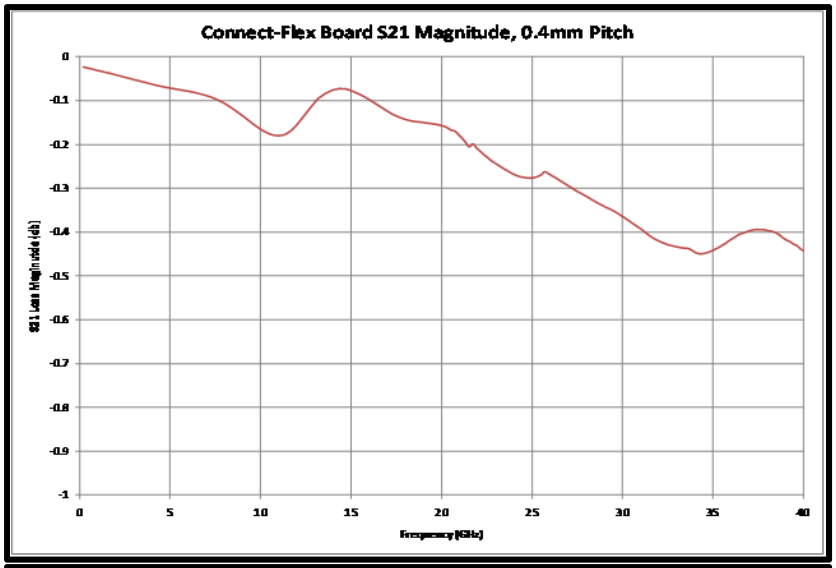
Within Board
Surrogate Traces fall Short

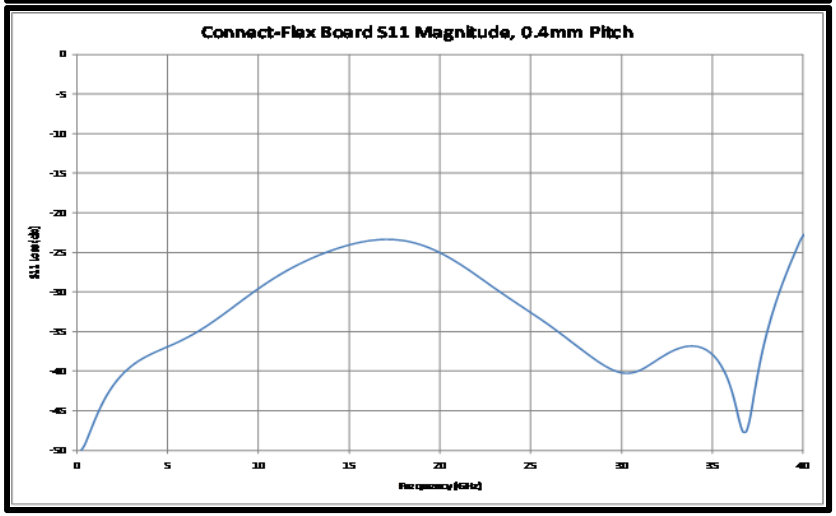
De-embedding Printed Circuit Boards
4 – Full De-embedding: Socket Probe™

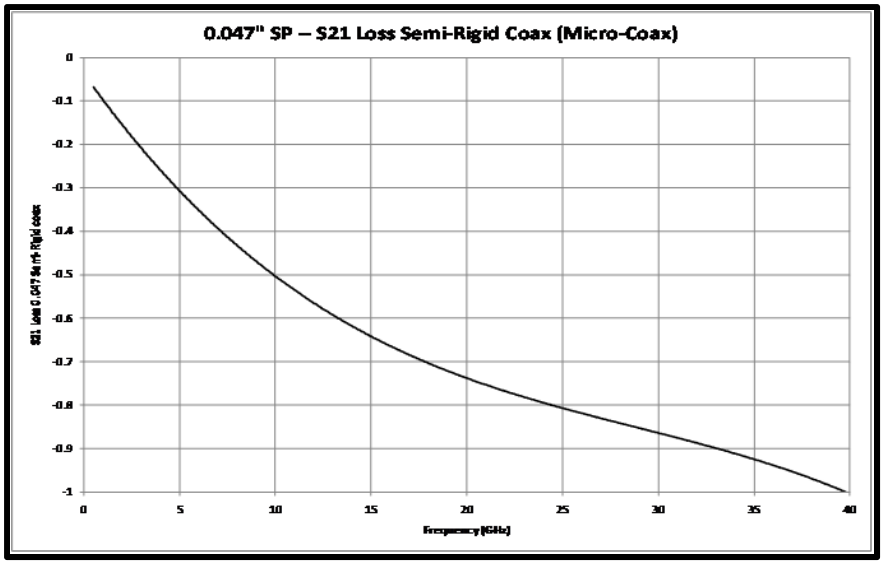




De-embedding Printed Circuit Boards
4 – Full De-embedding: Socket Probe™

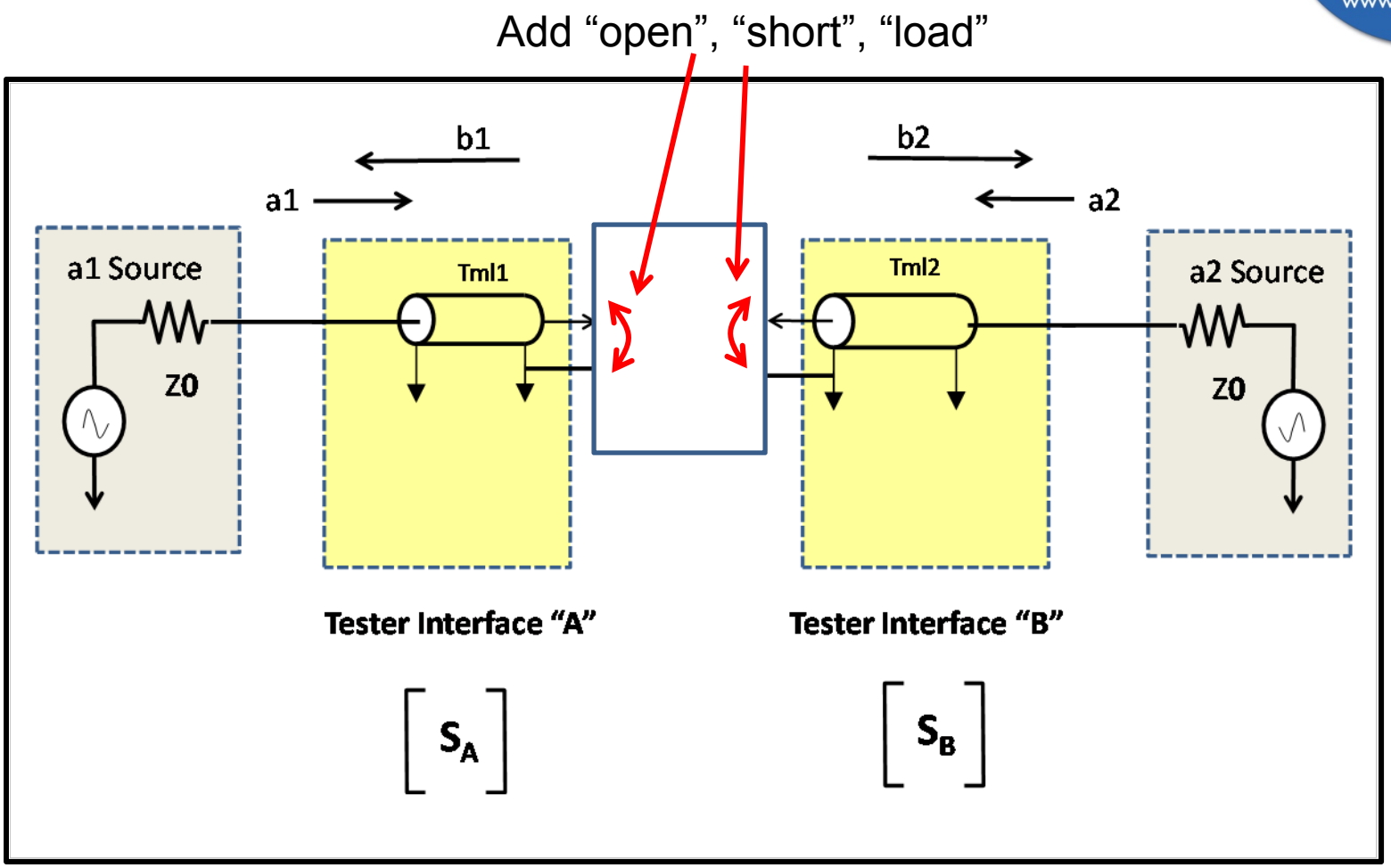






Total Losses <1.5db @ 40GHz!

De-embedding Printed Circuit Boards
4 – Full De-embedding: OSL



De-embedding Printed Circuit Boards
4 – Full De-embedding: OSL

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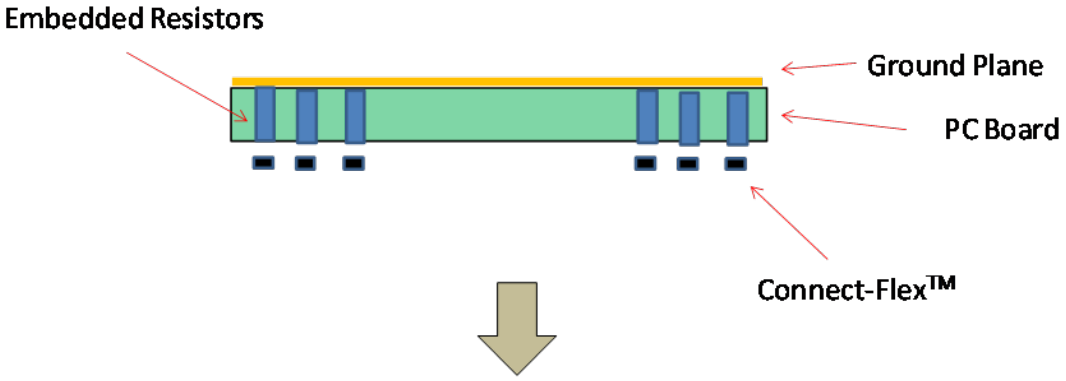
OSL Miniature Standards
(LOAD Standard Shown)



De-embedding Printed Circuit Boards
5 – Conclusions

1. Current process and Fabrication Issues result in high variability in losses between traces on a board and between boards.

2. De-embedding must be done on every board to fully compensate for these losses. However, traditional methods are painful and error-prone.

3. Surrogate de-embedding helps but is not good enough for precision measurements.

4. New technologies using a Socket Probe™ or OSL inserts with embedded components allow a test engineer the ability to cost effectively and accurately debug each trace.