Integrating Tester and Semi-Custom Interconnect Solutions for Multi-Port SERDES IO Characterization up to 16 Gb/s

Ron Lesnikoski
Principle Hardware Engineer
Oracle Systems

Introduction

- Design and manufacture of semi-custom, highly integrated interconnect systems that address the complex issues of characterizing device IO performance at bit rates exceeding 16 Gb/s.
- Design Focus on Signal Integrity, Reliability, Modularity, Scalability, Minimal Setup Time
- Find a way to deliver the signal accurately and under the proper test channel conditions

The Problem

- Characterizing a super scale SOC devices with multiple high speed serial ports for functionality and performance
- Big Issues
  - Signal Integrity and Bandwidth
  - Test Methodologies and Instrumentation
    - Constantly Evolving; Support DFT
  - Scalability to 100's of lanes
  - Cost
  - Power, Cooling, Test Cell Investment

Our Approach

- IO Connector Density Drives Scalability to Achieve Maximum Test Coverage
- Maintain Investment in existing Test Cell Infrastructure, Use low cost test platforms
- Adapt Connectors to Scale To device IO Test List
- Use Lower Cost Modules that build on Existing DUT board hardware
- Reuse ! Commercial Connectors are Limited

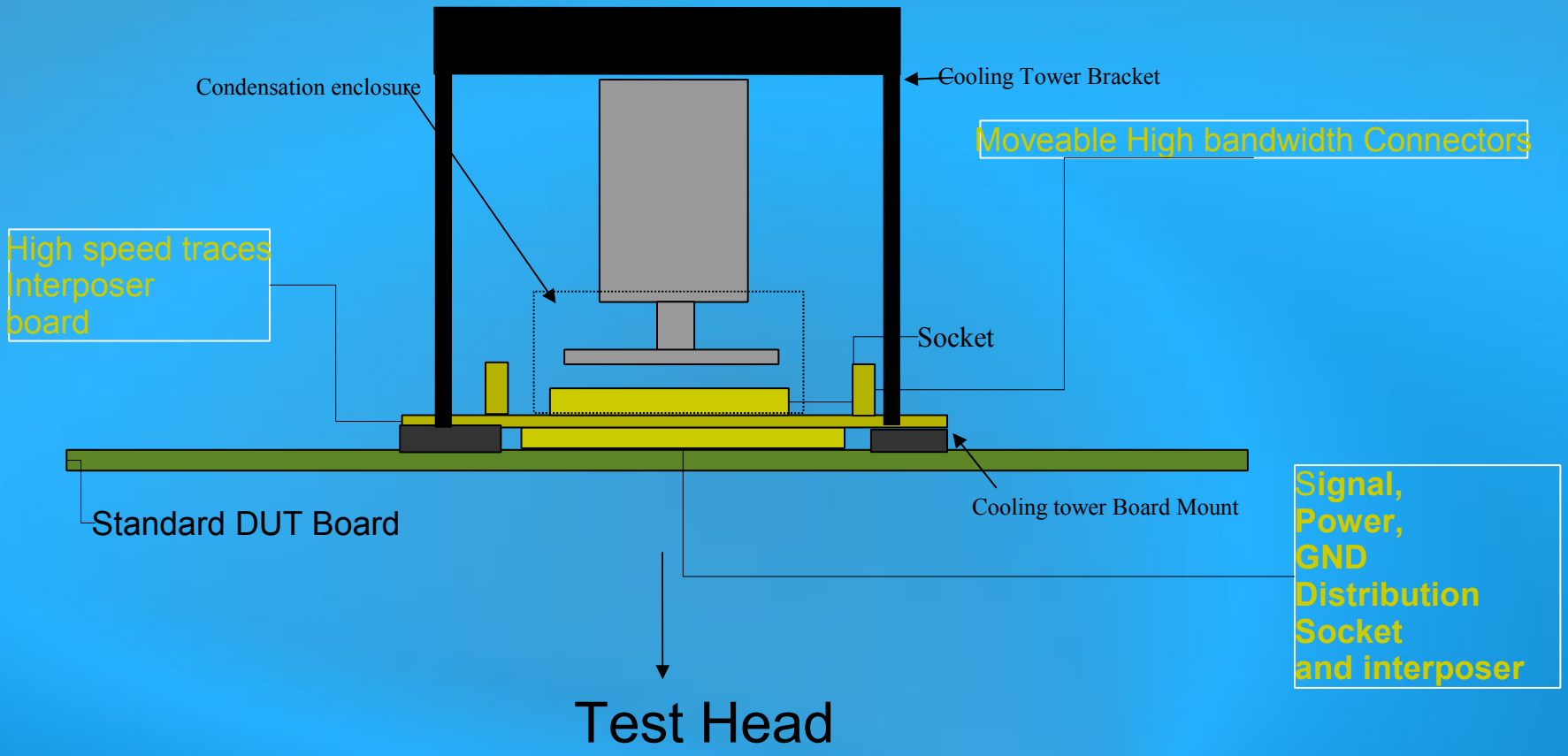
Example Application

- Last Generation Large Network uProcessor
- > 200 Lanes, multiple protocols, ranging from 2.5 Gb/s to 9.6 Gb/s
- Goal - Characterize IO performance at the Chip Level through 9.6 Gb/s (Jitter, BER, IO Functionality, Sensitivity)
- Provide Functional Debug Capability for PHY and Logic Layer

Challenges

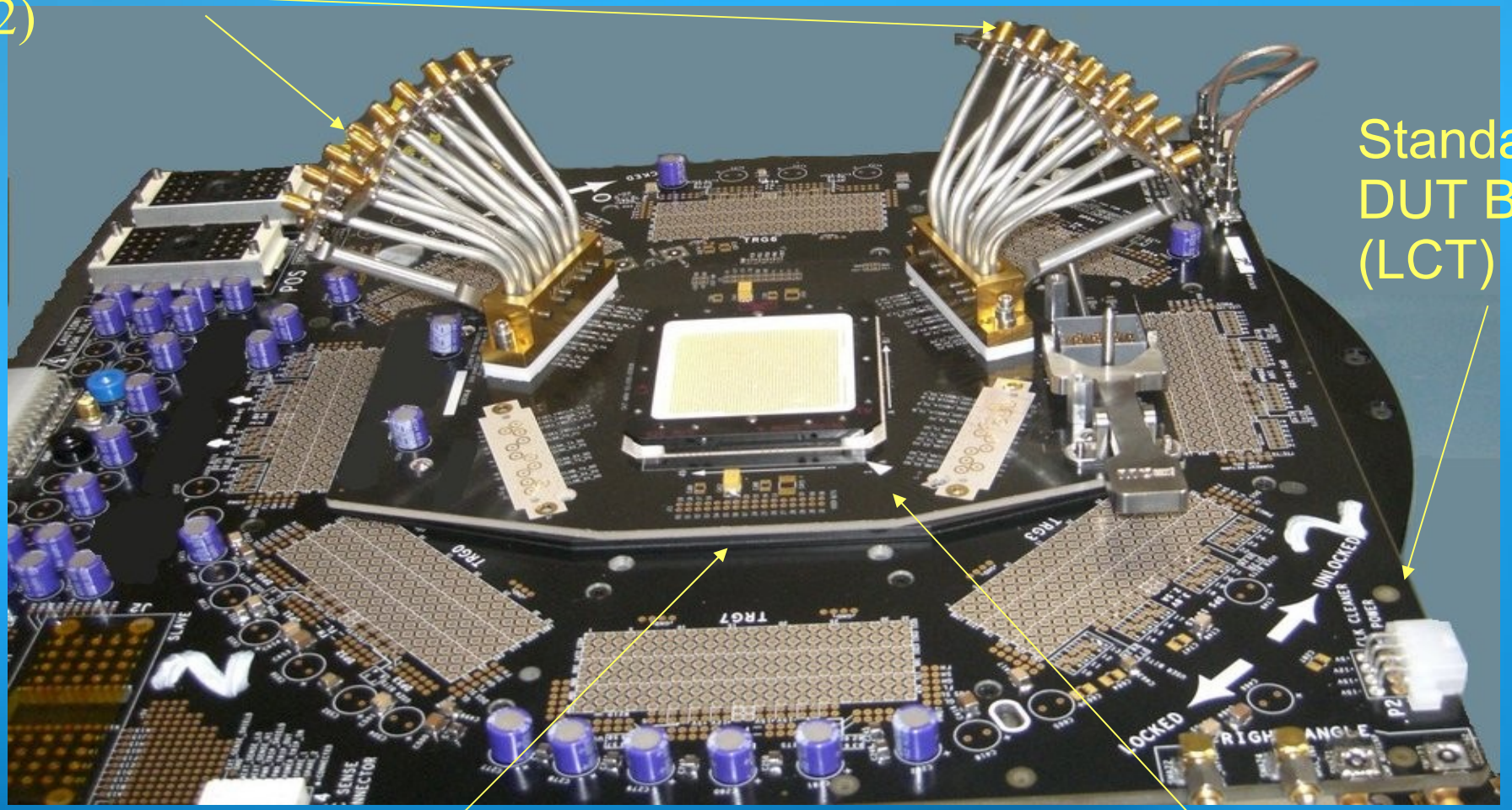
- Device Cooling Hardware – Limited Board area for interconnects. Device IO and Core Power management
- Signal Integrity-Distance to DUT, low insertion loss
- Power Integrity- Lots of decoupling close to DUT
- Test Cell Operation
  - Not a Bench Environment!
  - Must be Rugged, Reliable and Easy to Repair

Solution Block Diagram



- Supplied by XpandATE Technologies LLC

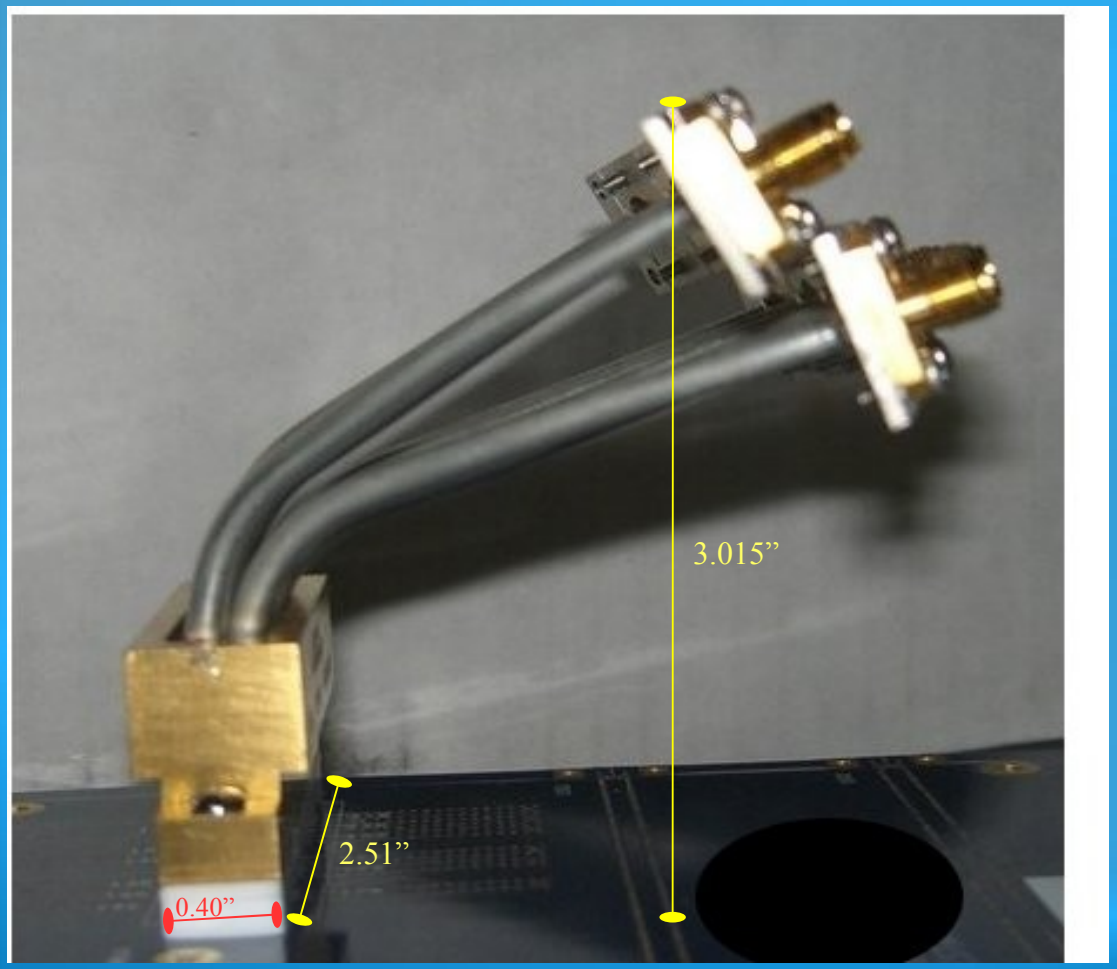
System Description



Connector Description

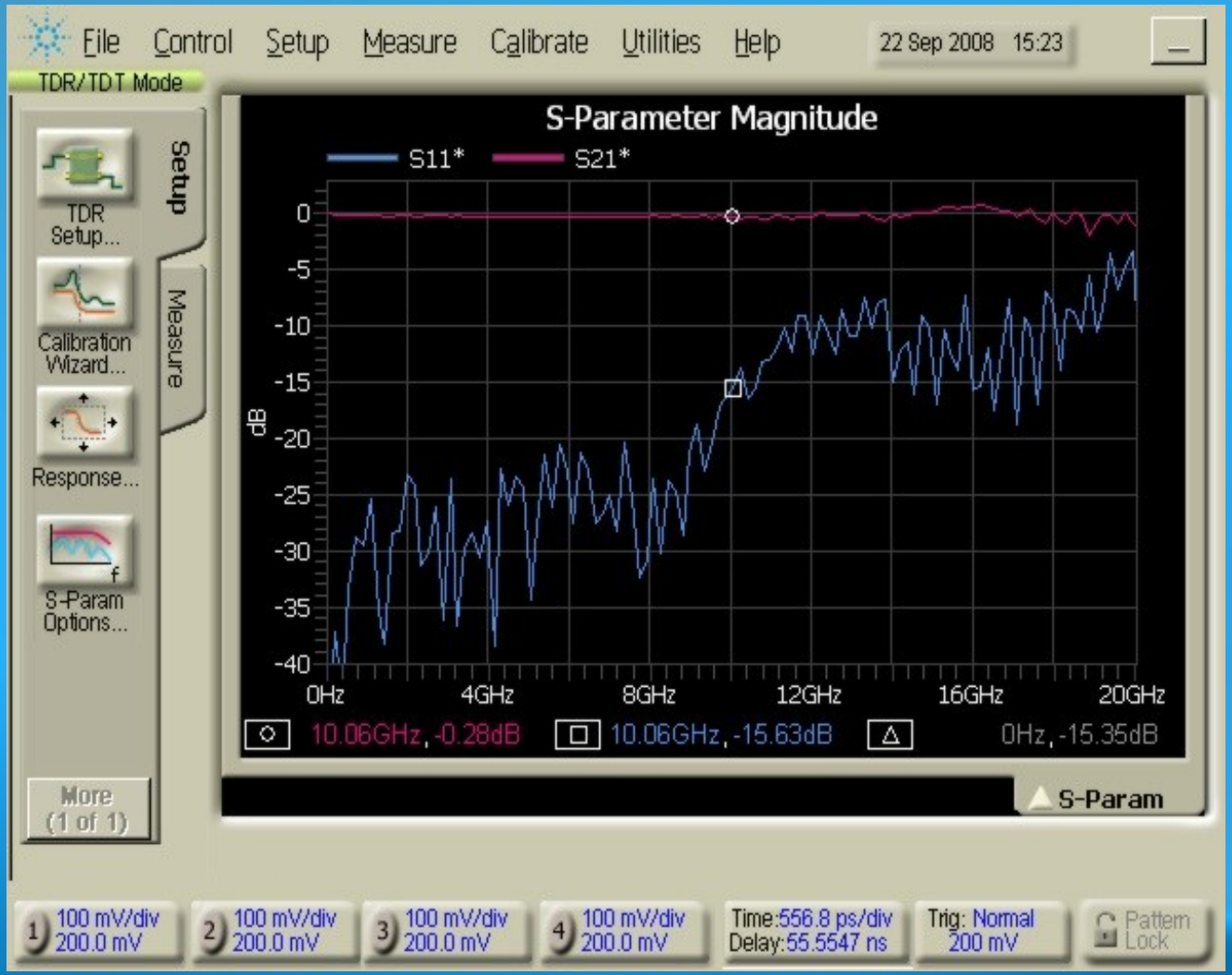
- 12 Channel,16 GB/s operation. Channel to channel skew less than 3ps across connector
- 12 channels consume 1.02 in^2 of board area
- Designed for top mounted board connection. Easy to place close to DUT. Easy to move during operation.
- Angled to ease cable bundle connection change-over
- Board connection interposer is designed for repair and retrofit in the field
- Board Launch designed to minimize connector to board insertion losses

Connector Design Details



1) Reduces total board/connector footprint
2) Reusable high reliability connector that mounts directly to the board
3) Board component costs are lowered since most SMAs can be eliminated
4) Connector design eases layout restrictions and reduces the board size by placing more signals close to the DUT
5) Promotes fast setup and changeovers in characterization test suite. Cables can be pre-loaded and inserted 12 at a time.
6) Adapt to cooling systems and tight configuration issues
7) Connector maneuverability; Top down mounting, Change hardware without removing DUT board from test platform.
8) Can be repaired in the field, uses modular construction to minimize down time

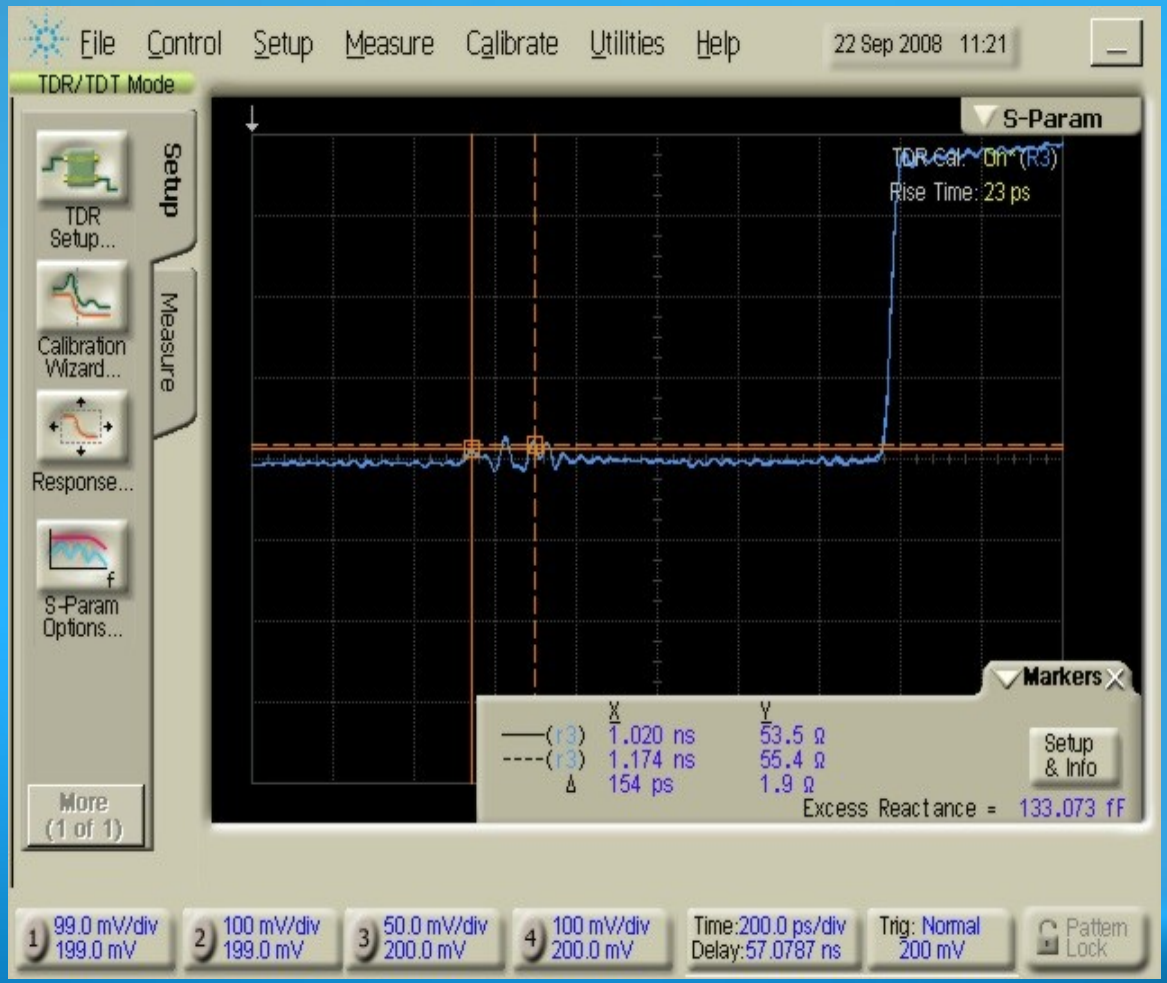
Connector/DUT Boards S-Parameters



Plot taken with channel 2 shorted to channel 3 through board launch strip line connection looped through DUT Socket

Connector S11 and S21 Plots

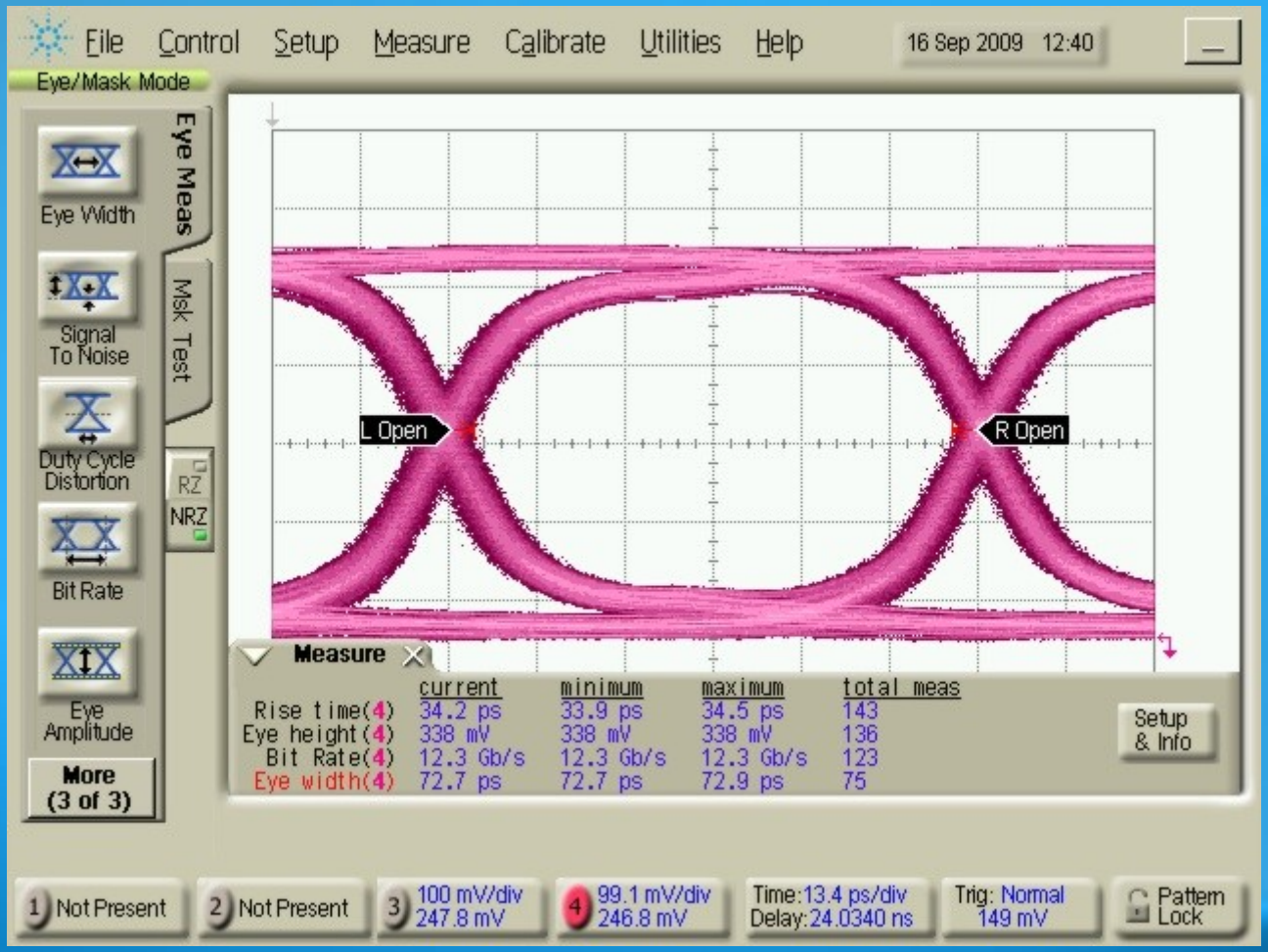
Connector TDR performance



Small Impedance shift at connector to board to connector vias and pins

53 to 55 ohms

Eye Pattern



Eye Measured in Socket

12 Gb/s 500mV Differential Signal

PRBS 2^7-1 pattern

through 5” board trace

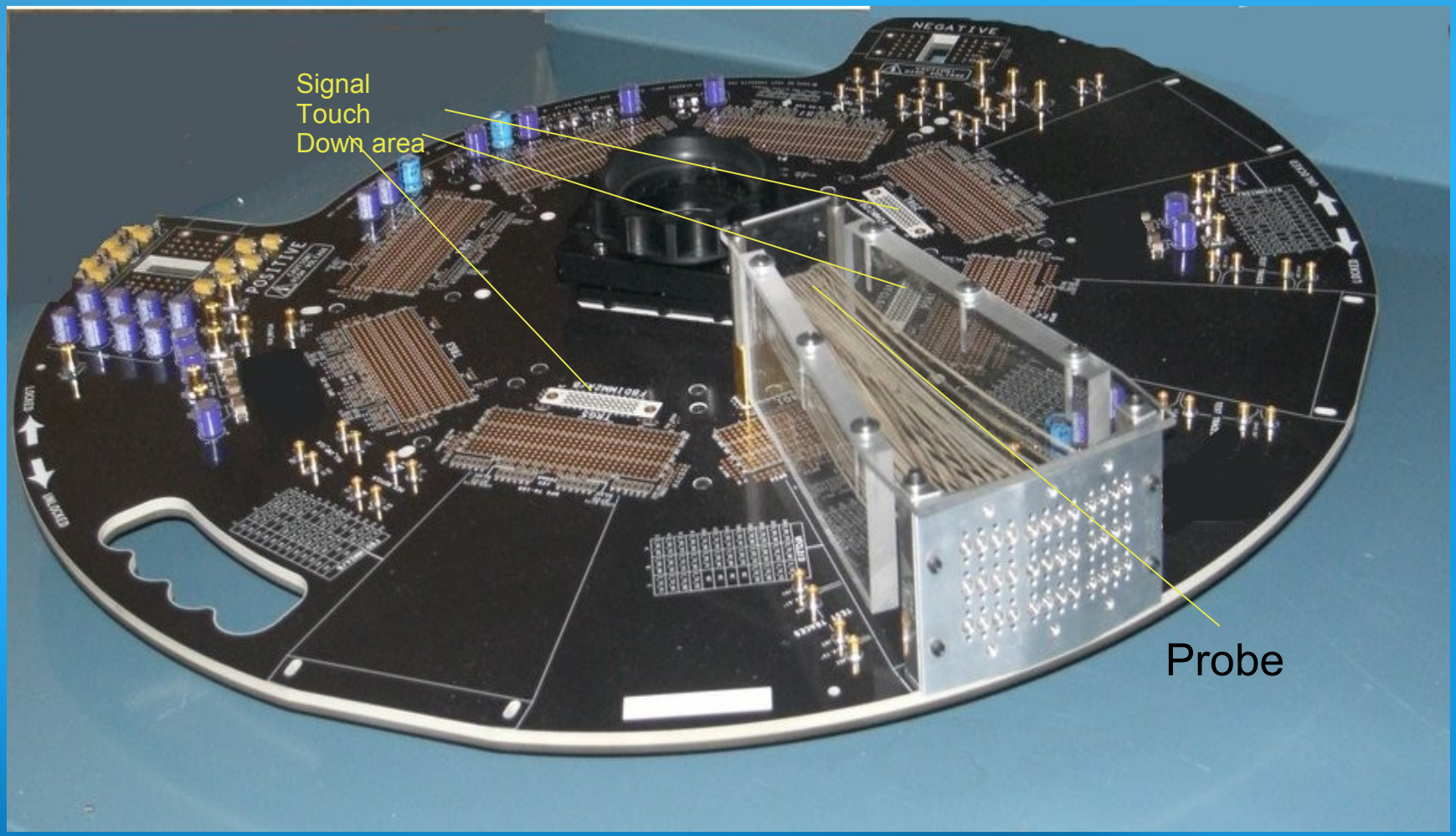
Higher Density Probe Solution

- For Slightly Lower Performance and less stringent mechanical constraints, we offer a much higher density probe/signal breakout solution
- 36 channels, 9 GHz Bandwidth, less than 3ps channel skew
- 36 channel touchdown consumes 0.72 $inch^2$ of board space
  - SMA equivalent = 18 in^2 SMP equivalent 2.72 $inch^2$

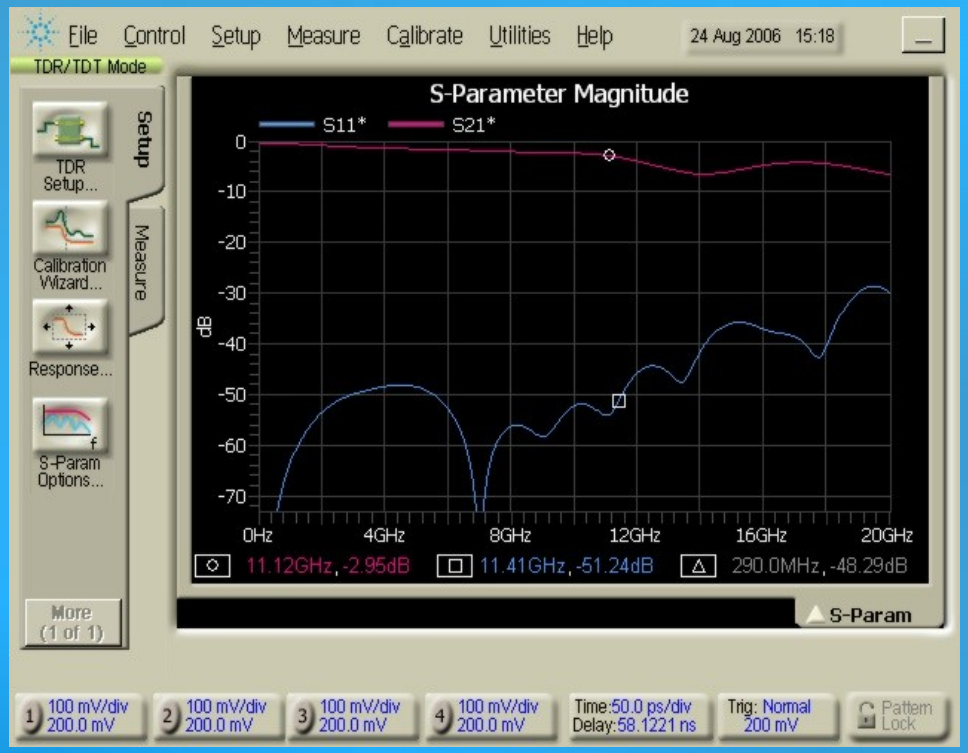
Addressing Higher Density

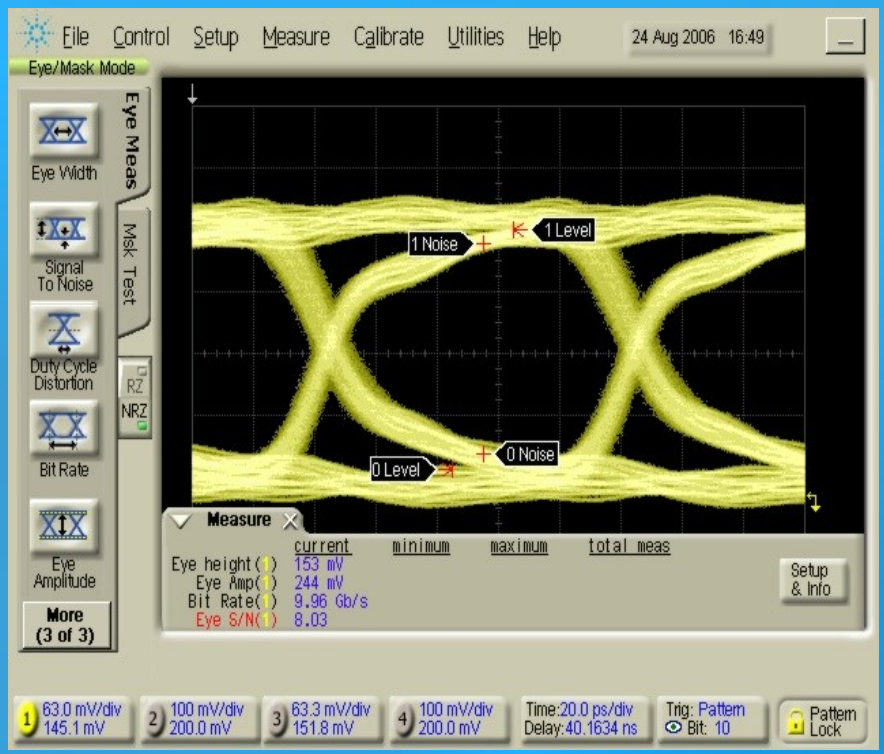
- Need for Higher Density Full Port Interconnect
- Used to P
- Analyze Block Read/Write, Protocol and Mission Mode Debug at the Chip Level
- Lower Bandwidth IO Characterization to 10 Gb/s

High Density Hyper-Probe



Hyper-Probe Performance





S21 S11 plot -3dB at
12 GHz

10 Gb/s PRBS 2^{31}-1
7 inch Rogers traces

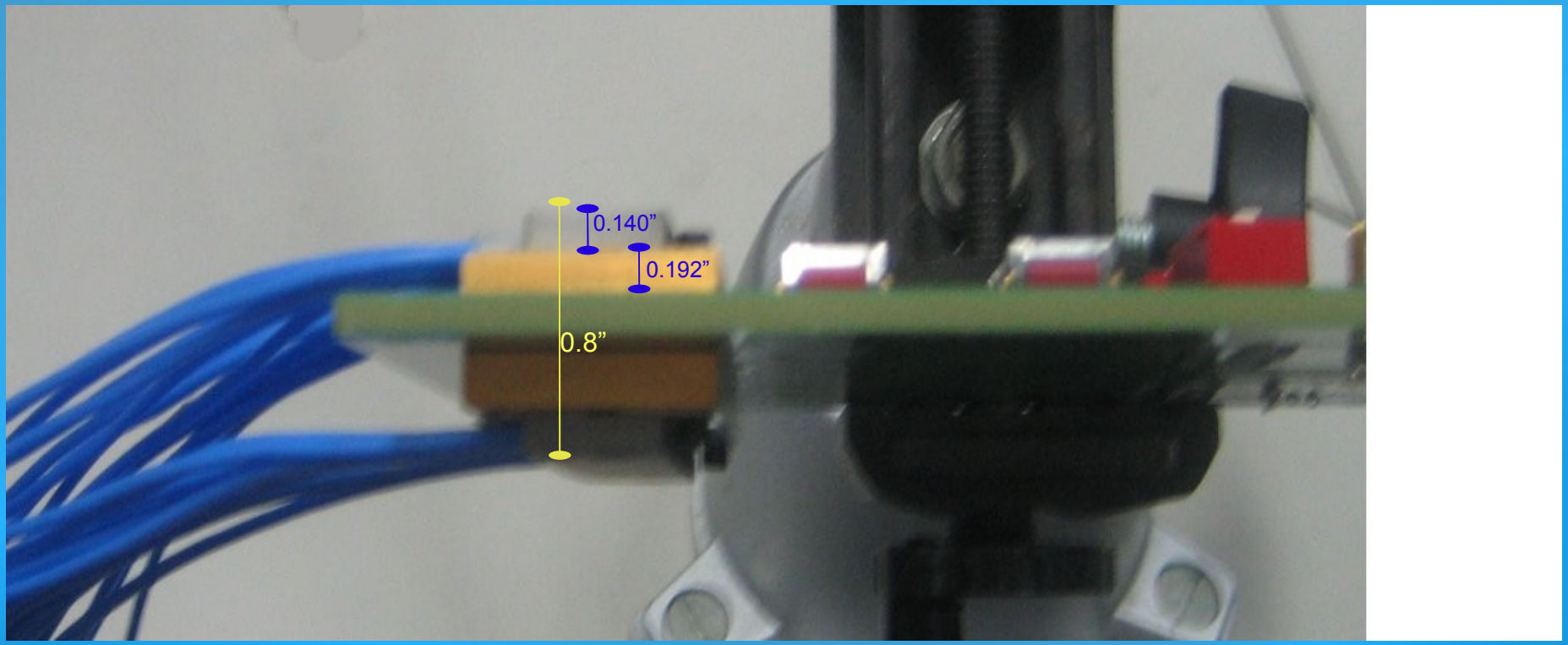
Edge Launch System Probing

- High Density 32 Channel Connector System for Back Plane Test Cards and DUT Board Applications Extensions
- Top Bottom Mount Clam Shell Connector
- 4 GHz Bandwidth over 2m

Specifications

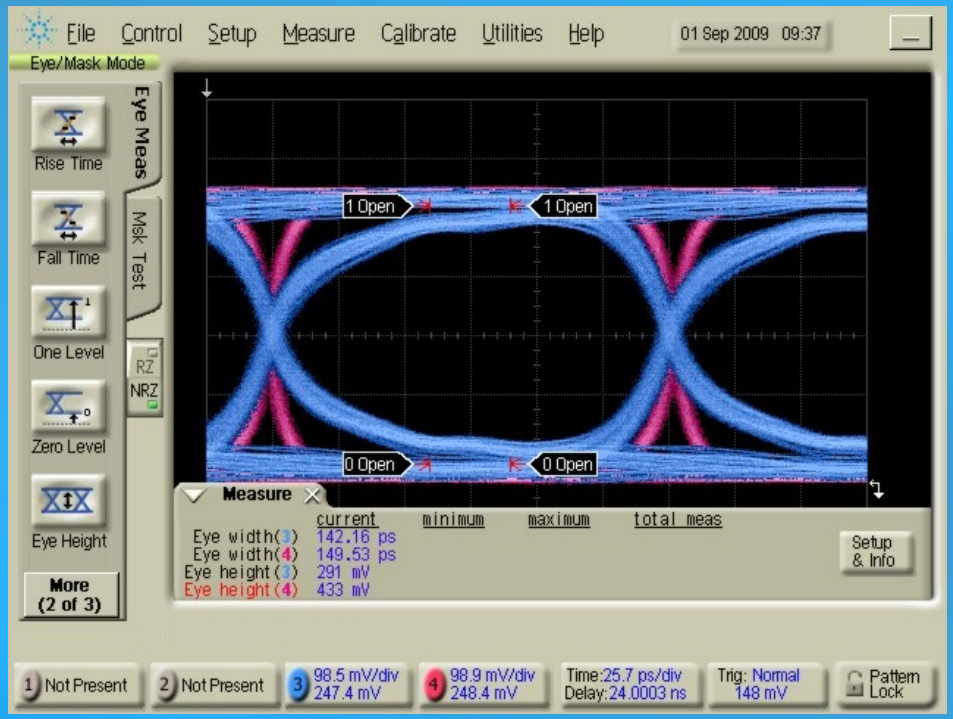
Number of Channels	32
Impedance	50 ohms +/- 5%
Loss Tangent @ 10 Ghz	-1.69 dB/ft
Bandwidth (-3dB)	4GHz
Return Loss	≤ -30dB to 10 GHz
Connector Crosstalk	< -110dB at 4 GHz

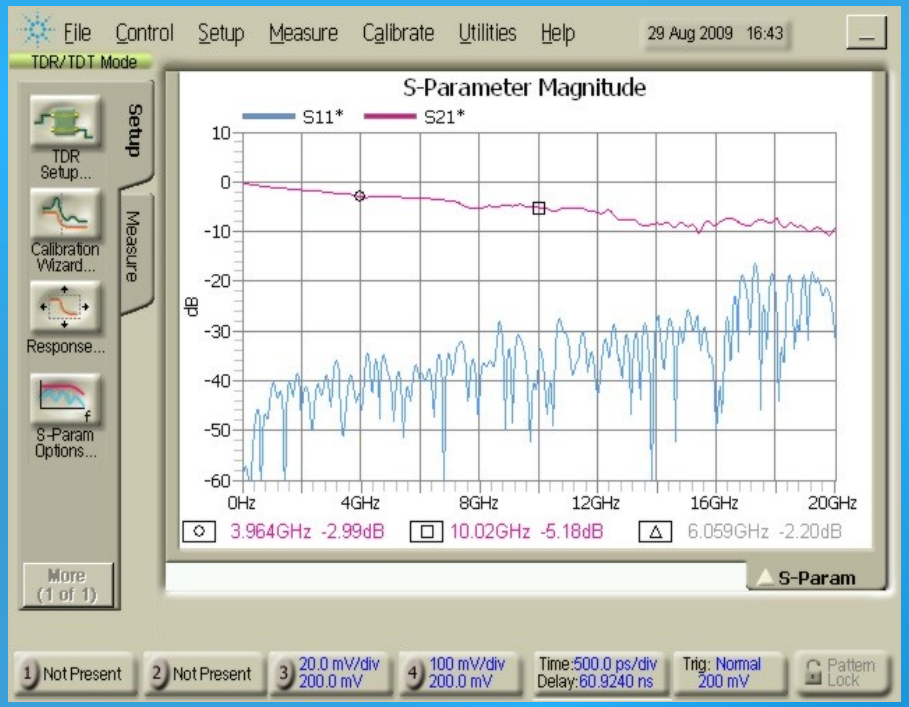
Clam Shell Application



In System Probe Card for FBDIMM2 Port

Connector Performance





2 m Cable Interconnect

Blue Trace Clam shell Connector
Red Trace JBERT through 1m Lab Standard

Summary

- Large Scale SOC Debug – Required Multiple Optimized Test Cell Solutions to Reach IO Speeds and Densities we Required
- Future DFT Support at Higher Bit Rates will Simplify Connector/Test Cell Designs
  - Learned some things!
- Partnership with Signal Integrity, Probe specialists and Board Suppliers was mandatory for success

Acknowledgments

- Partners
- Signal Integrity Inc - Probe Manufacturing and Design (www.signalin.com)
- MC Test Products – Boards Manufacturing and layout services (www.mctest.com)
- XpandATE Technologies – Overall System Design, Probe Design, Test, Signal Integrity Characterization (www.signalin.com)