



Advancing the High Speed Interconnect Ecosystem™ ...



# Advancing Test and Measurement Instrumentation using New Transmission Line Technologies

ATE, Load Boards, Test Sockets, Device Interface, and Probes

Jamal S. Izadian, Ph.D.

RFCONNEXT, Inc.,

[jsi@rfconnext.com](mailto:jsi@rfconnext.com)

[www.rfconnext.com](http://www.rfconnext.com)

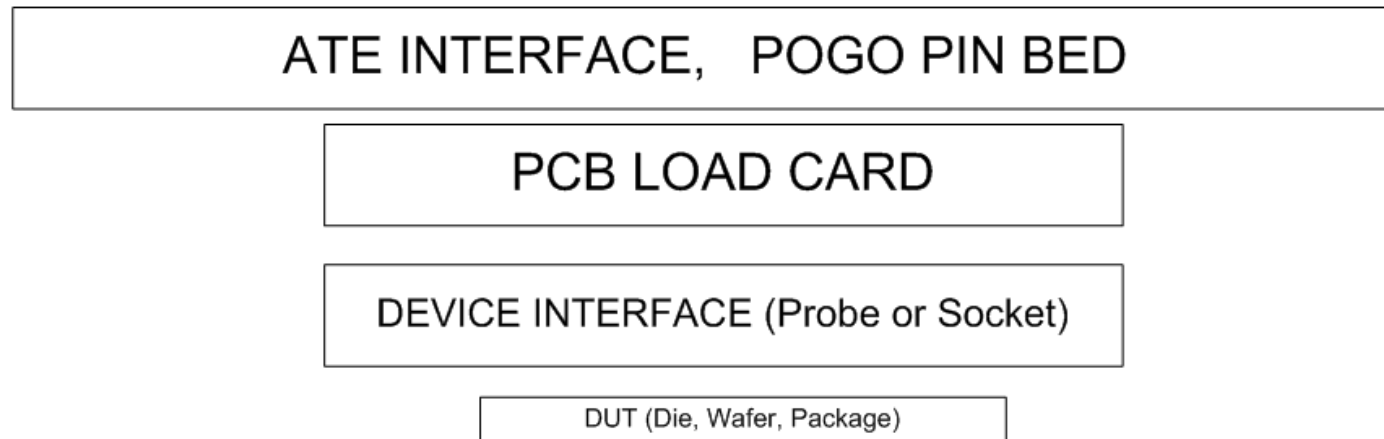
# Outline

- Incremental PMTL/VMTL embedding into ATE
  - A) Existing Test System
  - B) Evolving Test System
  - C) Overhaul of Current ATE
- Probes, Sockets, Cabling, Connectors
- N- Port Network Analyzer Implications

# ATE Systems Components

- ATE interface, POGO PINS bed/Blindmate
- Load Cards
  - Matching POGO PINS(or Blind Mate Connectors) contact array for ATE interface
  - Device Interface for
    - Test Sockets
    - Probes
- Handlers/Trays/Mechatronics

# Current ATE System Technology



# Intermediate Solution

ATE INTERFACE, POGO PIN BED

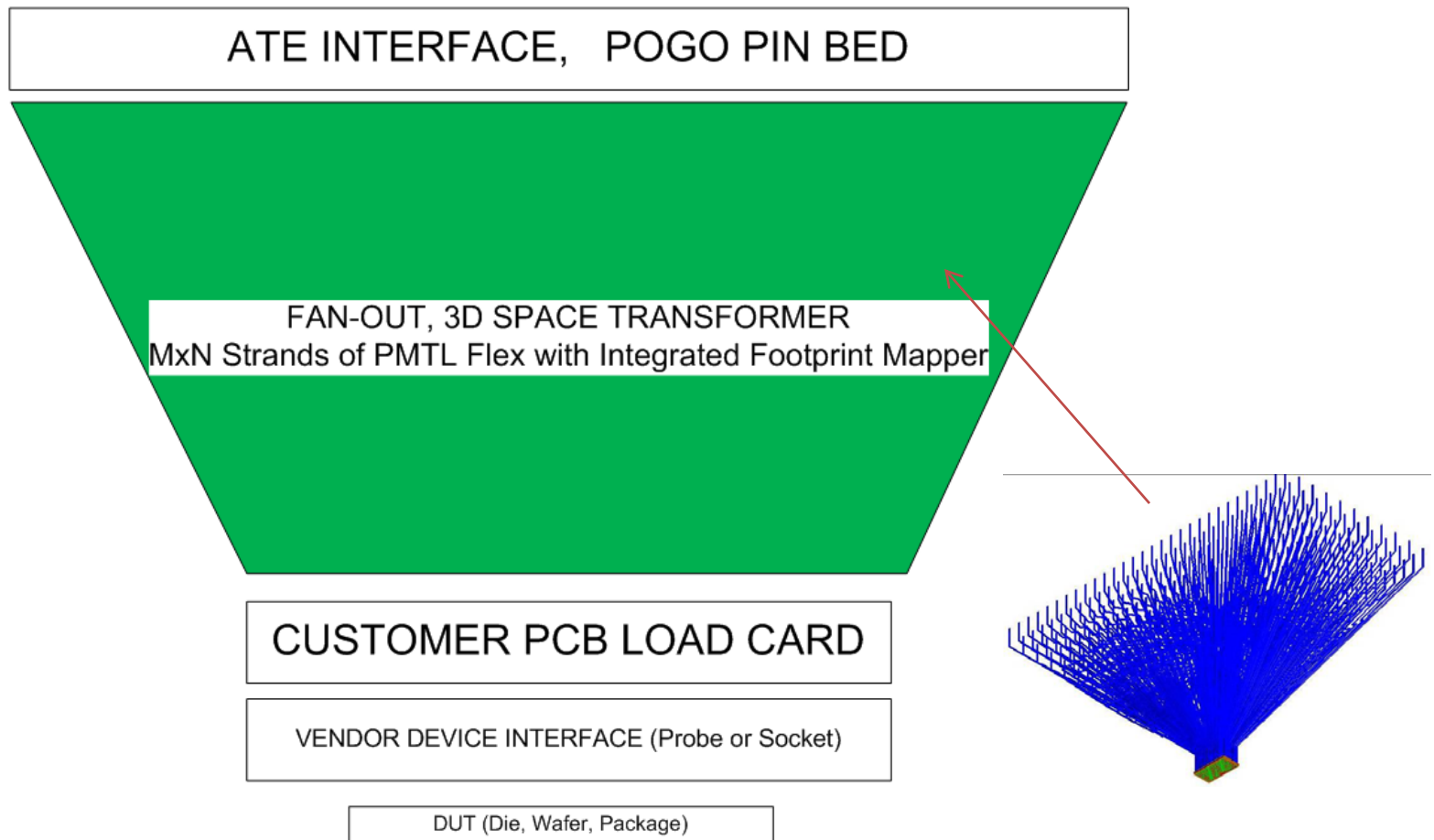
CUSTOMER PCB LOAD CARD

PMTL PCB LOAD CARD MAPPER  
From Customer Footprint to Vendor Foot Print

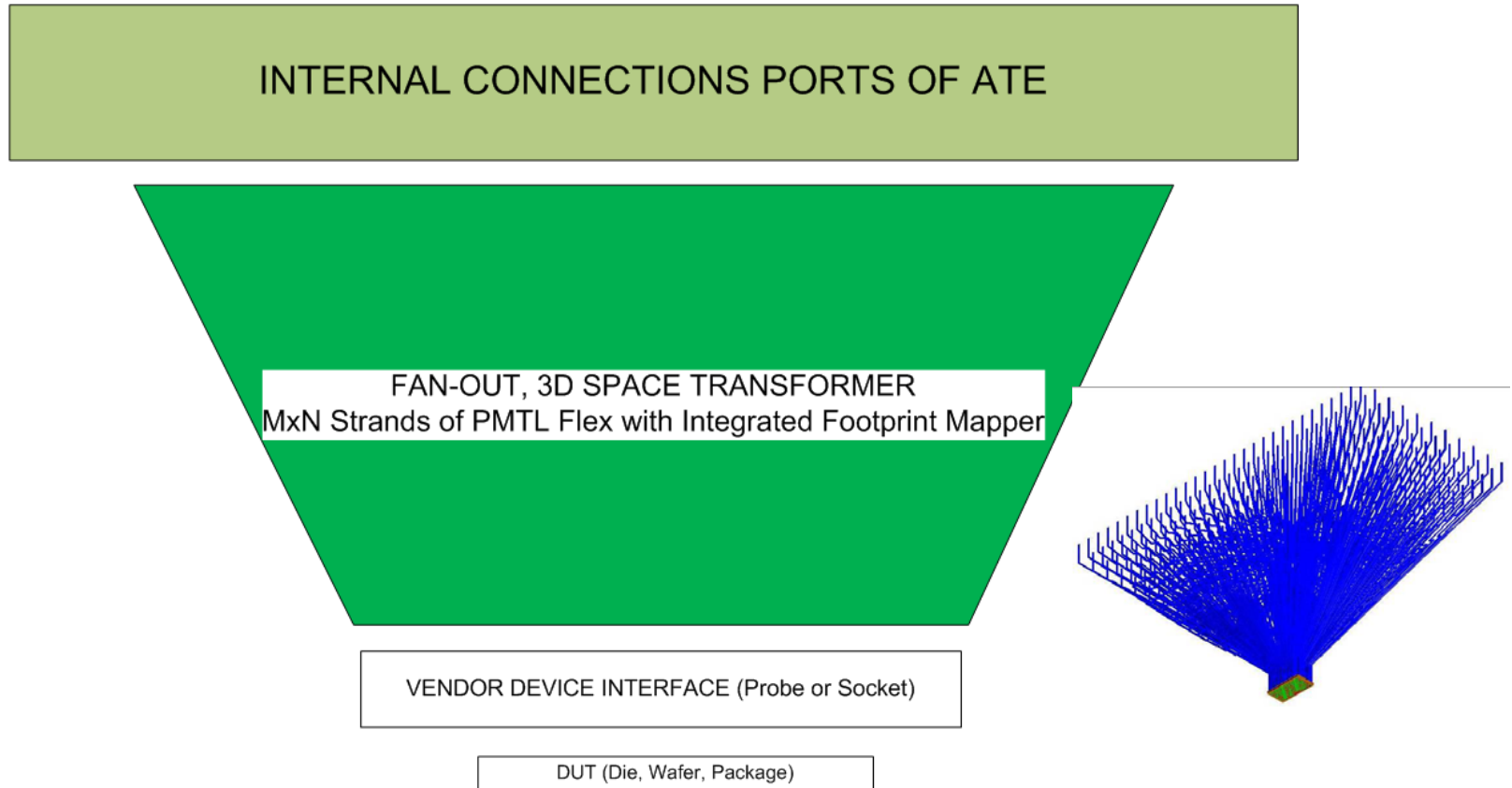
VENDOR DEVICE INTERFACE (Probe or Socket)

DUT (Die, Wafer, Package)

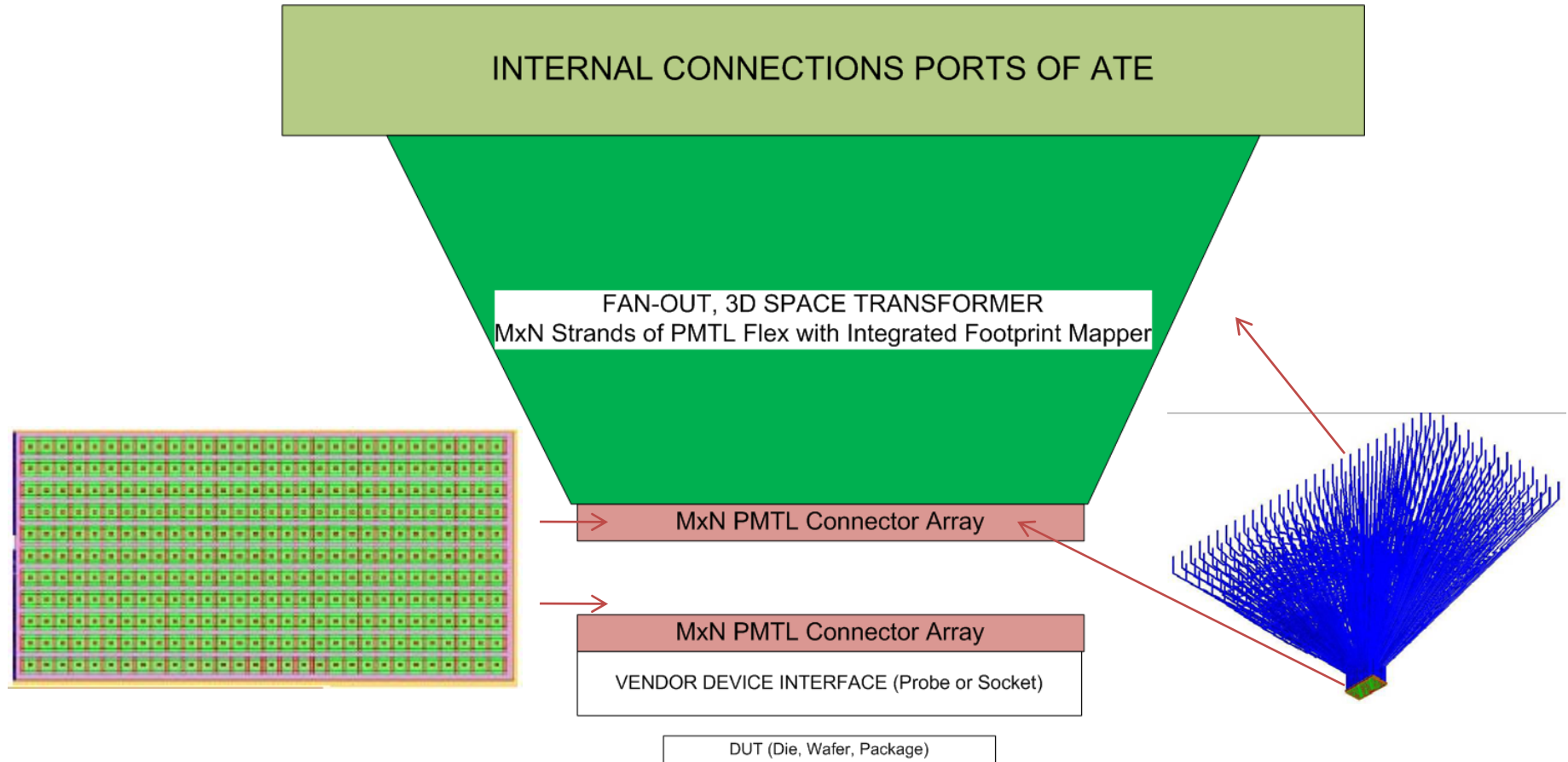
# Interfacing to Existing ATE Footprint Using PMTL



# Interface To Internal ATE Ports(Alternative to Probe Cards)



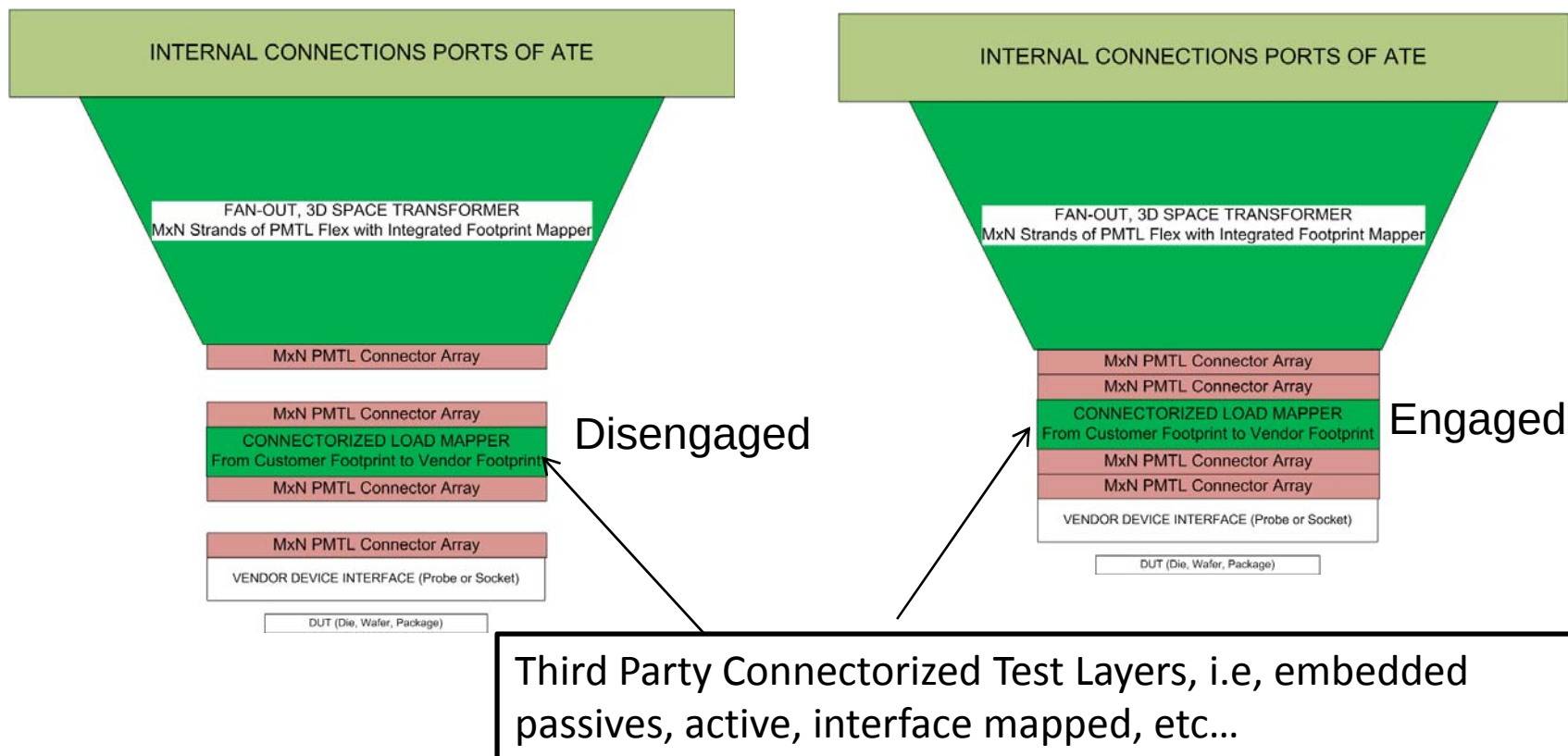
# Implementing Standardized PMTL 2D Connector Array



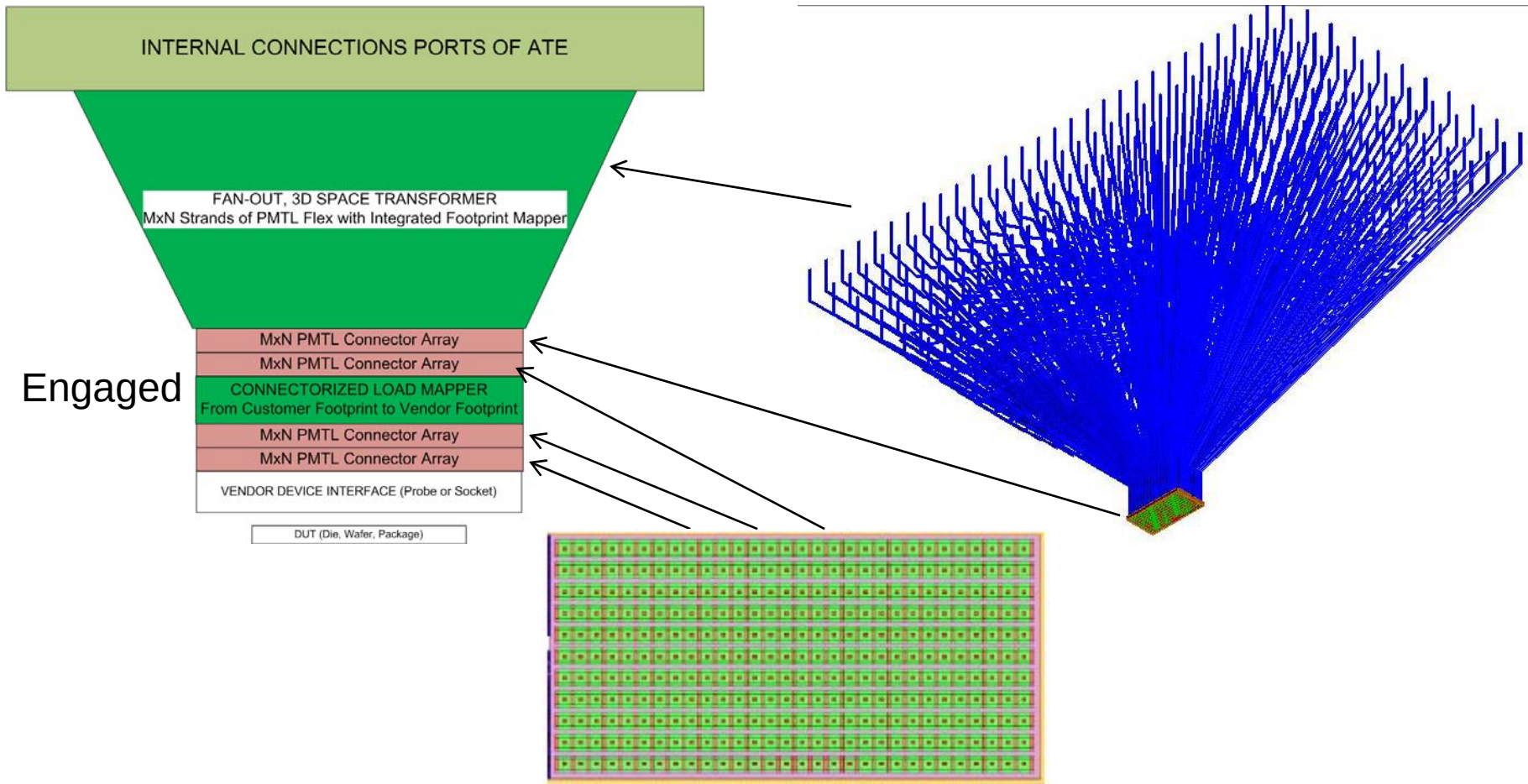


# Standardized Connector Array with Footprint Mapping

Allows all parts from ATE vendor, Device Interface (probes, Sockets) vendor, and spatial transformer vendors, all fit together perfectly



# Standardized Connector Array with Footprint Mapping, with uFlex PMTL

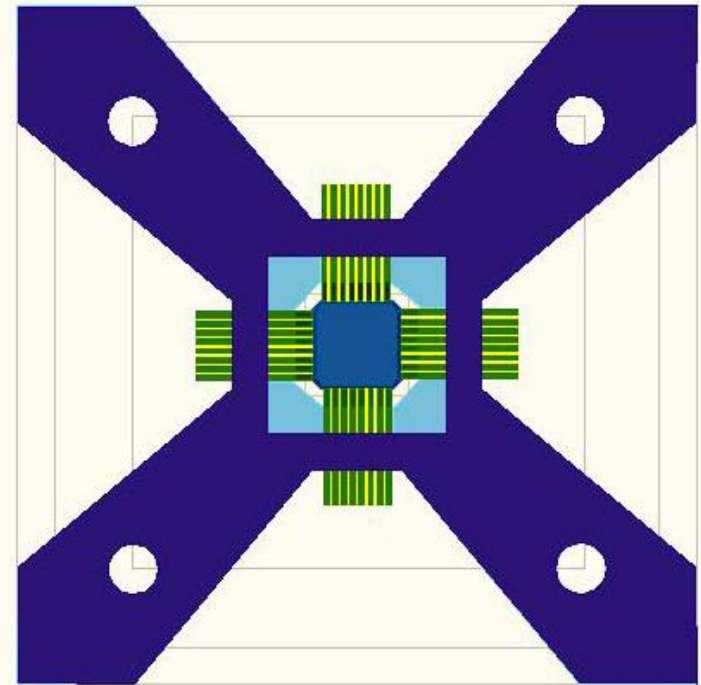


# Universal Test Socket For Quad Packs (UTS)

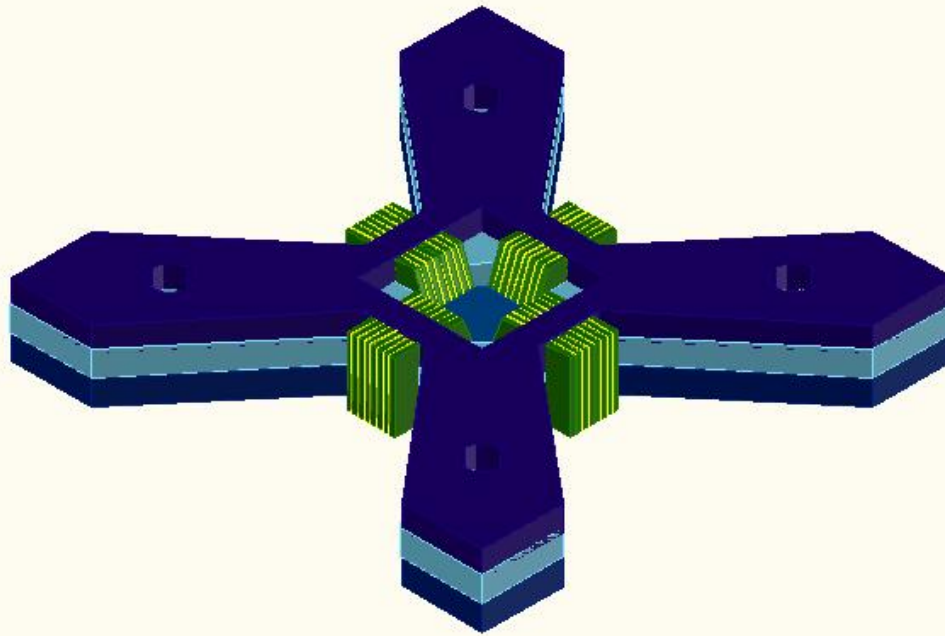
With embedded PMTL

# RFConnex's Reconfigurable Device Interface UTS

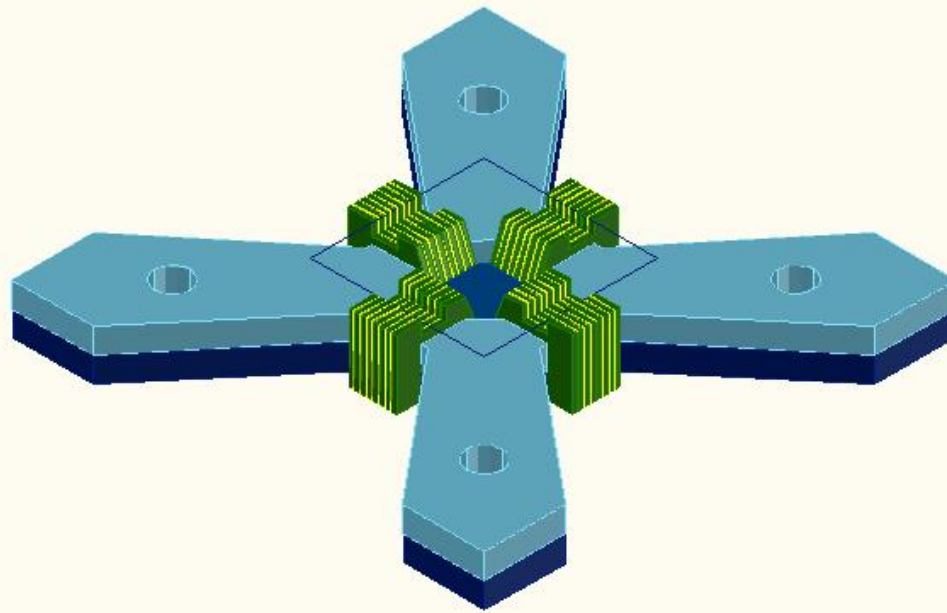
- Trying to Match Existing Socket Foot Print One-to-One (gray lines)
- Match the Boards Pad Foot Print
- Uses a Minimal Space
- Low Profile
- Modular



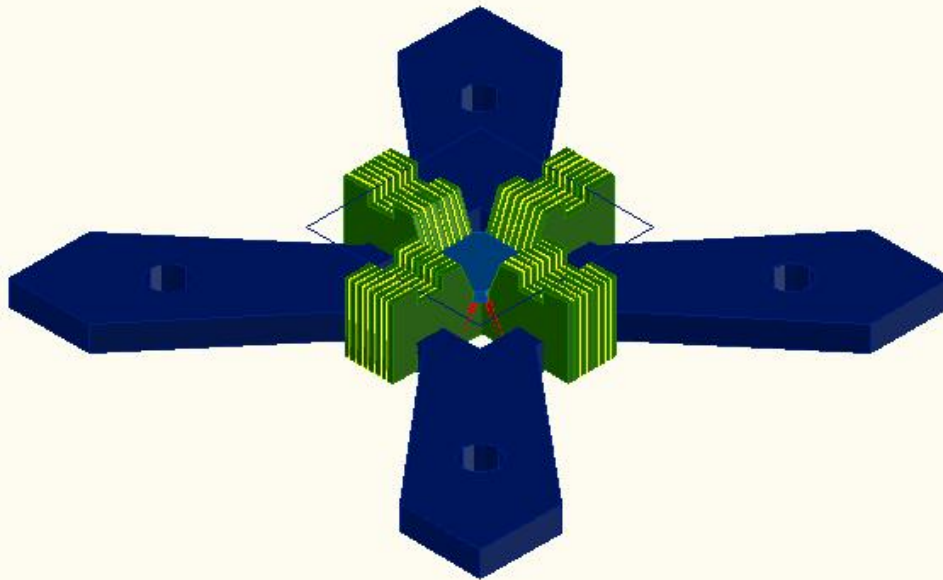
# 3D View, matching Foot print and Board Interface and Pad Pattern



# Removing Layers, showing easily replaceable contactors

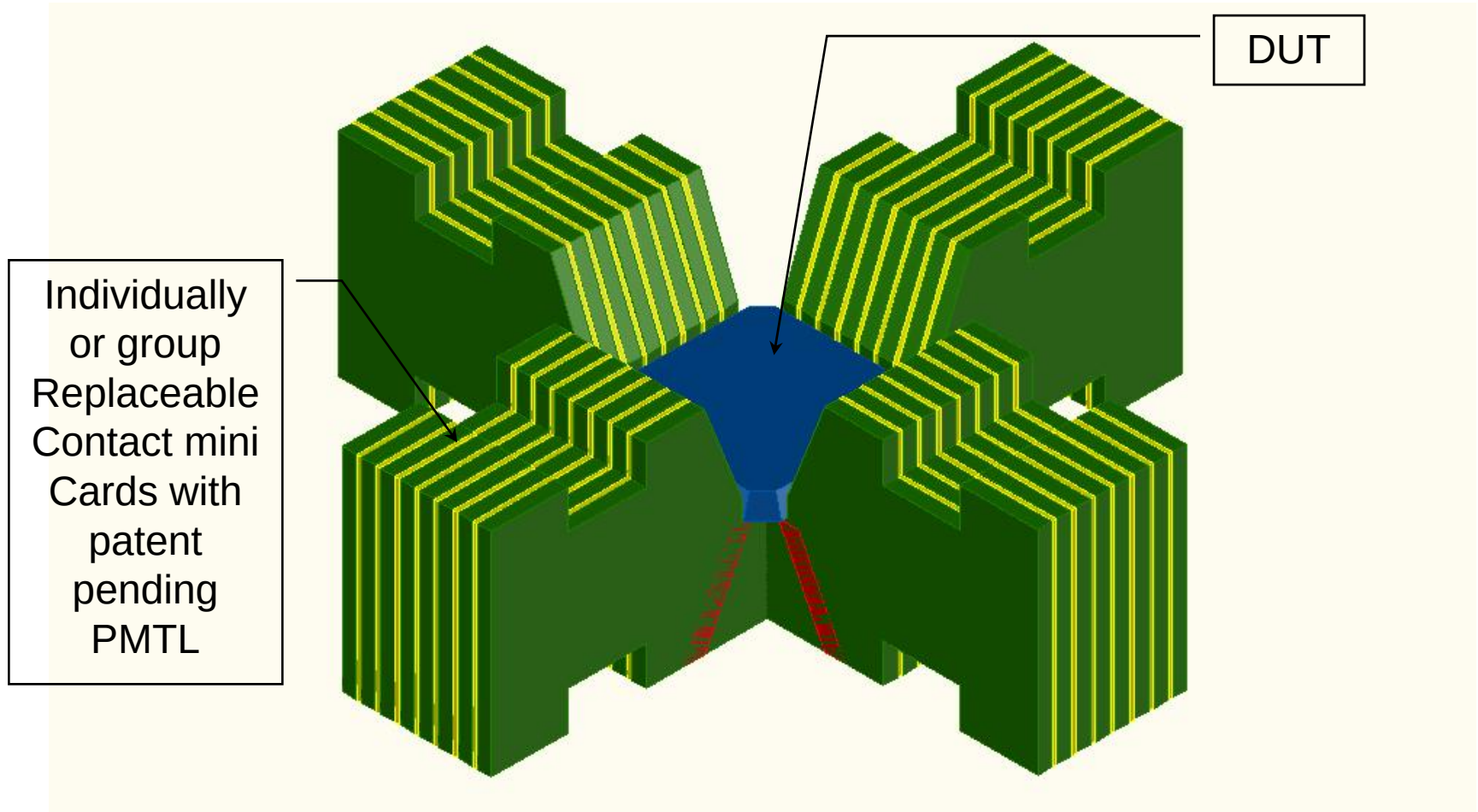


# Removing Next Layer, showing easily replaceable contactors



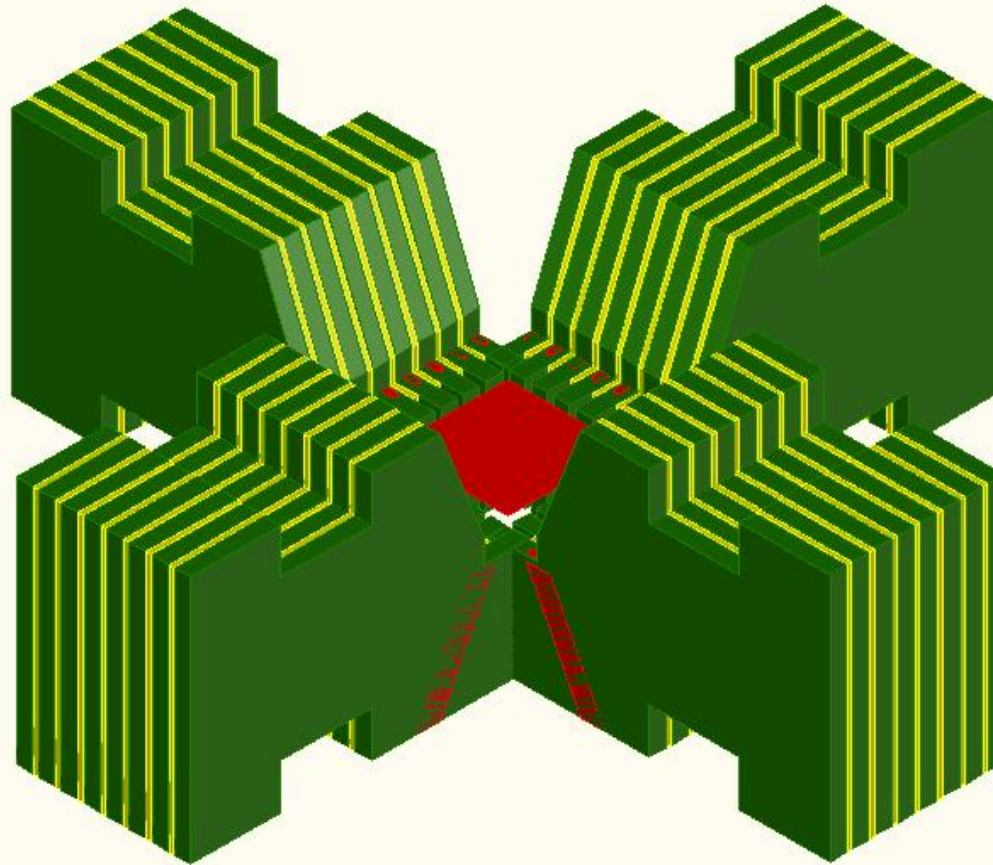


# The PMTL Connectivity, all replaceable parts

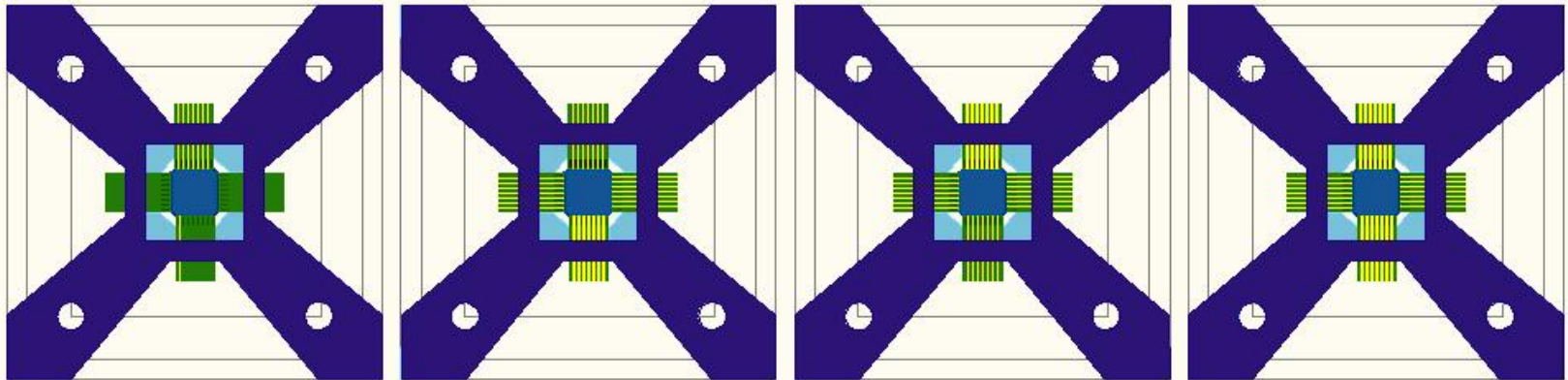




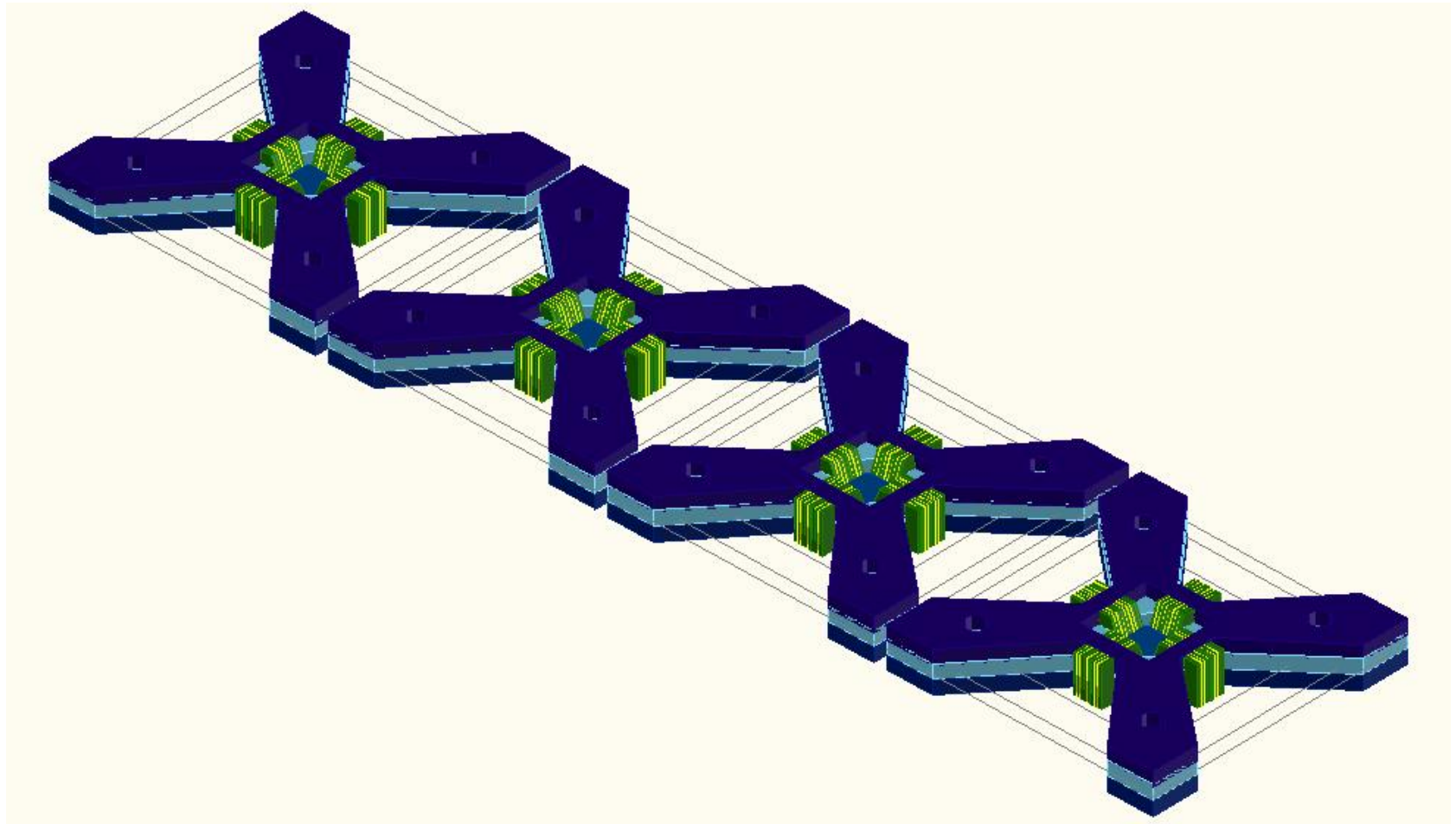
# DUT removed



# In Quad Arrangement 1x4 array , shown with QFN DUT



# 3D View



# Advantages of RFC Solution

- Because of patent pending PMTL, we can bring reference ground for Board pad to the DUT pins, reducing parasitic, and eliminating requirement for impedance re-matching
- Impeccable single or differential signals with controlled impedance
- Special connector technology, distributes the contact energy to larger areas, thus helping to last longer

# Advantages of RFC Solution-2

- Easy Access to Contactor and easy replacement from top, disposable
- No need to remove socket from Board for repair/replacement of contactor
- Ground Contact from side, and bottom,
- Heat Sinking are from Bottom
- Very low Foot Print, can increase DI density 64:1 for current performances board

# Advantages of RFC Solution-3

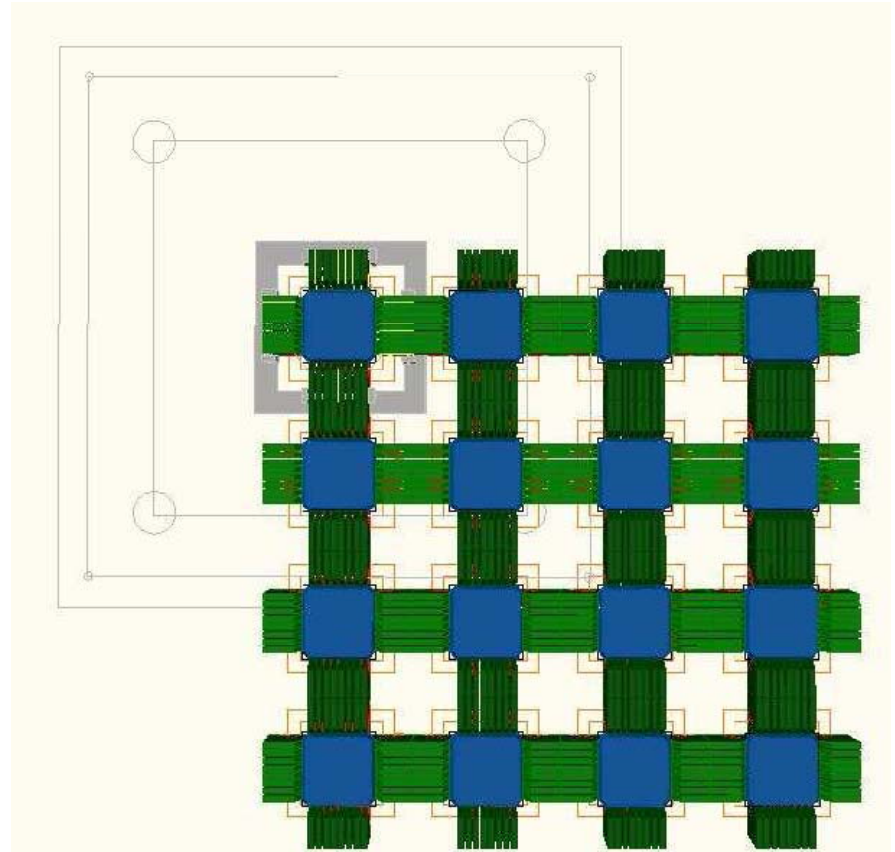
- Modular construction can be very easy access
- Scaleable to various DUT, and Packages and types
- Reduces ATE down time
- We were limited by the Existing Footprint, if we are allowed to modify Performance Board Pad pattern, slightly, we could further improve utility of our GIGA-LOW-UTS

Increasing DUT Density  
16:1 for a single Spot  
64:1 for Quad

Our Modular Technology allows  
Increasing Testing Parallelism  
On Existing Load Cards

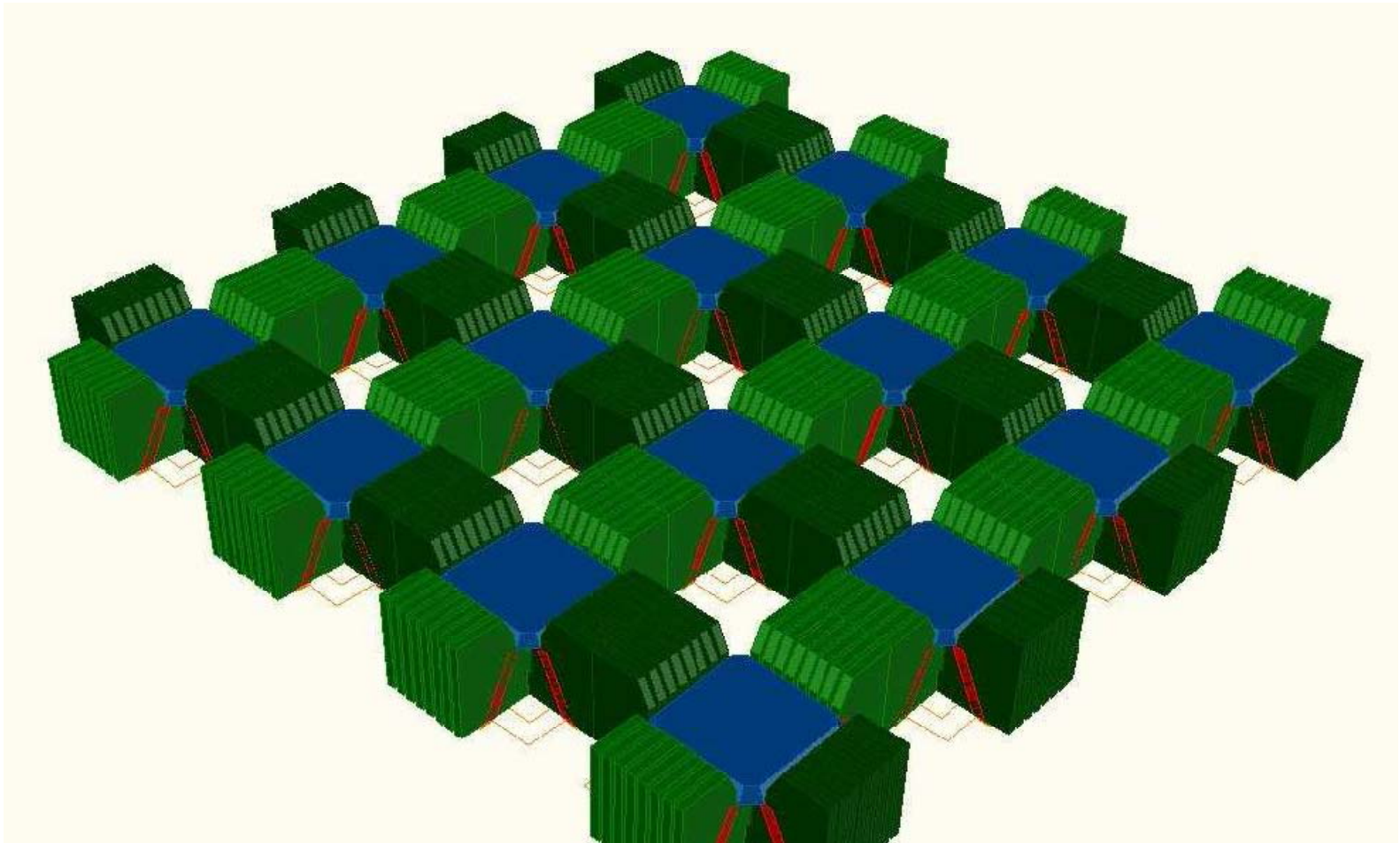
# Comparing Present Foot Print with a 4x4 DI (QFN DUT)

- Note that for the same Socket Foot Print, we can provide 4x4 interface or 16:1
- For the quad board, this will be 64:1
- Promises increased parallel testing

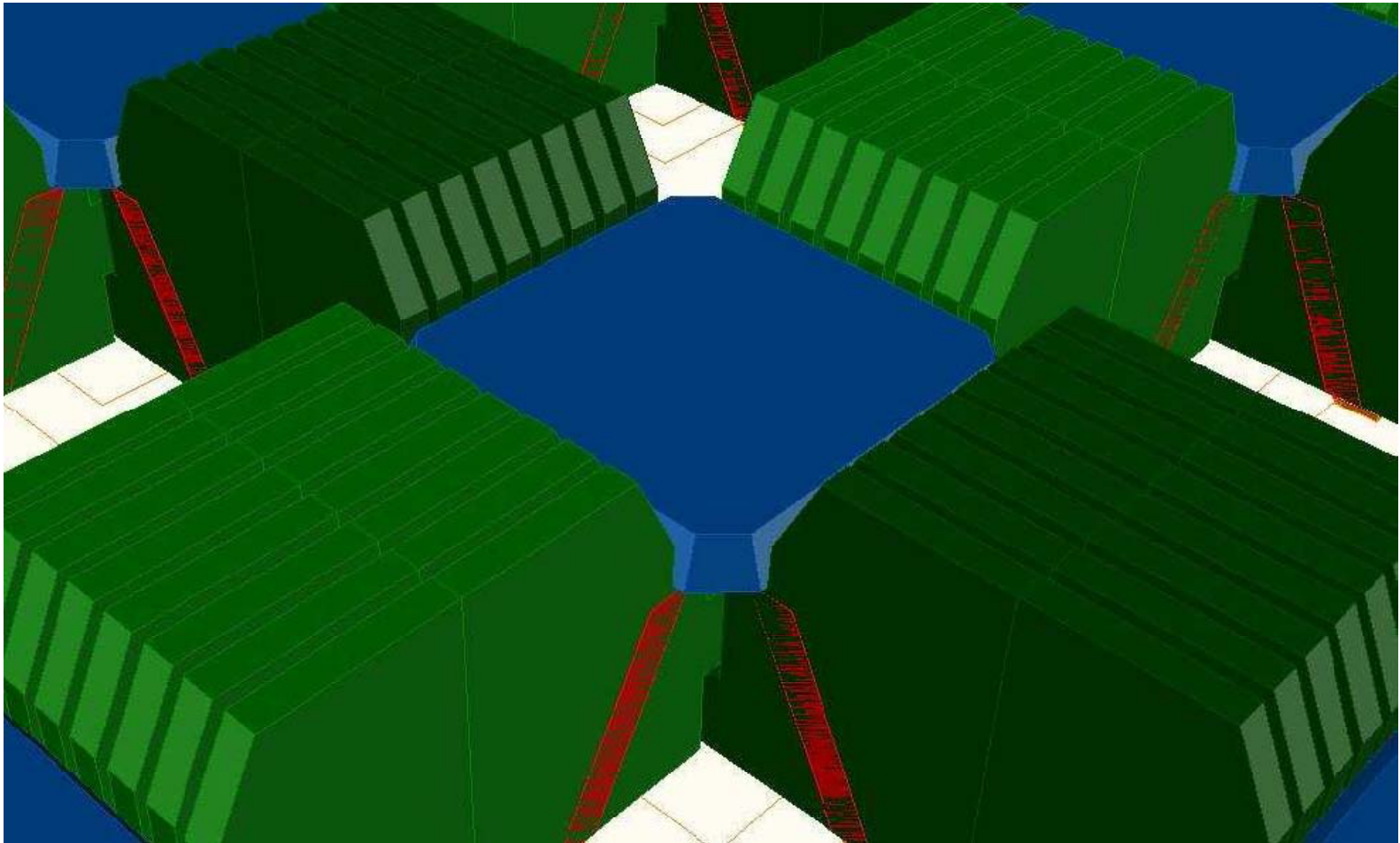




# 3D view of proposed 4x4 Socket Array



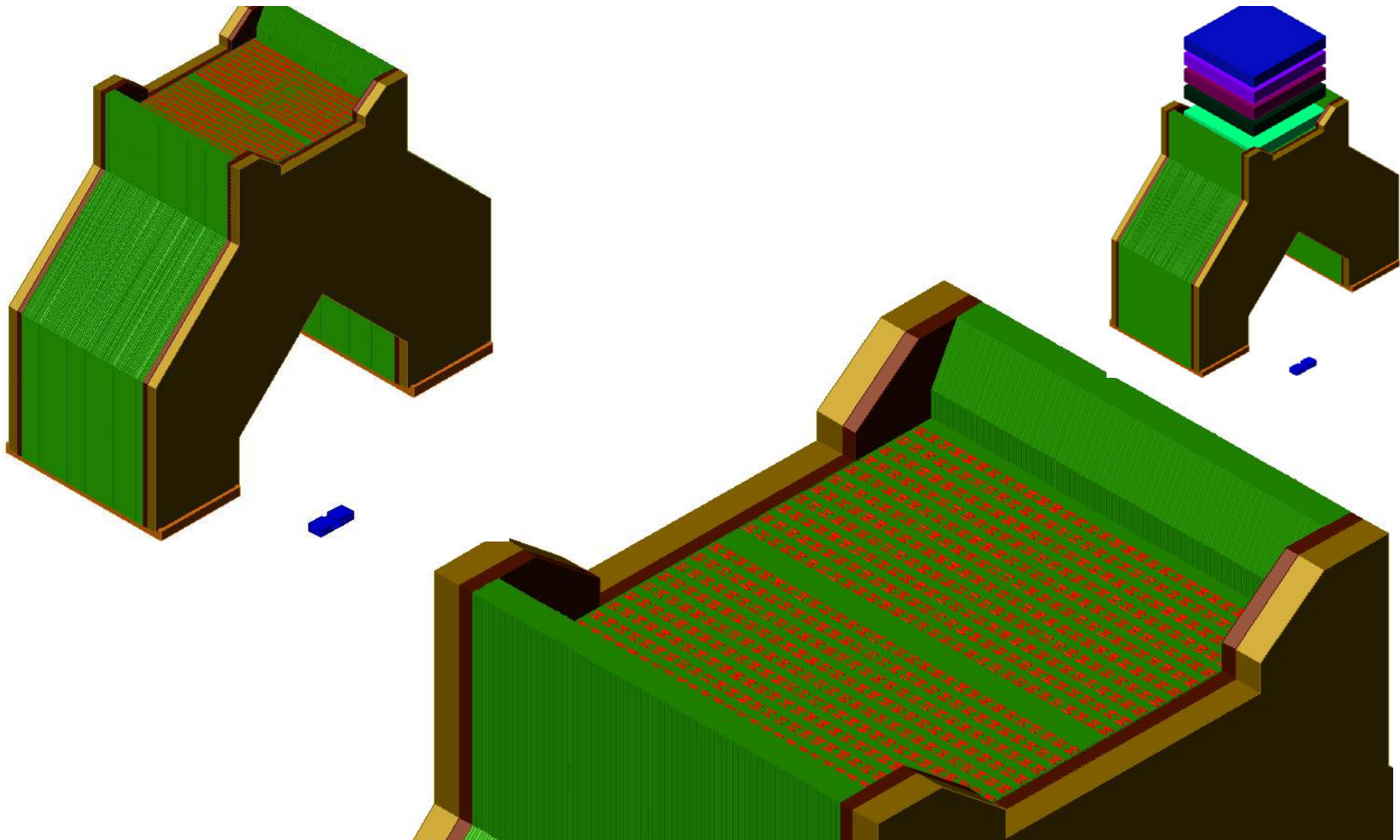
# Close up of a single DUT



# BGA/LGA test Universal Socket

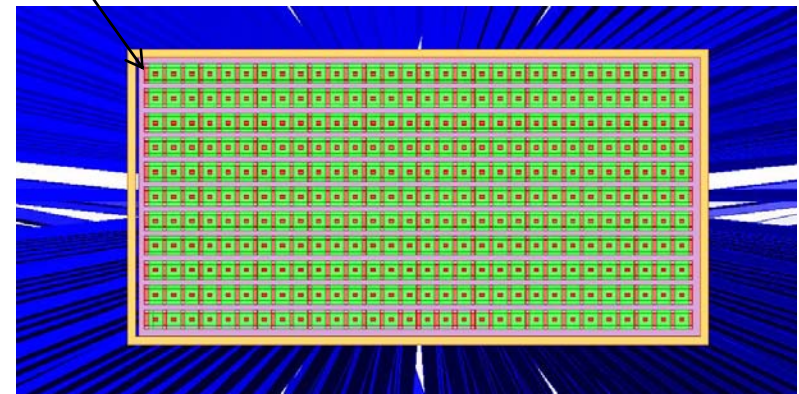
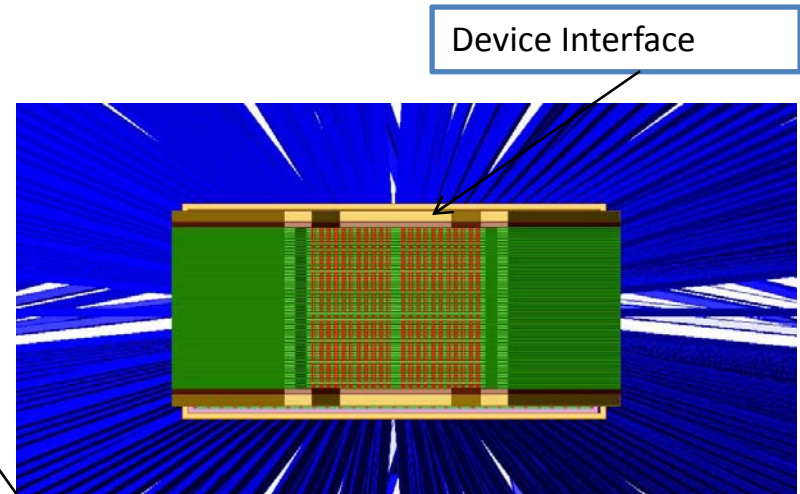
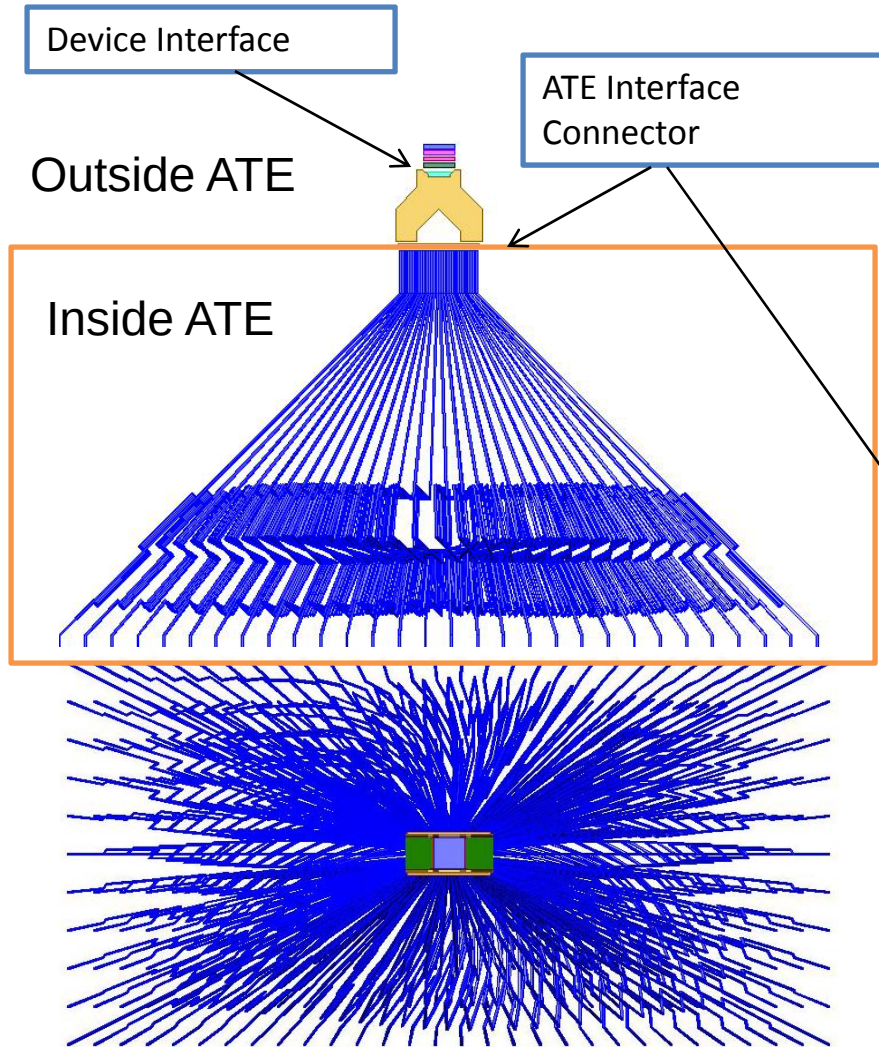
- With MxN array with possible calibrated reference at DI, using SOLT, LRL, TRL, TOSR, and others
- Uniform Signaling, DC-65GHz,
- Power, control, Mixed Signal, High Speed, RF
- THE FUTURE OF MULTI-PORT VNA

# UTS with 2D Connection Array, of Single or Differential, or Hybrid of PMTL external to Test Head





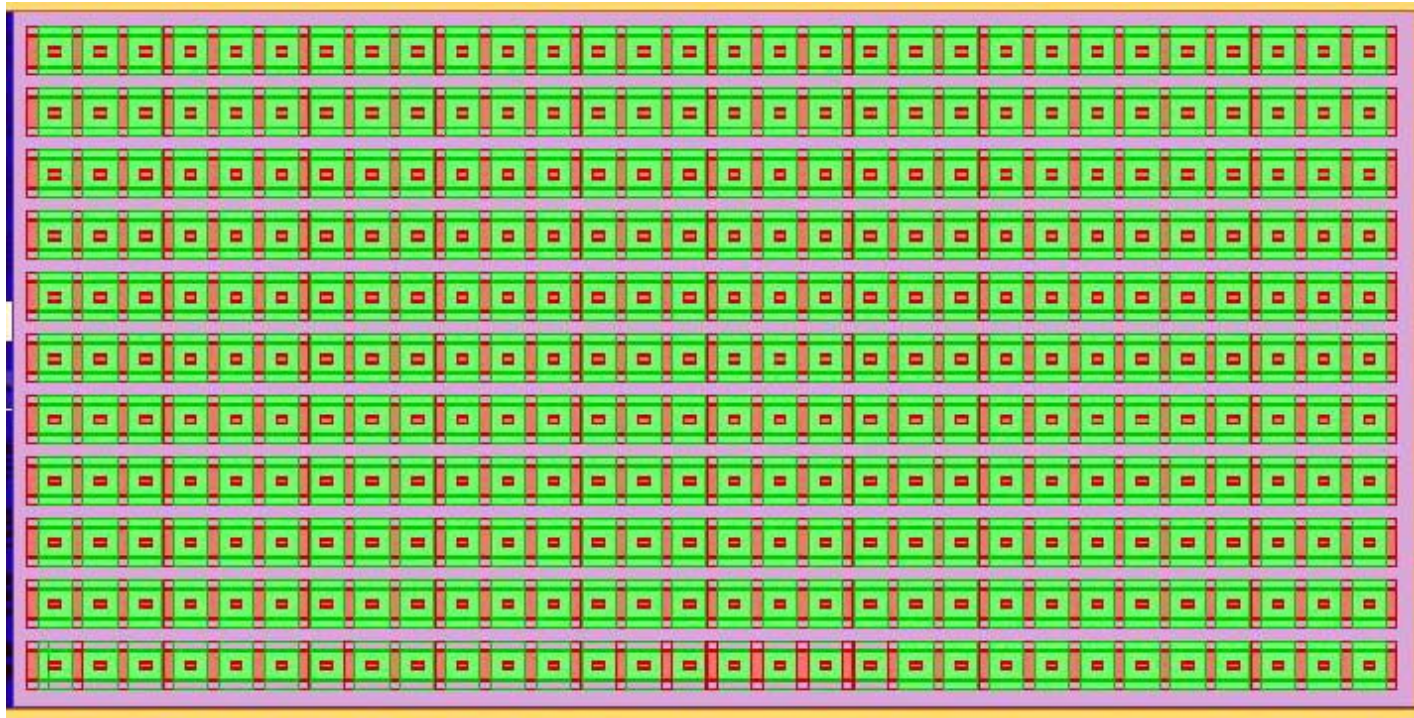
# Evolution of Integrated ATE and UTS



# The Future of ATE...

## Standardized, Mappable INTERFACE

- 2D Connector of full bandwidth, TEM PMTL interface... with uflex Printed PMTL Cables fan-out/fan-in



# The Benefits of New PMTL/VMTL Technologies for ATE's

- Standardized Footprint
- Multivendor, Multi user compatibility
- Controlled Impedance all the way to die pad
- Uniform Signaling contents,
  - DC
  - Control
  - Digital
  - RF
  - Mixed Signals
- Single/ Diff Pairs
- Embedded Components(Third Party Products)
  - L,C,R, Chips, Bias Tee's
- Superior Electrical Performance
  - No or low cross talk
  - No parasitic, PMTL™/VMTL™ Confined Field Interconnect(CFI)
- Universal Test Probes
  - Reconfigurable Footprint,
  - Pitches 25u and up
  - Variable force contact
  - Reusable, replaceable, disposable, low cost
  - Independent probes tips with +-z
  - Grouped in desired multiples
  - Match a large families of die pad patterns

# The Benefits of New PMTL/VMTL Technologies for ATE's

- Flexible PMTL Fan-out-in,
  - Complete mechanical decoupling,
  - Provide fine and coarse Z movements
  - Equal Delay, Minimum or no Skew
  - Controlled Impedance, Excellent match
  - Low Insertion loss
  - Provides excellent phase linearity compared to traditional coaxial lines and connectors
- Standardized 2D PMTL Connection Array
  - No more POGO pins
- Mapping any ATE to any Device footprint
  - Cheaply
  - Readily
  - Cross Platform Utilization
- Wide bandwidth for the future
  - PMTL™/VMTL™ TEM transmission line technology provided DC-50GHz bandwidth and beyond at no significant cost
  - More connectivity density per area



# Multi-Port Vector Network Analysis

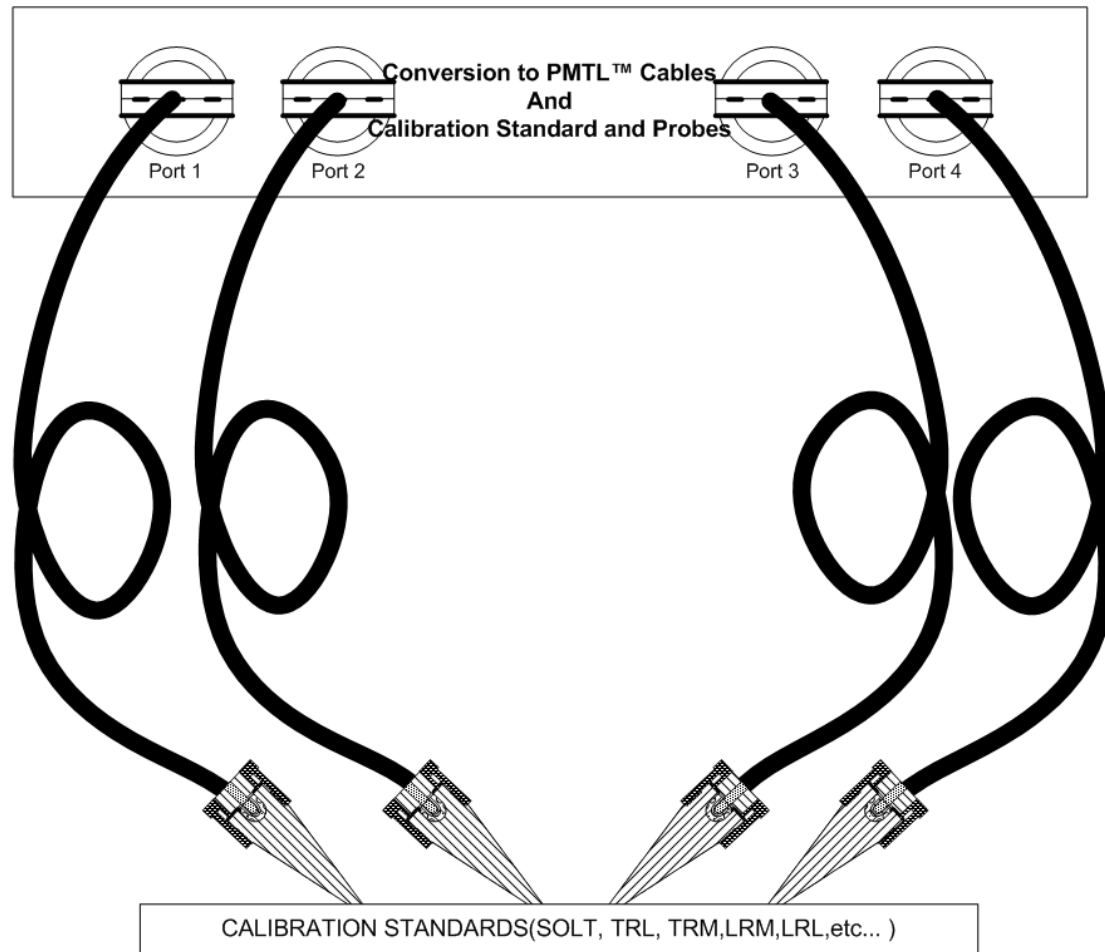
Looking Beyond 12 Port Network  
Analysis to 65GHz

*The COST of ownership must come down, Only new  
technology can make this possible*

# Enabling Technologies

- Lower cost Full Bandwidth Printed uFlex PMTL cabling
  - Unmatched Phase Linearity under bending/twisting, Highly repeatable
  - Use as internal VNA semi-rigid routing
  - Integrate on internal board signal routing
  - Use as front end VNA test cable
- Use Low Cost Flat Printed PMTL End Connectors /Launcher(No precision machined needed)

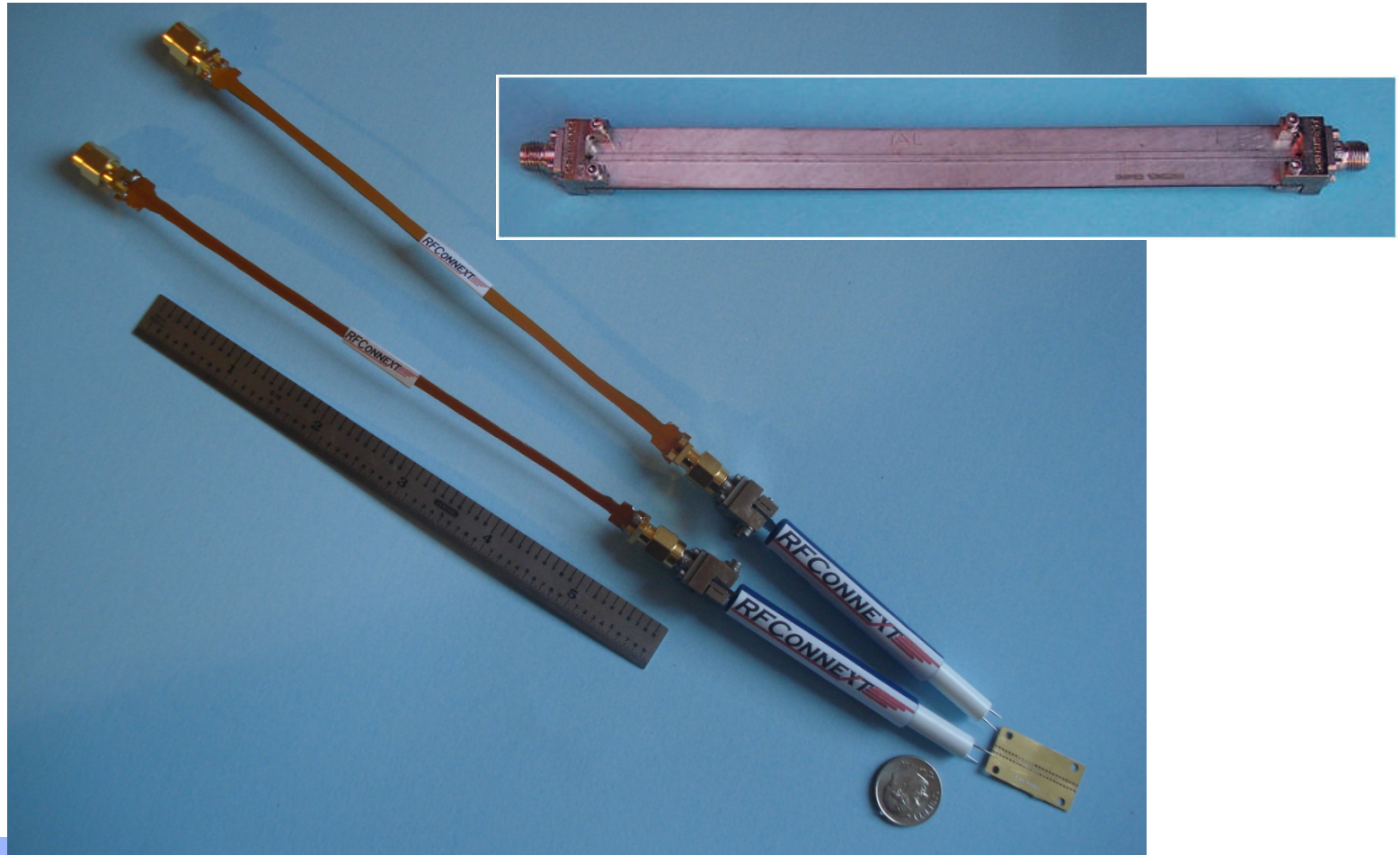
# Future Face of Full Bandwidth Network Analyzer(everything printed)



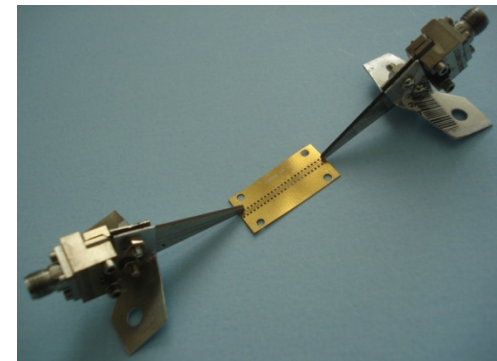
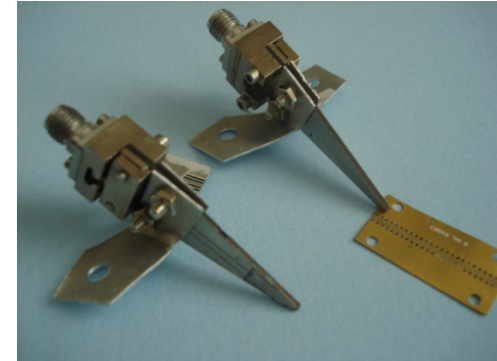
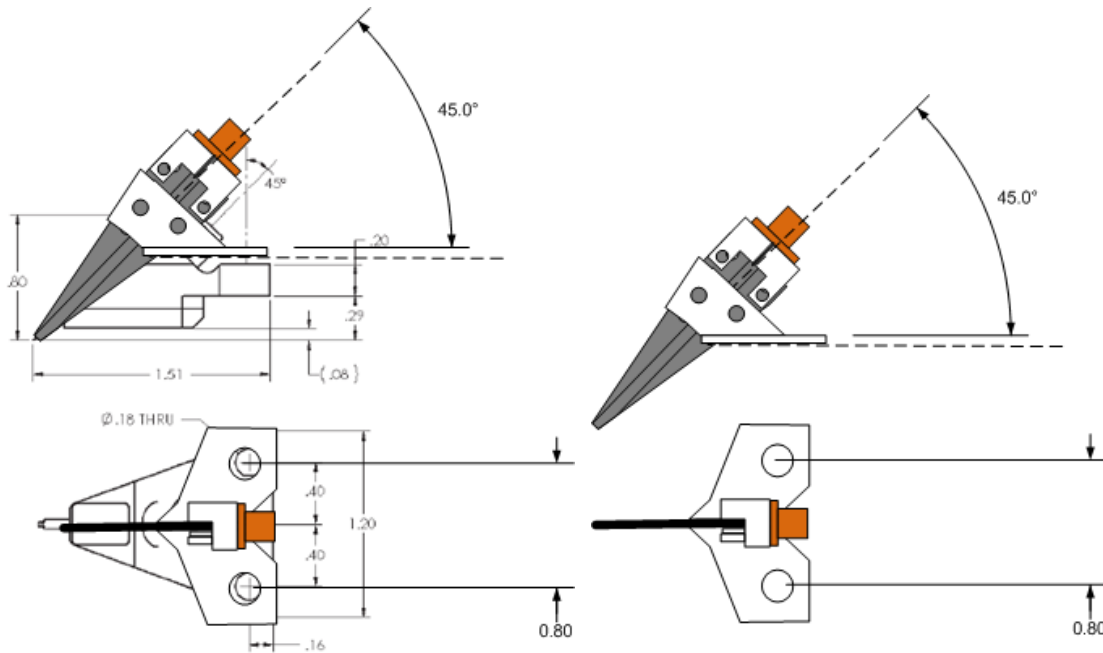
# Enabling New Probe Technologies

- Increased Density, while increasing bandwidth and speed
- Contact Controllability and compliance designed in
- Re-configurability
- Low cost disposability
- Field Repairable, all built in...

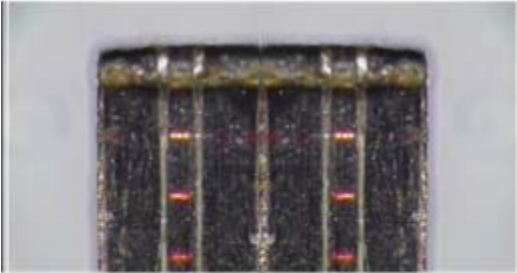
# Handy Probes with Printed High Speed uFlex



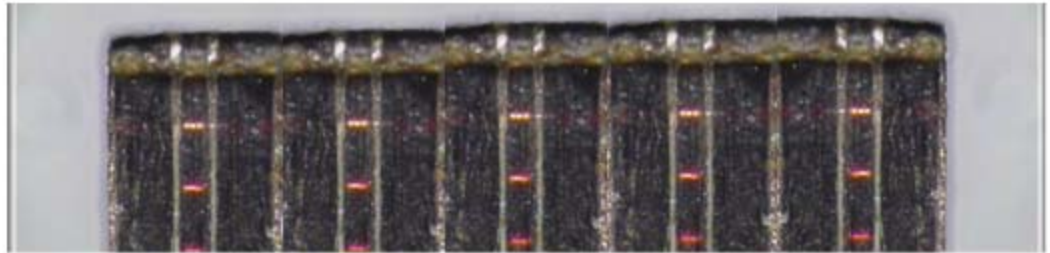
# Example of One-to-One Replacement for existing wafer Probes, and Any other(Super Imposed for Comparison) DC-50GHz...



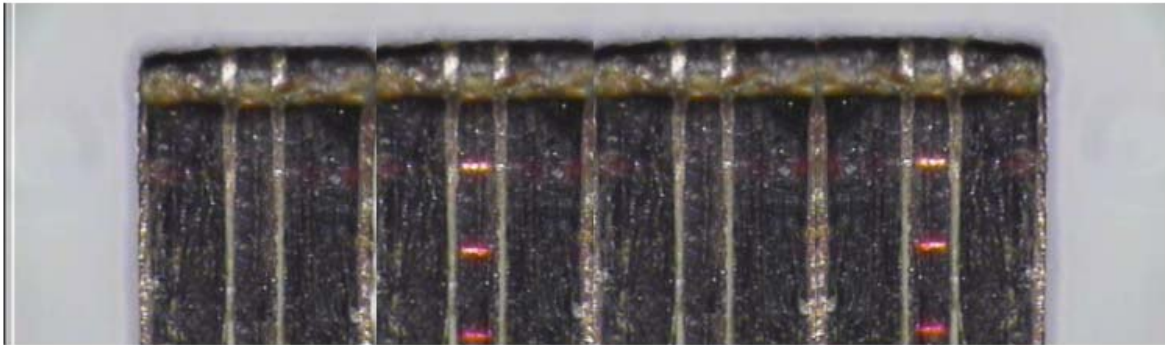
# Scalable, reconfigurable, printable matching any footprint, compliance



**PMTL Probe Tips  
GSGSG**



**PMTL Probe Tips GSGSGSGSGSG**



**PMTL Probe Tips GSSG,SGS, GSSG, GSG**



# Summary, Improving the ecosystem

- Testing is already expensive and complex
- Devices are becoming even more complex
- Testing must support a new high speed ecosystem
  - Must do more, faster and cheaper over wider bandwidth at speed
  - Must increase automation, parallelism, reduce TTM
- High Speed Interconnect is at the heart of it...