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The Quest for the Perfect Loadboard:

Understanding the Issues and Technology Advances in Device-to-Tester Interface Assemblies

The Quest for the Perfect Loadboard

Understanding the Issues and Technology Advances in Device-to-Tester Interface Assemblies

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The Quest for the Perfect Loadboard: - Purpose and Outline

The purpose of this presentation is to describe “non-ideal” losses in printed circuit board technologies and discuss emerging technologies to address these issues.

Outline:

1) Ideal vs. Non-ideal Losses
2) Classic Solutions
3) Emerging Technologies
    a) Conductive Bridge Technology
    b) Coaxial Vias
    c) Embedded Component Technology
    d) Embedded Coaxial Structures
4) Concluding Comments

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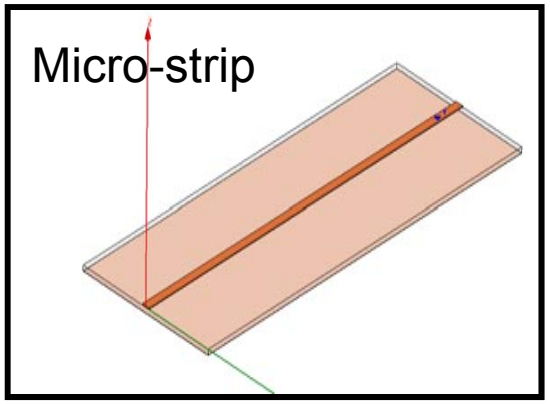
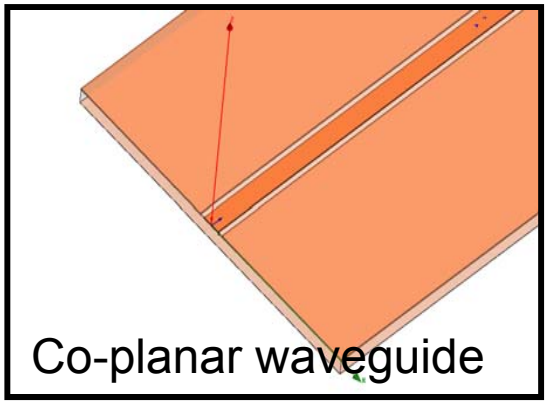
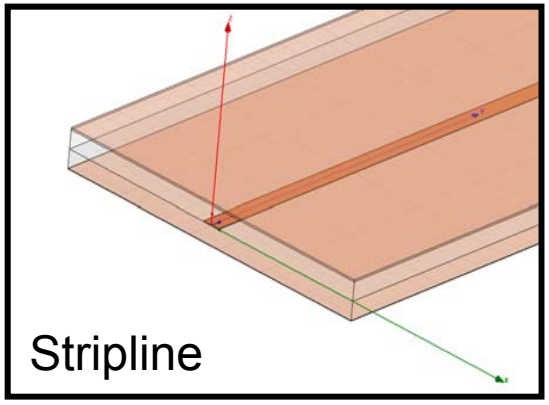
The Quest for the Perfect Loadboard
1. - Common Transmission Line Structures

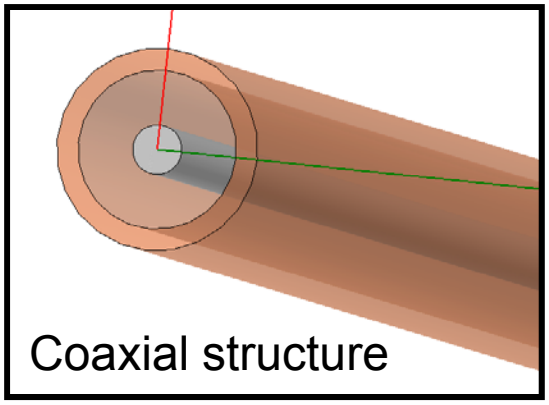


Ideal Losses:
-Serial Loss (skin effect)
-Dielectric Loss

Non-Ideal Losses:
1. Etch Tolerance
2. Average Material Thickness Tolerance
3. Within-sheet Thickness Variation
4. Material Weave and Dielectric Variation
5. Metal Plate Variation
6. Regional Variation Within a Board
7. Copper roughness







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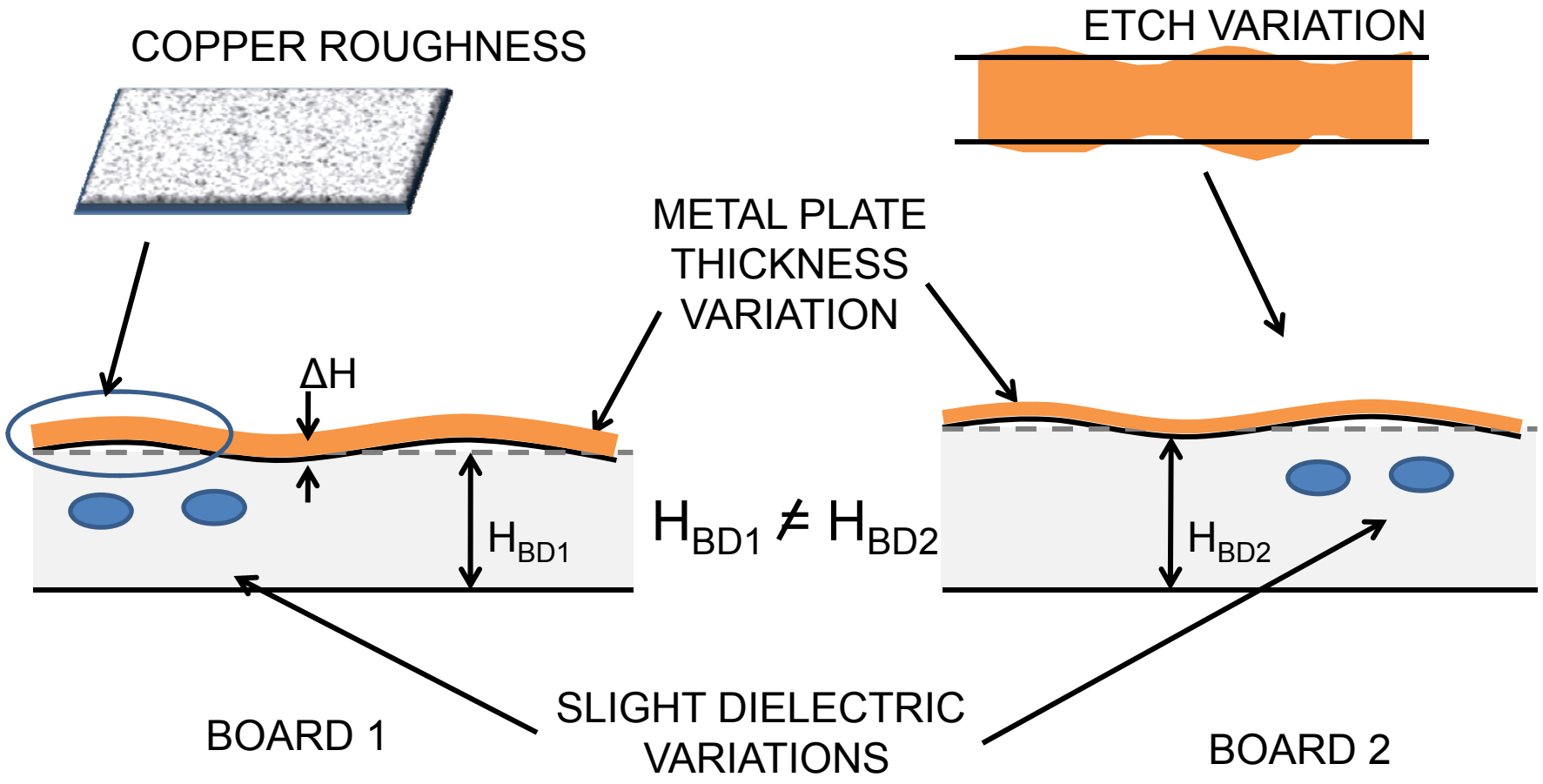
1. - Practical “non-ideal” Losses



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1. - “micro-reflections” concept

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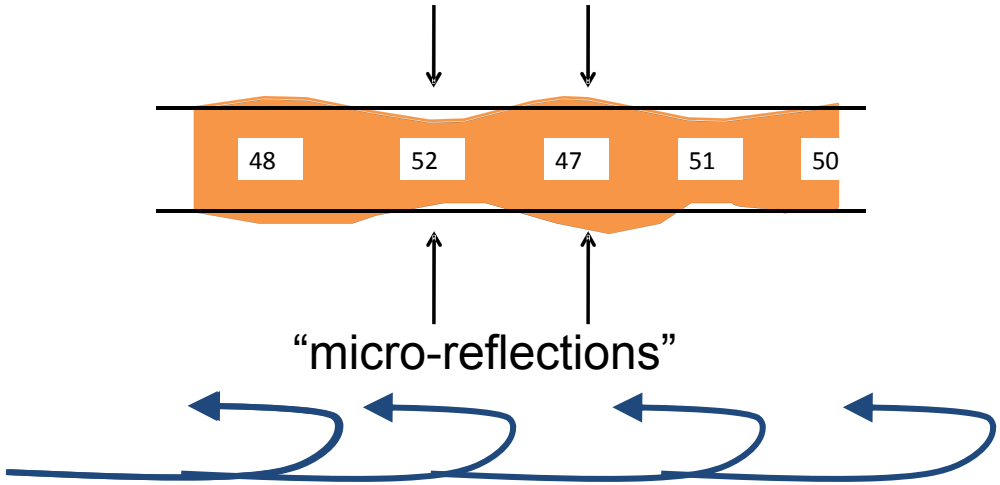
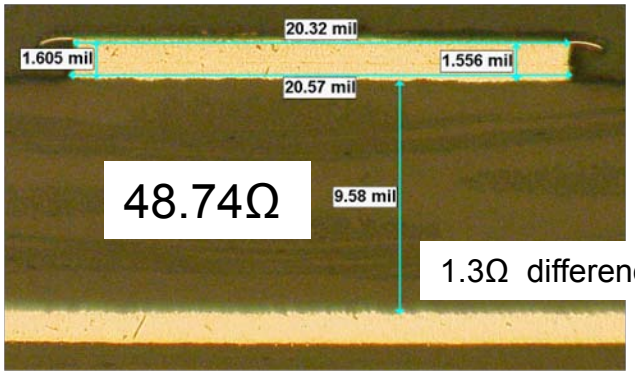
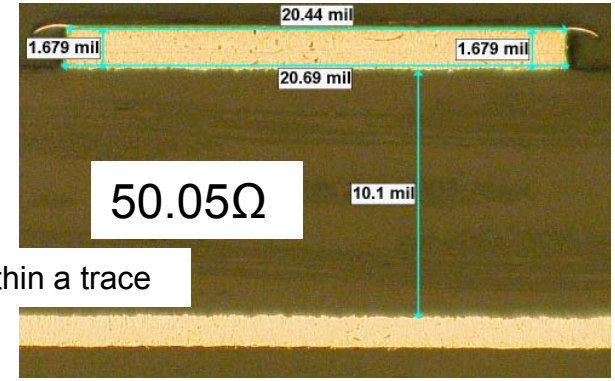
Etch Tolerance Within a Trace







1.3Ω difference within a trace

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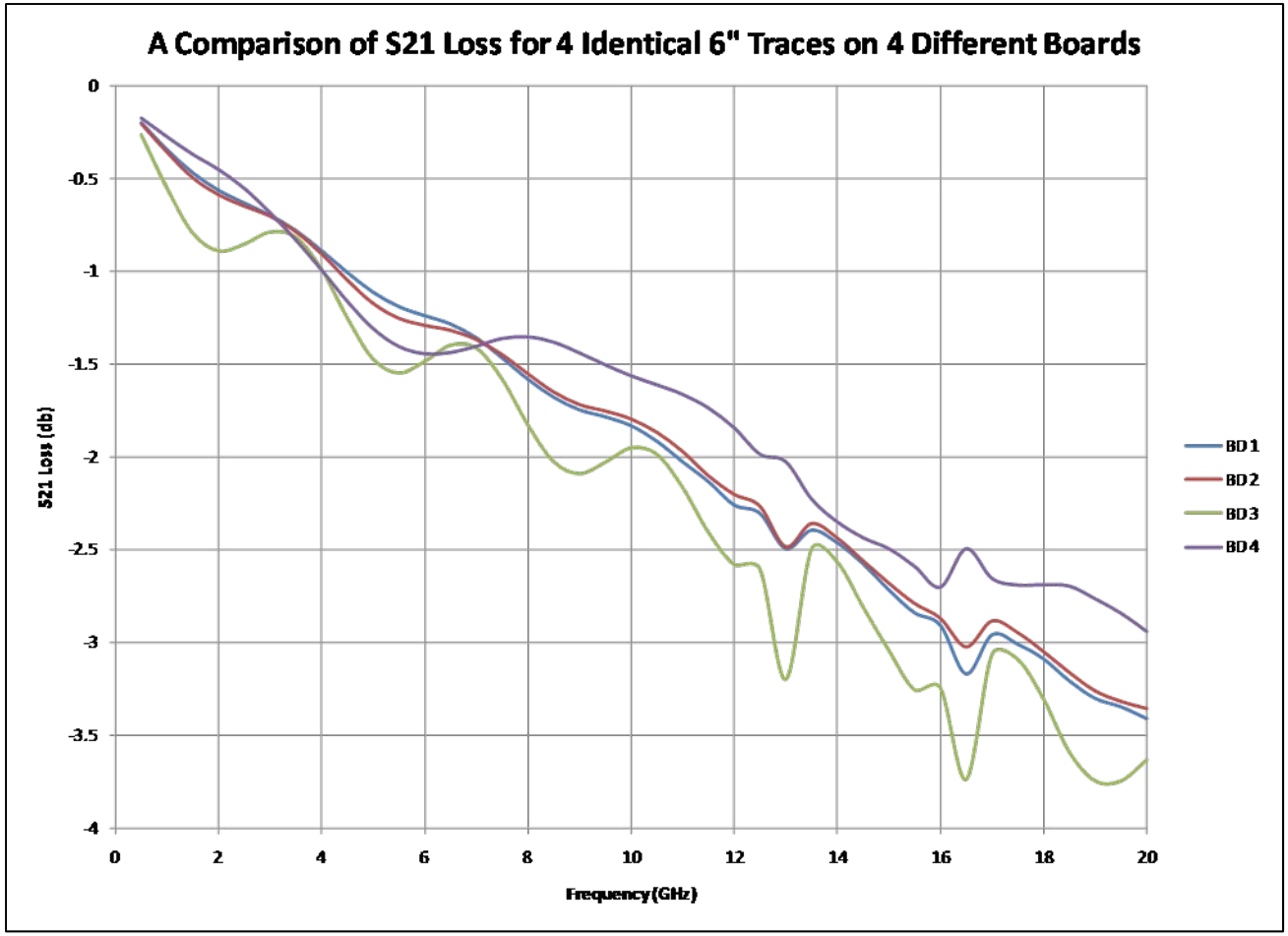
1. - “micro-reflections” consequences



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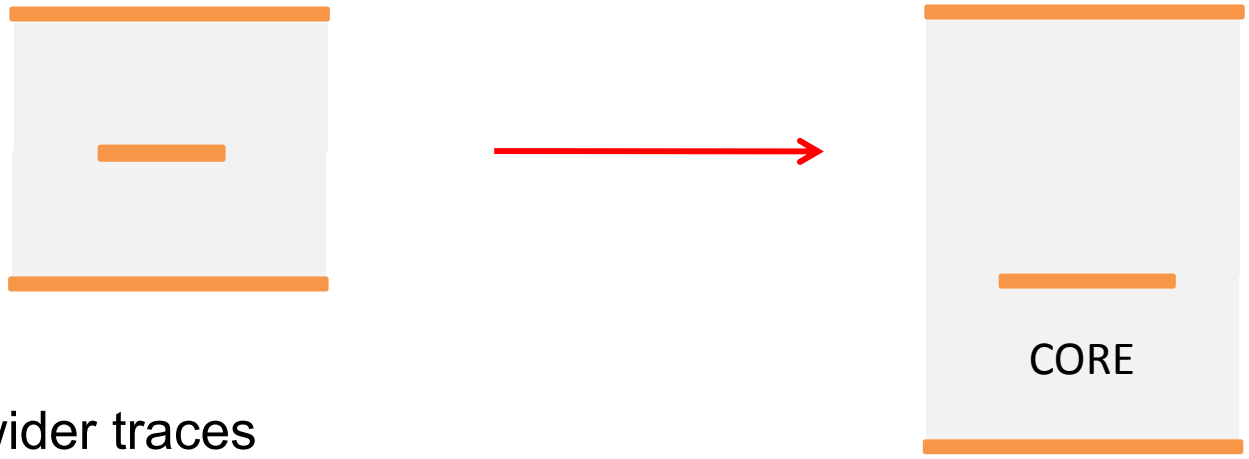
2. - Classic Fixes



1. Use of wider traces
2. Use of thicker materials
3. Use of impedance tapers for coupled lines so that long runs may be wider
4. Sorting and manual selection of materials
5. Reliance on “core” (laminate) materials for better thickness control

But thicker boards cause issues for fine pitch and for supply decoupling.

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3. Emerging Tech - Drill then Press Technology

(1) Drill and plate all cores and pre-pregs

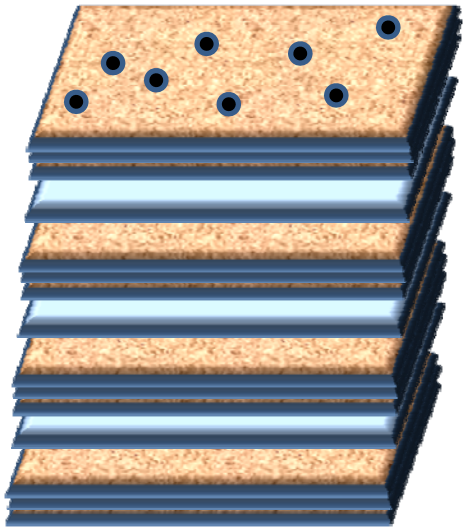
core

Pre-preg (Single ply)

core

(2) Fill pre-pregs holed with conductive "ink"

(3) Press



Allows for much thicker boards with fine pitches

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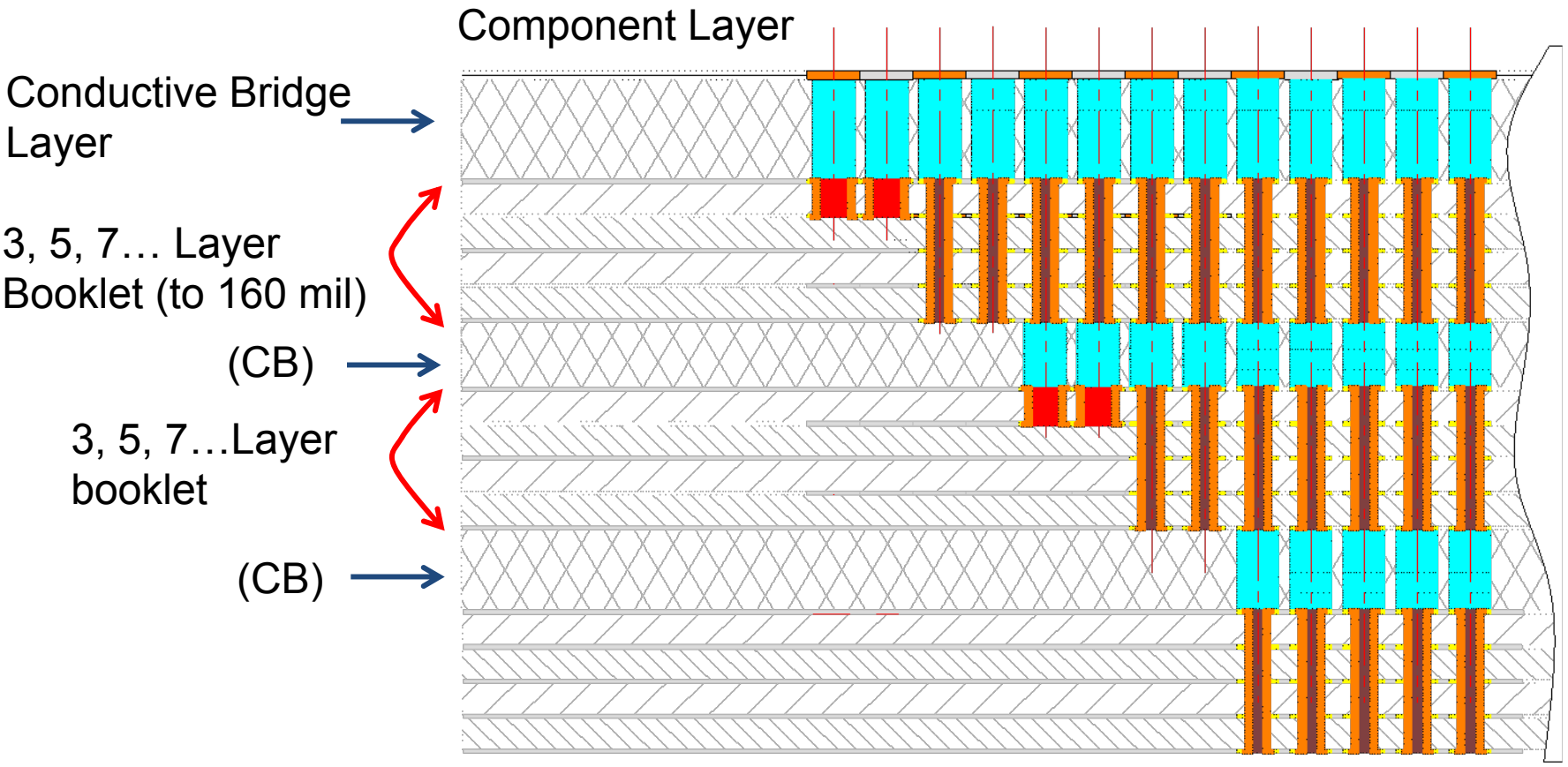
3. Emerging Tech - Conductive Bridge Technology™



Why? Better impedance control, lower loss lines

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3. Emerging Tech - Impedance controlled vias

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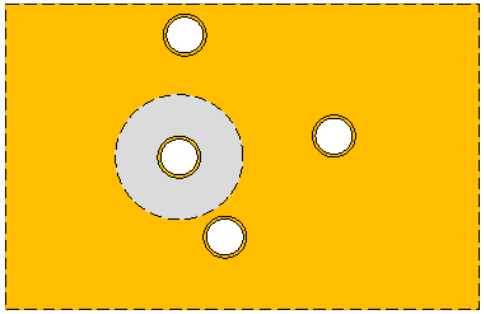
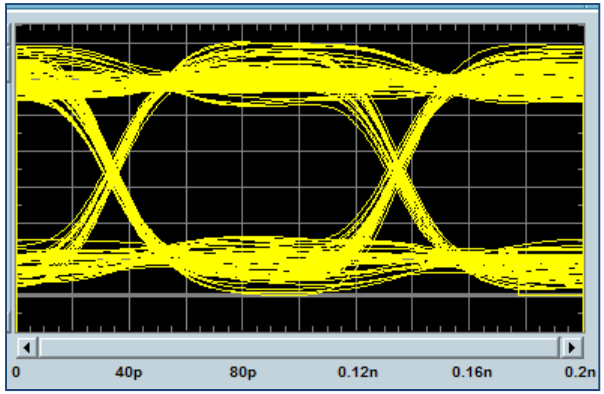
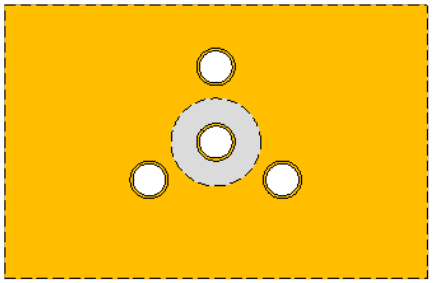
ANTI-PAD ADJUSTMENT ONLY

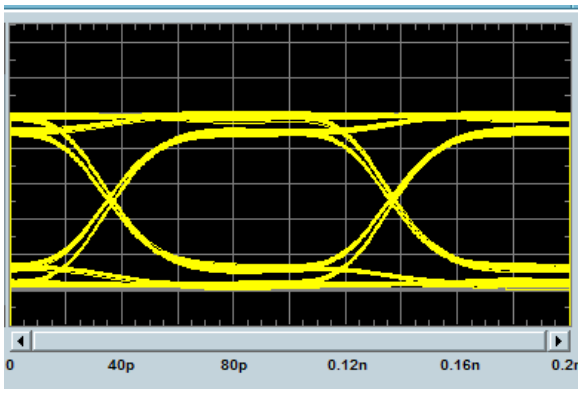




ANTI-PAD ADJUSTMENT ONLY DATA EYE
10 Gbit/sec

ANTI-PAD ADJUSTMENT WITH 3 SYMMETRICAL GND VIAS





SURROUND GROUND VIA DATA EYE
10 Gbit/sec

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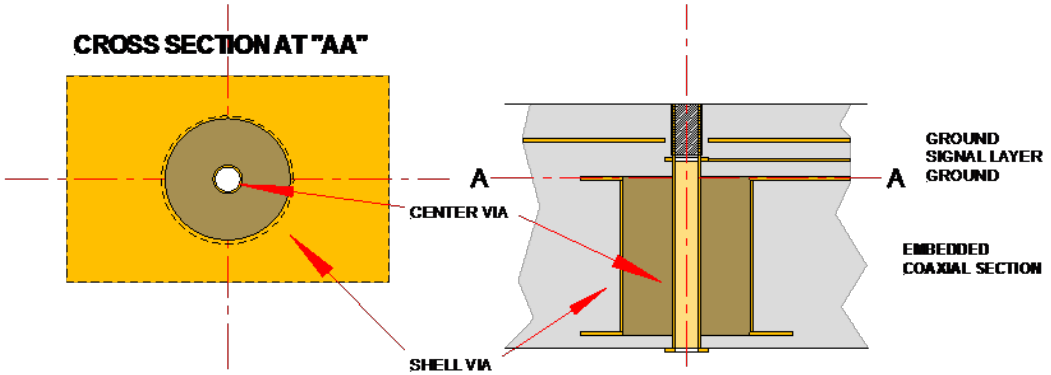
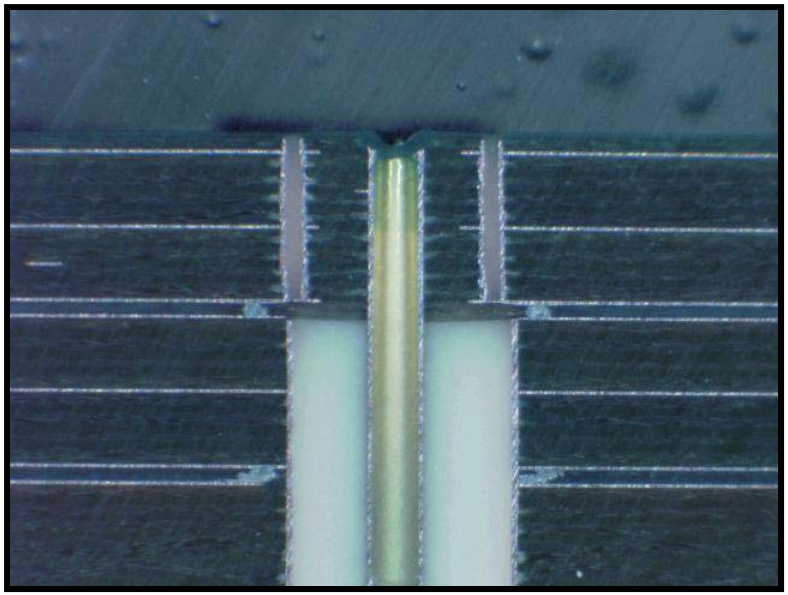
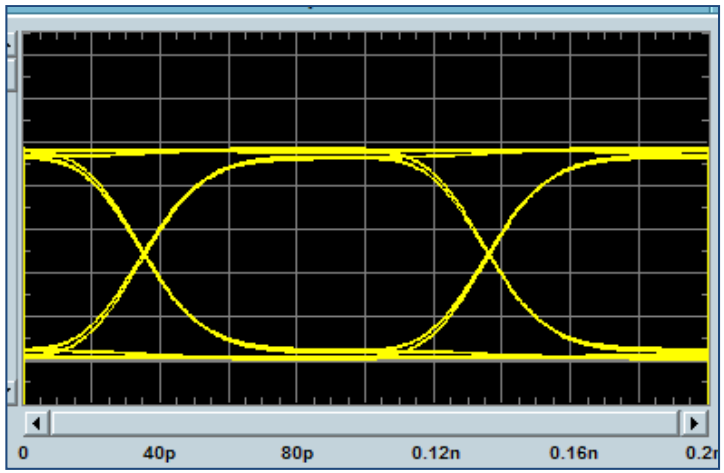
3. Emerging Tech - Coaxial Via







EMBEDDED COAXIAL VIA: 10 Gbit/sec

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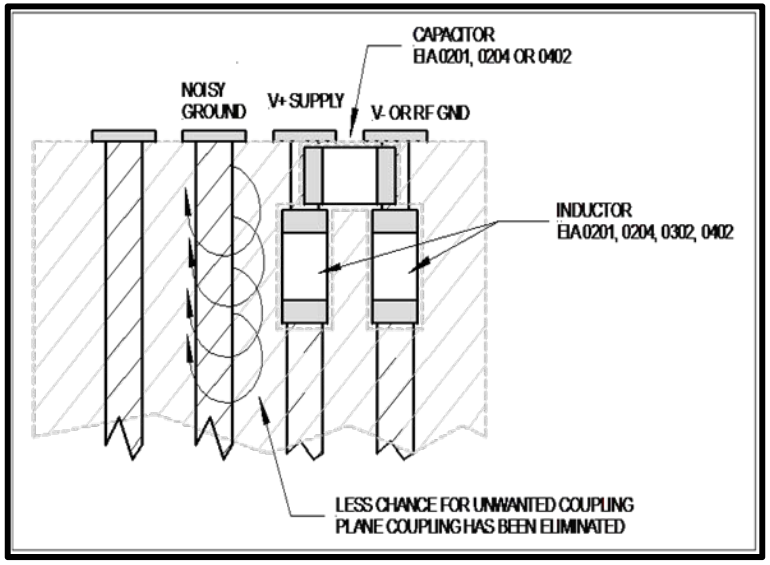
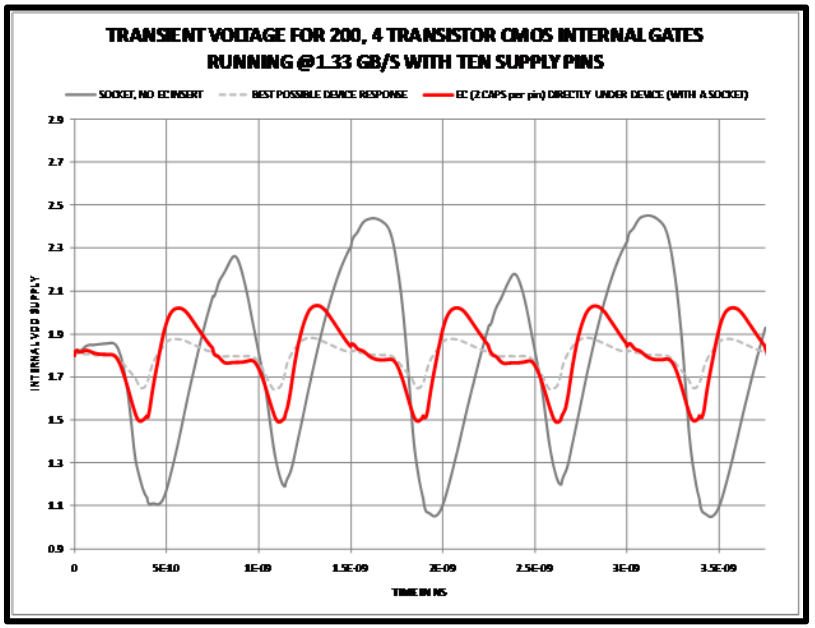
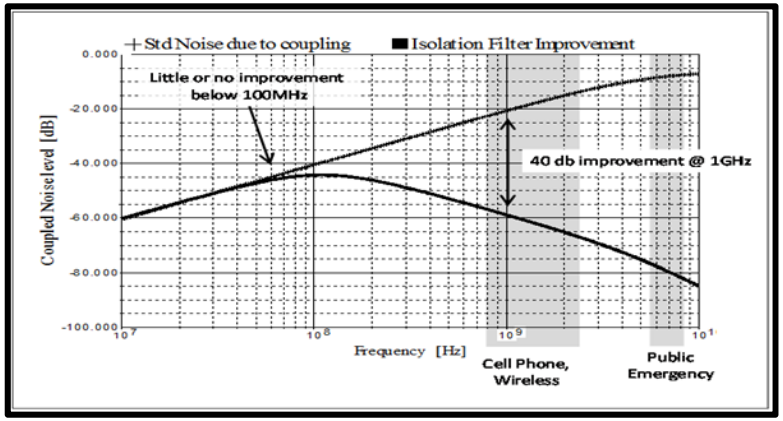
3. Emerging Tech – Embedded Components







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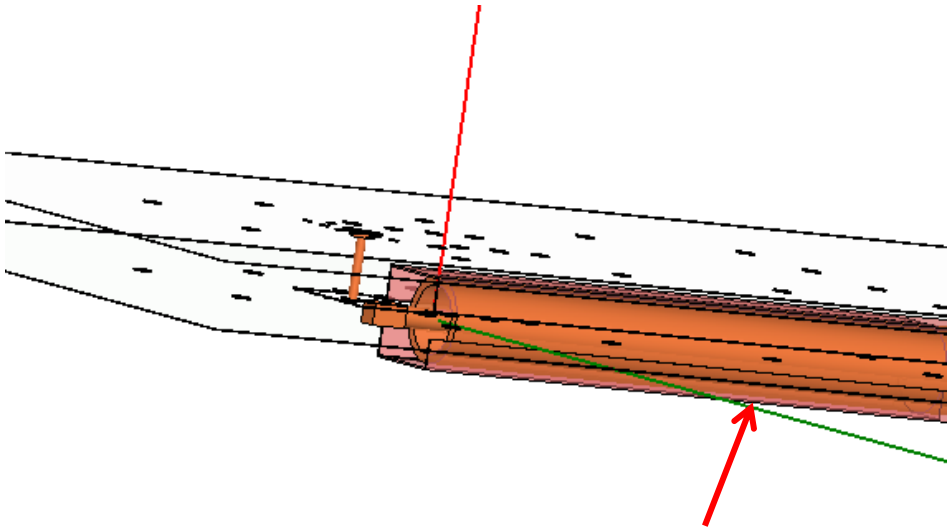
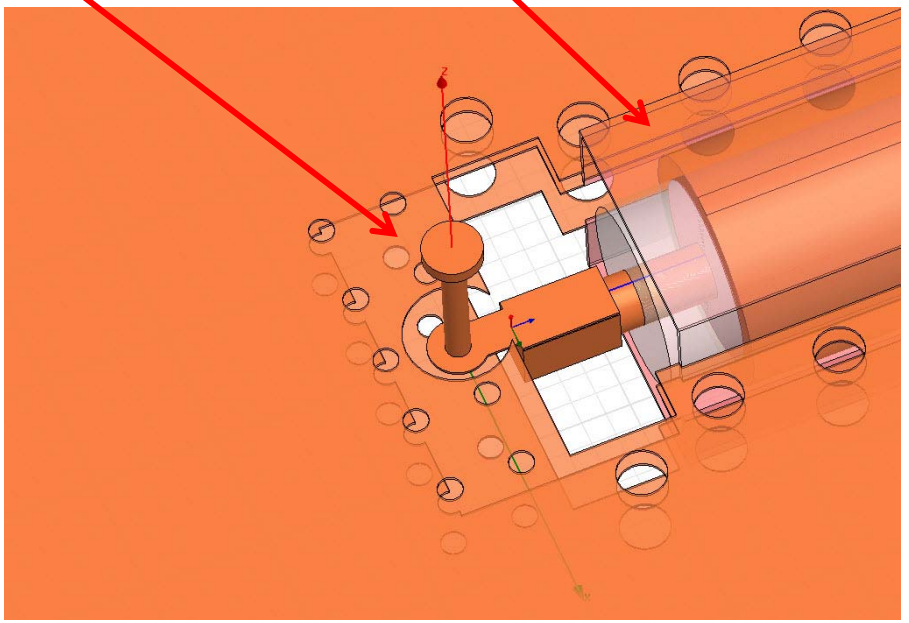
3. Emerging tech - Embedded Coaxial Via



Metal shell for housing coax

Via to BGA grid

Coaxial Structure



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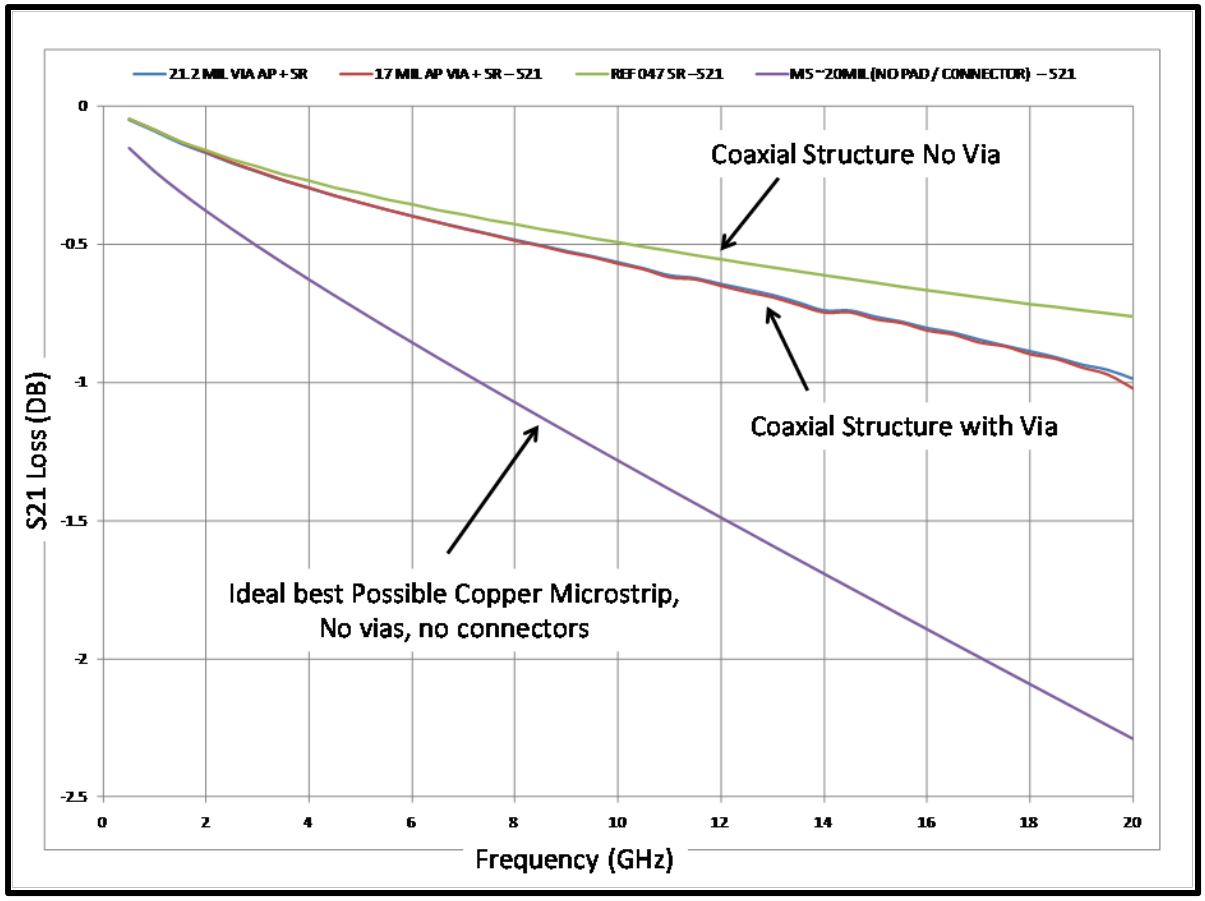
3. Emerging Tech – Embedded Coaxial Structure

IMPROVED LOSS



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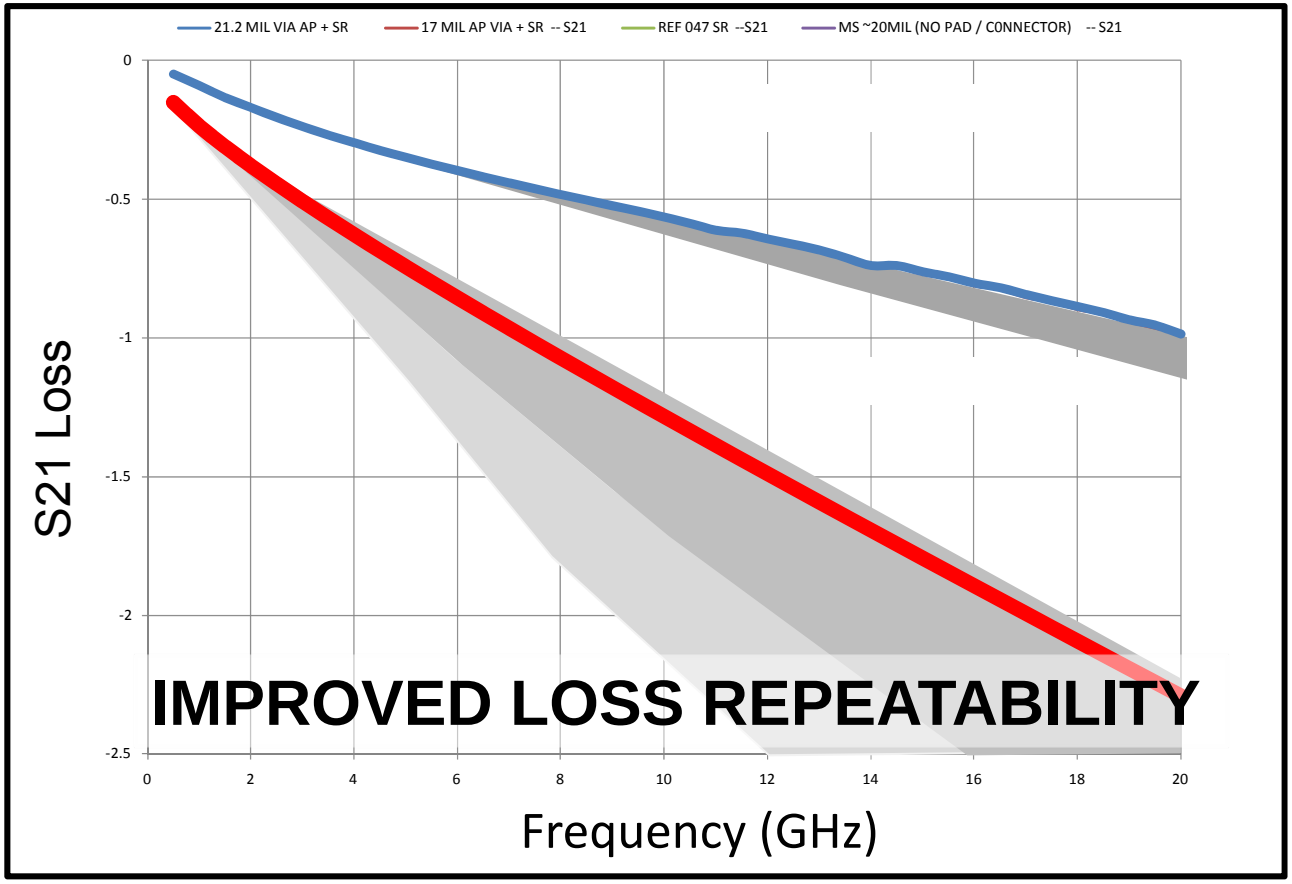
3. Emerging Tech – Embedded Coaxial Structure

A Comparison of S21 Loss Repeatability as a Function of Frequency



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Conclusions

1) As common operating frequencies get faster and faster, practical issues in pc board fabrication become more of a problem. The key seven known issues discussed are:

   a) Etch Tolerance
   b) Average Material Thickness Tolerance
   c) Within-sheet Thickness Variation
   d) Material Weave and Dielectric Variation
   e) Metal Plate Variation
   f) Regional Variation Within a Board
   g) Copper roughness

The Quest for the Perfect Loadboard Conclusions, con't

2) Emphasis and equalization generally only corrects for "ideal" losses. Thus "loss repeatability" should be the growing concern in high speed testing.

3) Classic fixes help but need newer approaches for fine pitch and supply decoupling.

4) Emerging technologies solve classic fix associated problems but only embedded coaxial structures really addresses loss repeatability issues.