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The Effect of Package Pin Map on Signal Integrity for Test Applications

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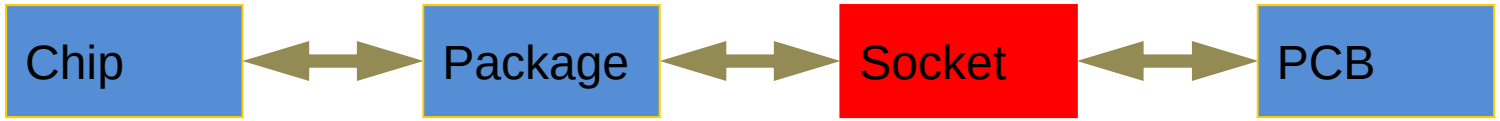
Outline

- Challenges
- Description of the case studies
- Bandwidth data
- Discussion
- Summary
- Future work

Challenges

- Package design is more challenging than ever due to faster IC (integrated circuit) speeds
- SI (signal integrity) analysis has become a crucial step of the package design
- The system level SI analysis is the best practice to ensure design success
  - Final product system:

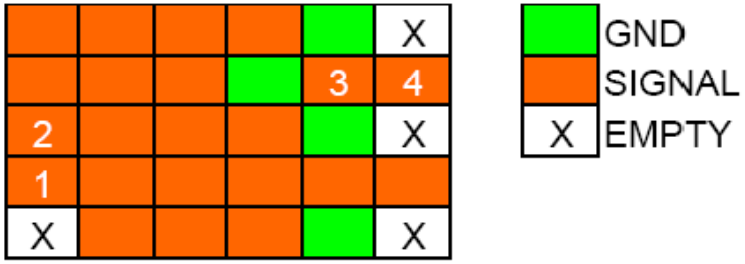
  - Package test system:



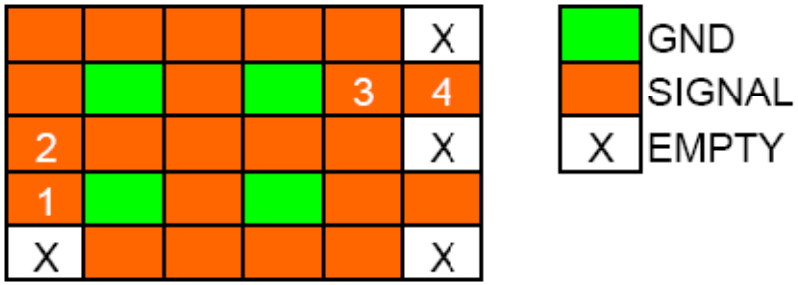
- The system level analysis for final product is often conducted by system design engineers
- The system level analysis for package test is seldom conducted
- Signal degradation caused by socket compromises system performance in package test applications
- Package design aspects such as pin map has significant effect on the SI performance of the sockets

Description of the case studies

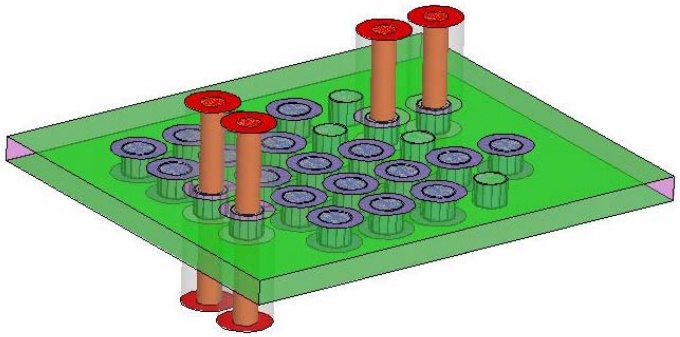
- Case 1, a real package pin map of a customer's product:



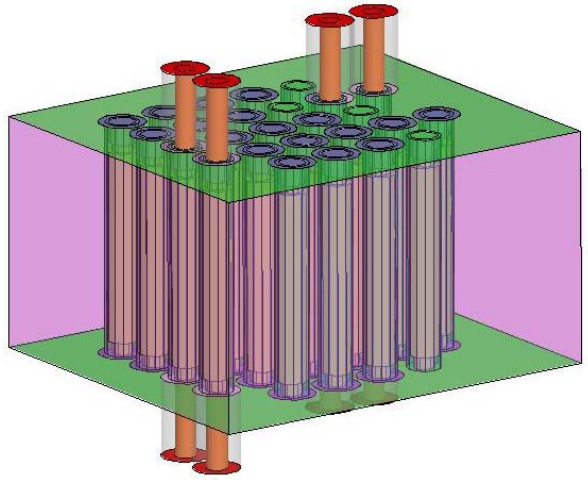
- Case 2, a revised pin map to improve the SI performance:



- Ansoft HFSS model setup
  - 1 mm pitch BGA, 0. 4 mm ball height and 0.5 mm ball diameter
  - Co-axial waveports
  - 0.6 mm contact diameter, various contact lengths from 1 to 4 mm
  - Socket material dielectric constant: 3.5
- Assume -1 dB bandwidth of 5 GHz is required

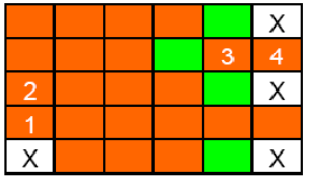


HFSS model of package only

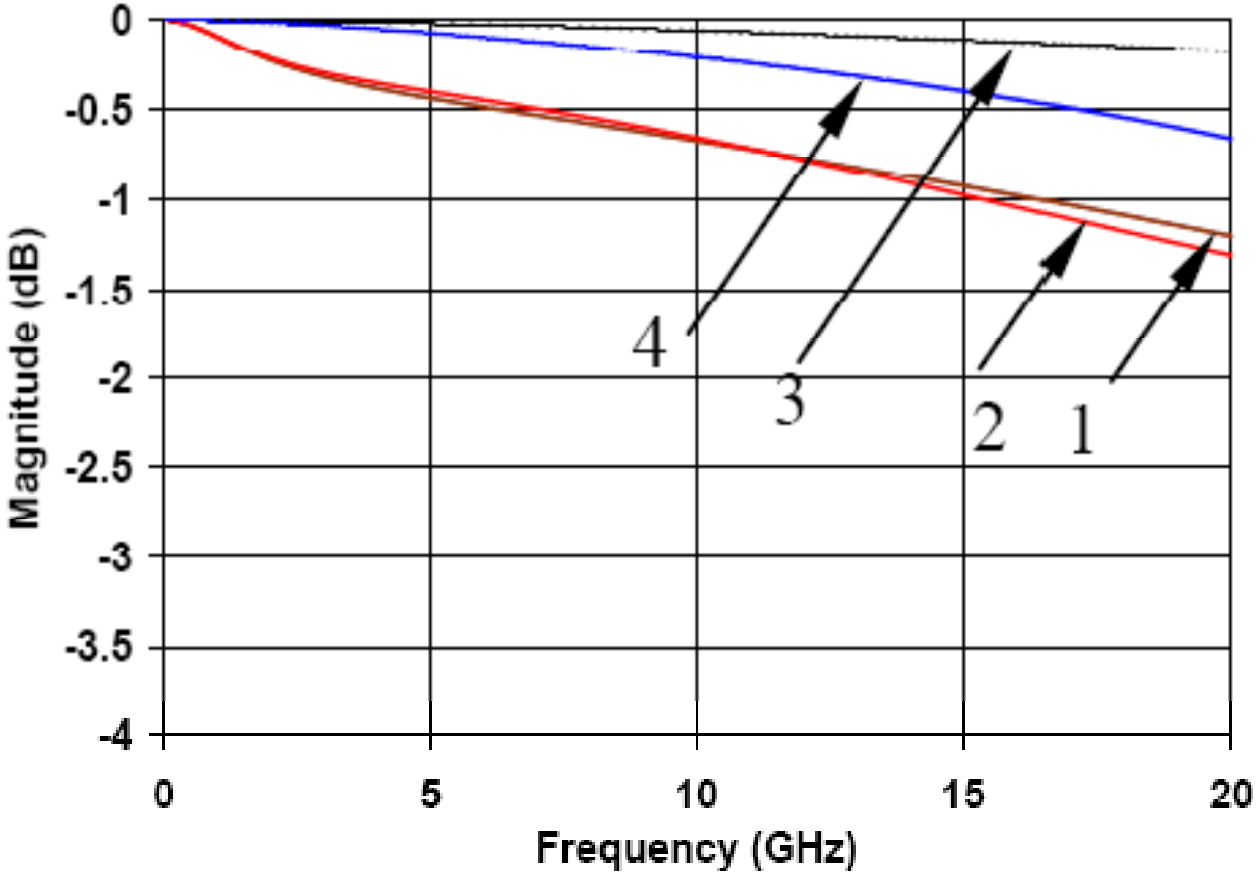


HFSS model of package and socket

Bandwidth data



- Insertion losses of package only (case 1):
  - -1 dB bandwidth over 15 GHz for all pins under study



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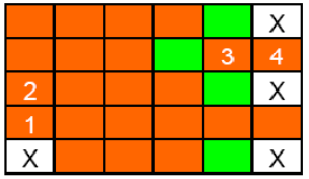
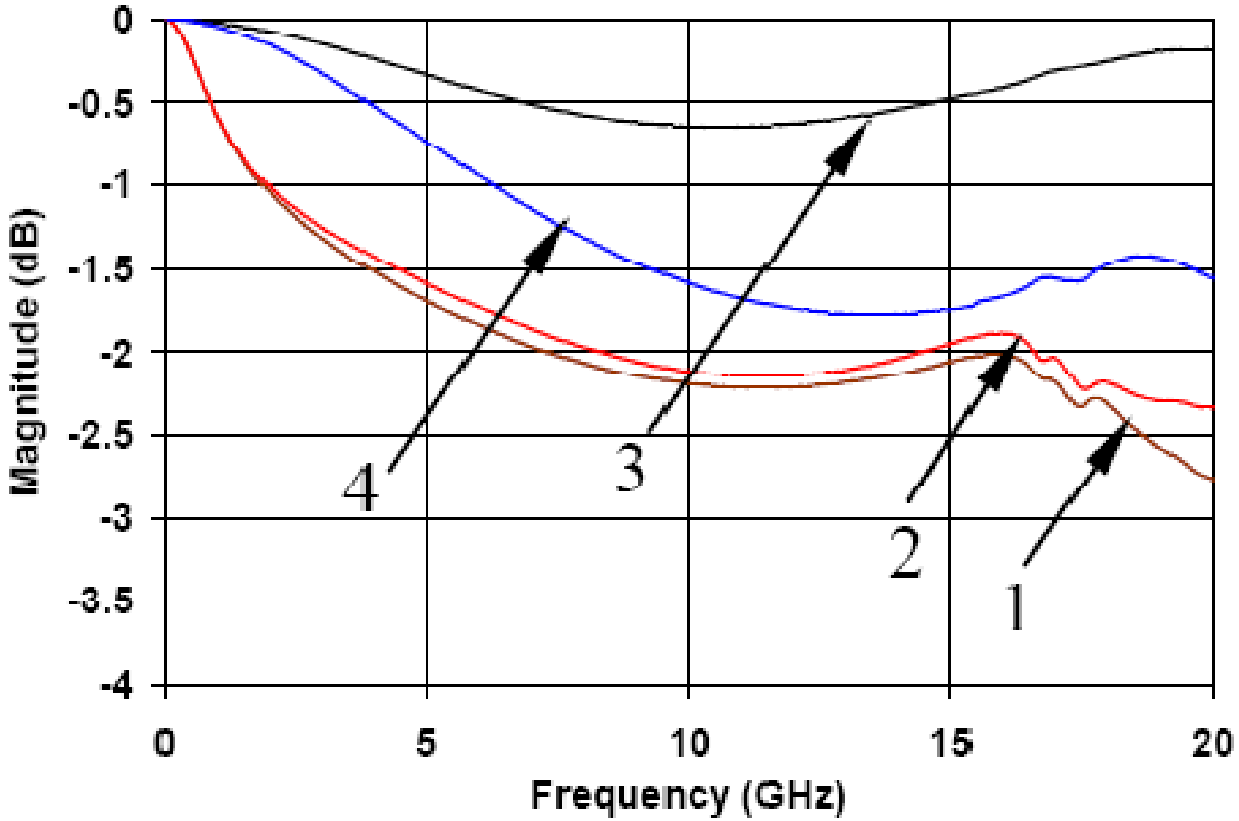
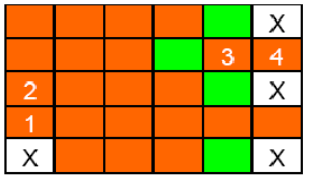
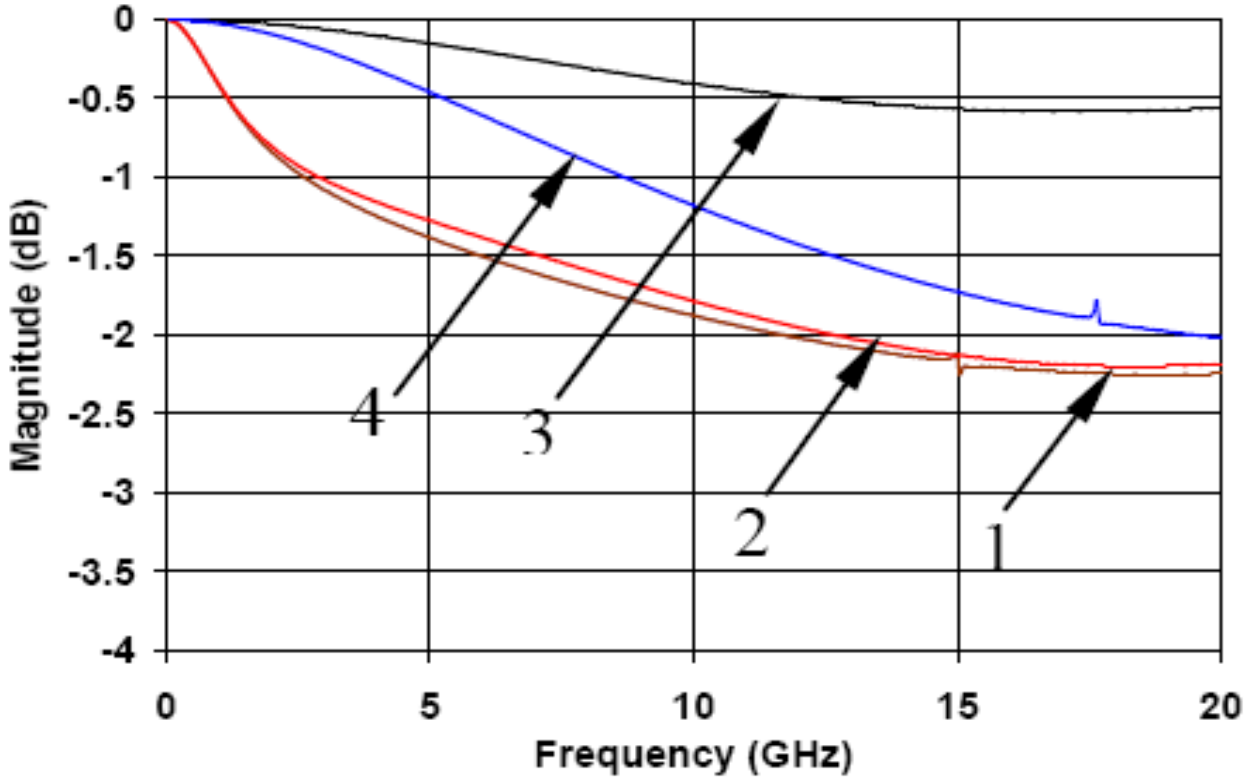


- Insertion losses of package and socket with 4 mm contacts (case 1):
  - -1 dB bandwidths of pin 1 and 2 fail 5 GHz requirement





- Insertion losses of package and socket with 2.5 mm contacts (case 1):
  - -1 dB bandwidths of pin 1 and 2 still fail 5 GHz requirement



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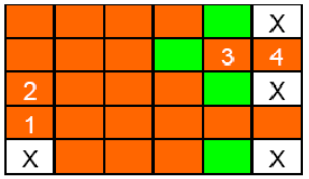
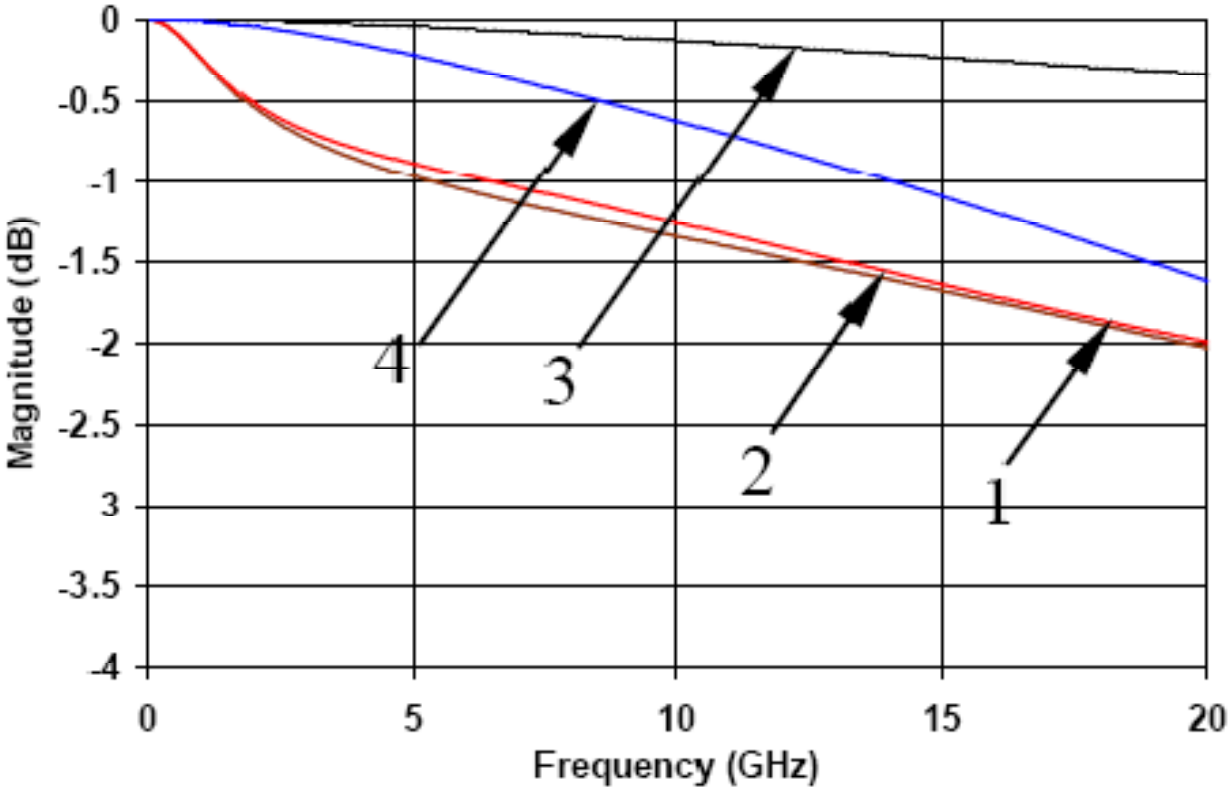


- Insertion losses of package and socket with 1 mm contacts (case 1):
  - All pins meet 5 GHz requirement



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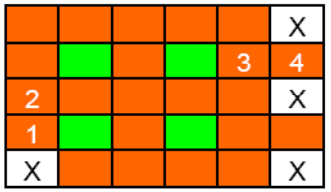
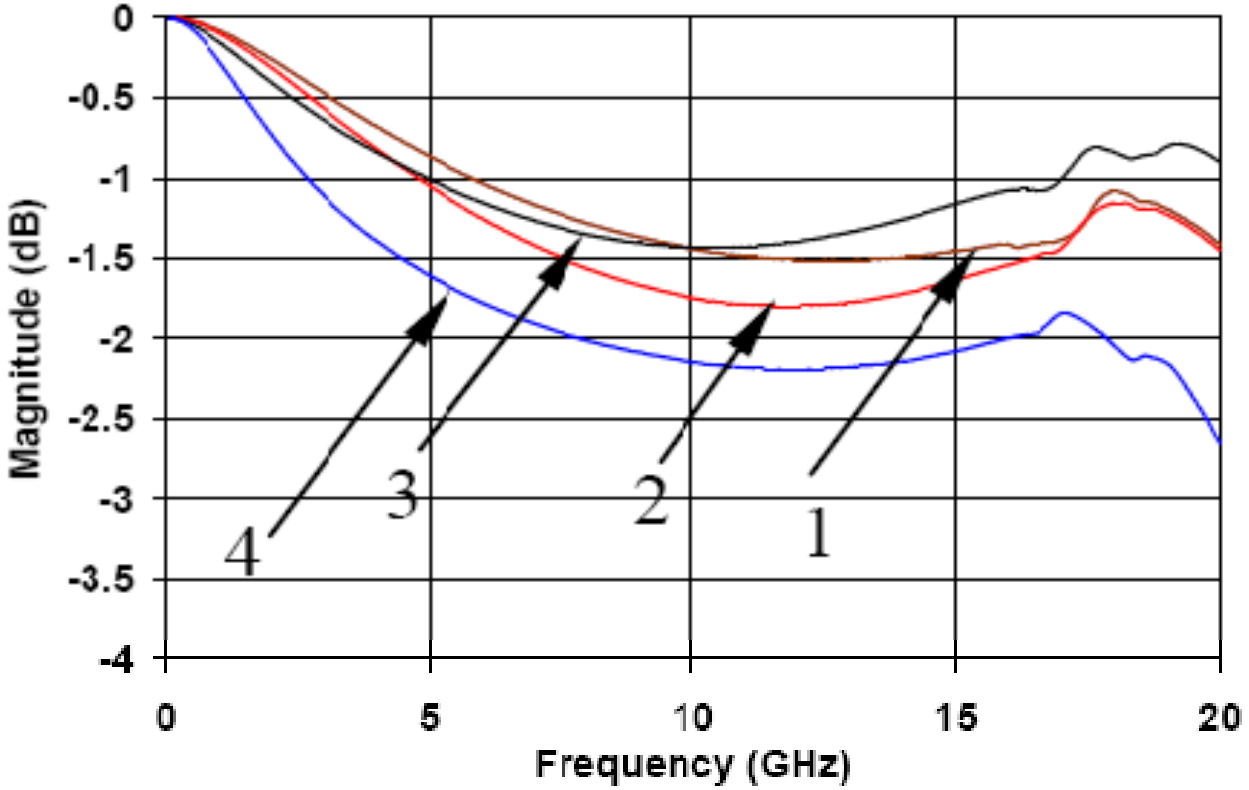
S21 plots



- Insertion losses of package and socket with 4 mm contacts (case 2):
  - Pin 1 and 2 already meet 5 GHz bandwidth requirement
  - Pin 4 has much worse bandwidth in this case



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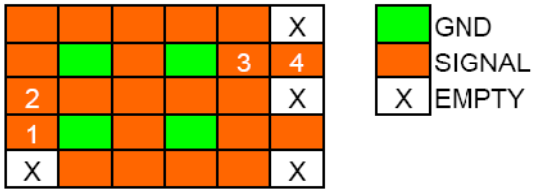
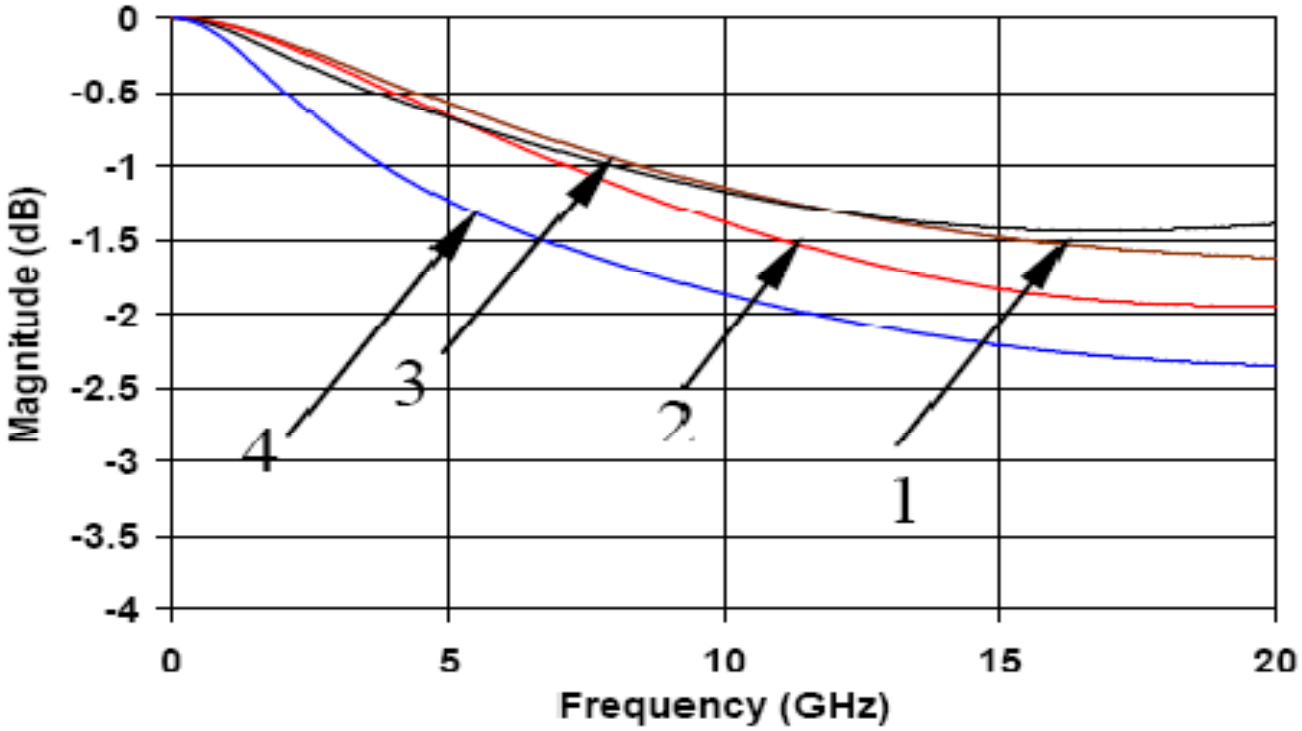
S21 Plots



- Insertion losses of package and socket with 2.5 mm contacts (case 2):
  - Pin 1, 2 and 3 all pass the 5 GHz bandwidth requirement with comfortable margins
  - Pin 4 still fails the requirement



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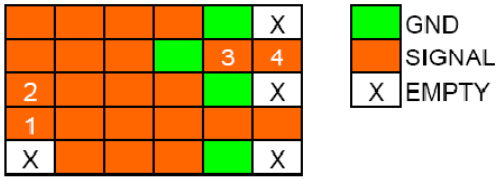
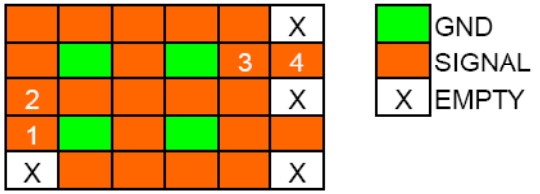
Discussion

- Case 1: The contact length need to be less than 1 mm in order to meet the bandwidth requirement
- Case 2: Except for pin 4, the contact length can be as much as 4 mm to meet bandwidth requirement
  - Adding an extra ground pin at empty location underneath pin 4 will improve its bandwidth beyond the requirement



Case 1



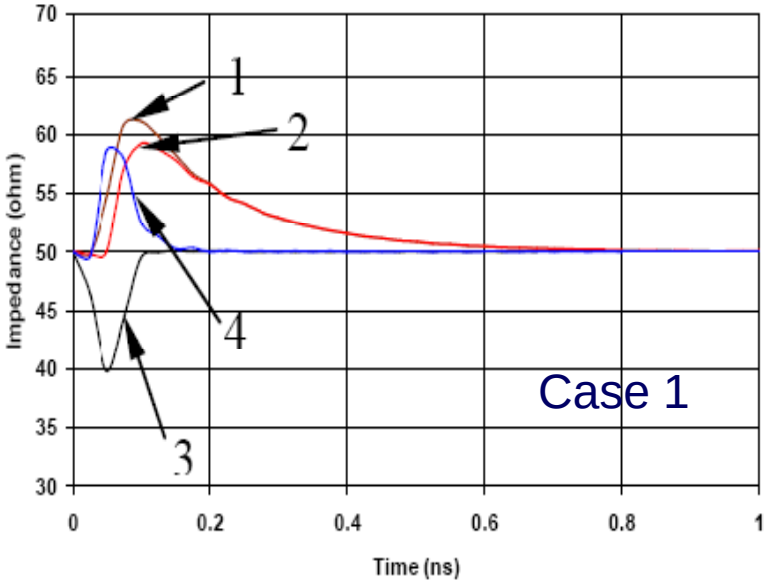
Case 2

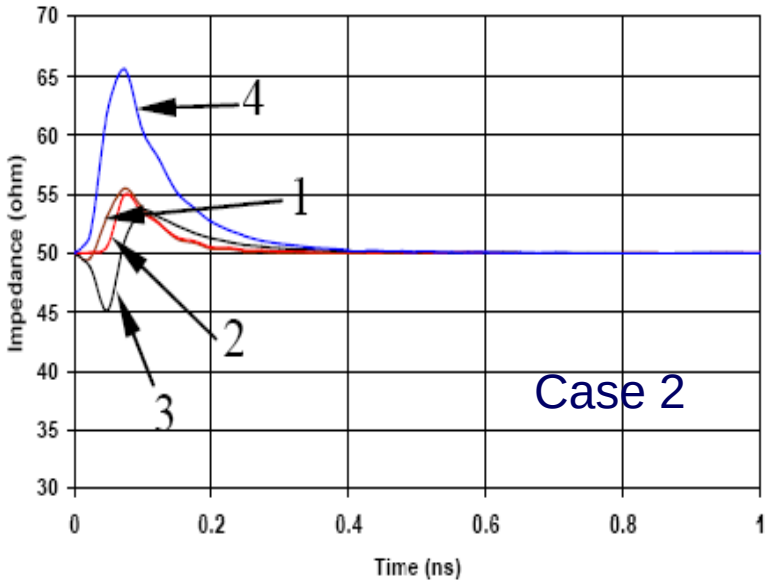
- What caused improvement?
  - Being adjacent to ground pin improves the bandwidth
  - What really changed is the impedance

$$Z = \sqrt{\frac{L}{C}}$$

TDR Impedance Plots

- TDR data:



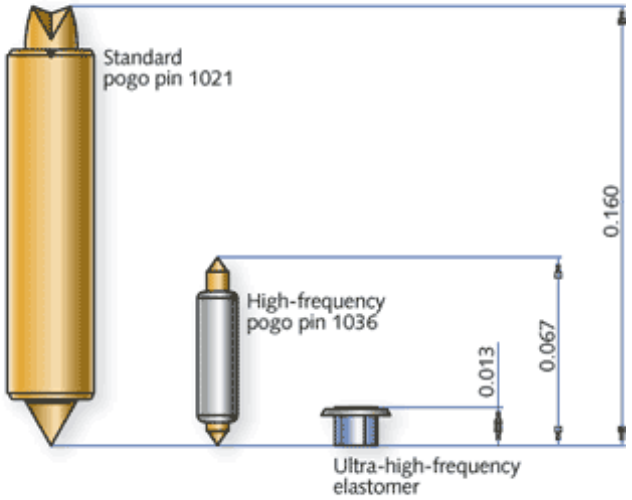


- Reflection coefficient:

$$\Gamma = \frac{Z_1 - Z_0}{Z_1 + Z_0}$$

Contact Length

- What is the significance of the contact length?
  - 4 mm or above contact length can be easily achieved by conventional spring probe technology (low cost, reliable contact, long cycle life)
  - 2.5 mm contact length can be implemented by spring probe technology too (higher cost, less reliable contact, shorter cycle life)
  - 1 mm or below contact length only can be achieved by elastomer or stamping pin technology (poor contact, very short cycle life)



Summary

- Package pin map has major effect on SI performance of the socket
- When impedance mismatch is small, even longer contact length can deliver high signal bandwidth
- It is desirable to have at least one ground pin adjacent to signal pin so the impedance can be better controlled
- For inevitable impedance mismatch caused by package pin map, extremely short contact length is the only way to achieve high bandwidth
- Shorter contact length increase the overall cost for test

Future work

- The effect of the package design on signal integrity for test application is only limited on signal bandwidth in this presentation
- The effect of the package design on power delivery network is also very crucial, need to be investigated in the future
- Some important aspects for power integrity study:
  - Package stack up designs
  - Total number of power and ground pins
  - Decoupling scheme on package