Control of Clock Jitter in High Speed Data Links

Tsunwai Gary Yip
Rambus Inc. Sunnyvale, California USA
www.rambus.com

***Abstract* — Fast data links require a low phase noise reference clock. An alternative is to reduce the noise of a low cost clock part using the band pass filtering inherent to the clocking architecture in the link. This study has a two-fold objective: to verify clock noise filtering in a 16 Gbps data link, and to prove the degree of filtering is adjustable. Two measured band pass filters are presented. Clock jitter reduction can be achieved by narrowing the difference in the loop bandwidths of the Tx PLL and Rx PLL, and by setting the band pass filter at the noise floor of the reference clock. Therefore, 16 Gbps data links can be designed to filter the reference timing signal, eliminating the need for a clean, expensive clock source.**

I. INTRODUCTION

The increasing speed of data links continues to drive the need for low cost, low jitter clock sources. Presently the noise floor of the reference clock source for some 5 Gbps links is around -138 dBc/Hz [1]. While such low cost clock parts are already available in high volume, cleaner clock sources will be needed to support 10 Gbps or faster data links unless alternatives, such as the control or reduction of reference clock jitter at the system level, are available.

The clocking architecture of a data link often includes measures to control or reduce jitters in the clock signal. When a clock signal passes through two PLLs in cascade, jitter amplification can be prevented by maintaining a sufficiently large difference between the loop bandwidths of the PLLs [2].

In some data link architectures, such as the XDR™ memory system, jitter of the reference clock is reduced. The clock signal propagates through the transmitting and receiving PLLs via different paths. Clock jitter is significantly reduced by an effective band pass filter resulted from the difference in the loop bandwidths of the two PLLs. The incomplete cancellation is also due to a mismatch of the propagation delay time through the two paths [3].

This paper focuses on the reduction of reference clock noise. Following an introduction of the noise sources in a data link will be a description on the mechanism of clock noise reduction. Data from a study of 5 Gbps links will be used to show the impact of the phase noise of the reference clock on the performance of the links.

The random jitter requirements of a 16 Gbps link will be presented along with the analytical results on clock jitter reduction by a large and a small band pass filters. The last part of this paper presents the detection of the band pass filter inherent to the link architecture, and the data of two band pass filters.

II. SOURCES OF PHASE NOISE IN A DATA LINK

The data and clock paths shown in Figure 1 include the major components which contribute to the random jitters in most high speed data links. Examples of link architectures that fit the description in Figure 1 include Rambus' XDR memory systems and FlexIO™ interfaces.

The random jitter in the received data stream is primarily due to the phase noise from the reference clock source, the PLL in the data transmitting device (Tx PLL) and the PLL in the receiving device (Rx PLL). Other components such as the driver and receiver circuits introduce significantly less jitter.

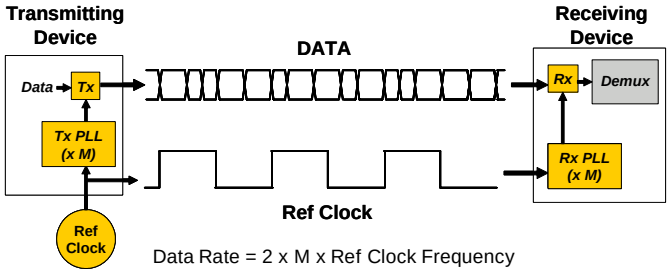

Figure 1: Sources of phase noise in a data link.

III. REDUCTION OF CLOCK JITTER

Phase noise originated at the clock source is carried by the reference clock signal along the data and reference clock paths to the Tx PLL and Rx PLL. The PLLs are low pass filters with different loop bandwidths. They reduce the high frequency jitter components in the clock signal to different extents. The remaining low frequency jitters are partially cancelled in the receiving device after the Rx PLL. Therefore, the link architecture effectively reduces the clock noise by band pass filtering. The amount of clock noise in the received data stream depends primarily on the following three factors:

- Phase noise of the reference clock source,
- Loop bandwidth of the Tx PLL, and
- Loop bandwidth of the Rx PLL.

A CDR may be present in a data link. When the high pass filter bandwidth of the CDR is low compared to the bandwidth of the PLLs, the PLLs are still the primary filters of the high frequency clock jitters. The bandwidths of the CDR in some popular data links are around 1.5 MHz, while the Tx PLL and Rx PLL bandwidths are between 8 MHz and 16 MHz. The amount of jitter filtered by the CDR is relatively very small.

The data links studied in this paper do not have any CDR. The PLL bandwidths are around 20 MHz and higher. Therefore the results in this paper are useful for understanding clock jitter reduction in data links which have a relatively low bandwidth CDR.

IV. Impact of Reference Clock Noise on Data Window

A series of experiments were performed to observe the effect of reference clock noise on the data window of an 8-bit wide 5 Gbps/pin interface. Nine different levels of phase noise, between -132 and -93 dBc/Hz, were added to the 500 MHz reference clock. Each of the eight links was delivering data in a clock pattern at 5 Gbps.

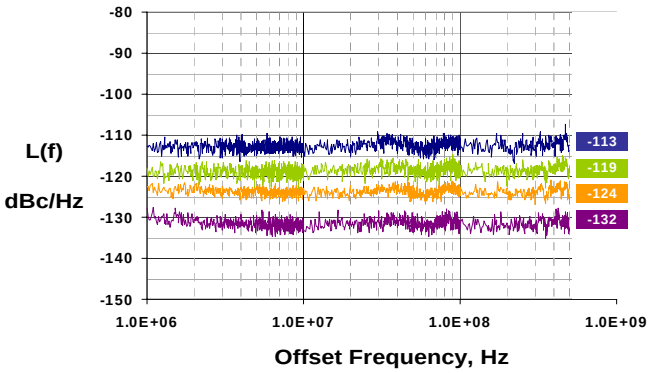

Figure 2: Four phase noise profiles of a 500 MHz reference clock.

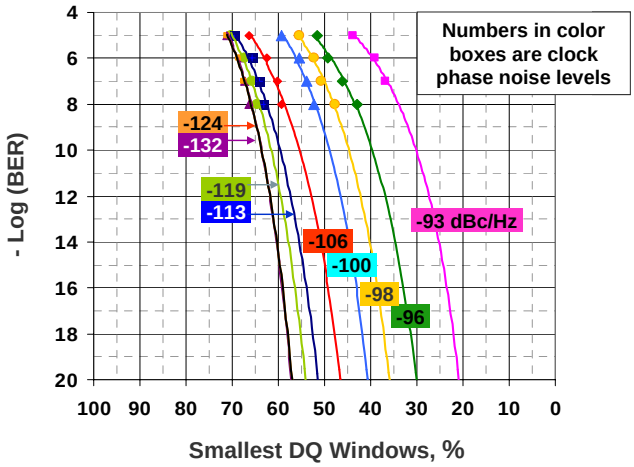

Figure 3: Impact of clock phase noise on data window.

Figure 2 shows four of the nine clock phase noise profiles used in the experiments. The lowest level was -132 dBc/Hz and the highest -93 dBc/Hz. The smallest data windows among the 8 links are reported in Figure 3. Using 50% UI at BER 10-20 as the criteria for passing, phase noise of the reference clock cannot exceed -113 dBc/Hz. Decreasing the noise level to -124 dBc/Hz improves the data window by about 5.5%.

Figure 3 also illustrates the fact that the intrinsic noise of the Tx PLL and Rx PLL can limit the improvement from lowering the phase noise of the reference clock. At -124 dBc/Hz, the DQ window was improved to 57.5%. There was no observable improvement when the noise level was further decreased to -132 dBc/Hz. This is because the amount of jitter due to the intrinsic noise of the PLLs [4] was large enough to mask out the residual clock noise in the 5 Gbps links.

V. Estimating Random Jitters of a 16 Gb/s Link

The above description of the process for creating a characterization environment is transparent to the user and does not require any user input. The test features are available in the LabStation GUI and also accessible during automated testing using commands written in LsScript.

The study of 5 Gbps data links in the previous section suggests that both the reductions of PLL intrinsic noise and reference clock noise are required for data rates beyond 10 Gbps. The RMS random jitter of each PLL (RJ_{TxPLL}, RJ_{RxPLL}) in the 5 Gbps links was around 2.5 ps. This section presents an estimate of the random jitters for the components in a 16 Gbps or faster data link.

In the timing budget of a data link, the random jitter of the link (RJ) is assigned a certain percentage of the bit time or UI. At 16 Gbps, the bit time is 62.5 ps. If the random jitter of the link is assigned 30% UI,

$$RJ = 30\% \times \text{Bit Time} = 0.30 \times 62.5 \text{ ps} = 18.75 \text{ ps}$$

For the bit error rate of 10-20, RJ is 18.53 times the RMS random jitter of the link, $RJ_{Link,\,RMS}$. Therefore,

$$RJ_{Link,\,RMS} = 18.75 / 18.53 \sim 1 \text{ ps}$$

This result implies the random jitter of each of the link components must be less than 1 ps. $RJ_{Link,RMS}$ can be approximated by the following equation:

$$RJ_{Link,RMS} = [RJ_{TxPLL}^2 + RJ_{RxPLL}^2 + RJ_{CLK}^2 + RJ_{Tx}^2 + RJ_{Rx}^2]^{1/2} \quad (1)$$

where RJ_{CLK} is the RMS random jitter due to the residual phase noise of the clock after band pass filtering. This term is dependent on the loop bandwidths of the PLLs and the phase noise of the reference clock signal. When RJ_{Tx} 2 and RJ_{Rx} 2 are small compared to the other terms, Equation (1) becomes

$$RJ_{Link,RMS} = [RJ_{TxPLL}^2 + RJ_{RxPLL}^2 + RJ_{CLK}^2]^{1/2} \quad (2)$$

For the purpose of estimating the order of magnitude, the three terms on the right side of Equation (2) are assumed to be equal. The RMS random jitter resulted from the intrinsic noise of the PLLs and the residual clock phase noise is roughly 0.6 ps each.

Figure 4 shows graphically that the bit error rate will rise as the data rate increases. In all the cases $RJ_{Link,RMS}$ is fixed at 1 ps and RJ equal to 30% of the link budget. As the data rate increases from 16 to 19.2 Gbps, the bit error rate increases from 10-20 to 10-14. This means that the random jitters of the components need to be less than 0.6 ps for links operating at faster than 16 Gb/s and BER below 10-14. References [5] and [7] have presented PLLs with sub-picosecond random jitter for 16 Gbps data rate. This paper focuses on the reduction of reference clock jitter.

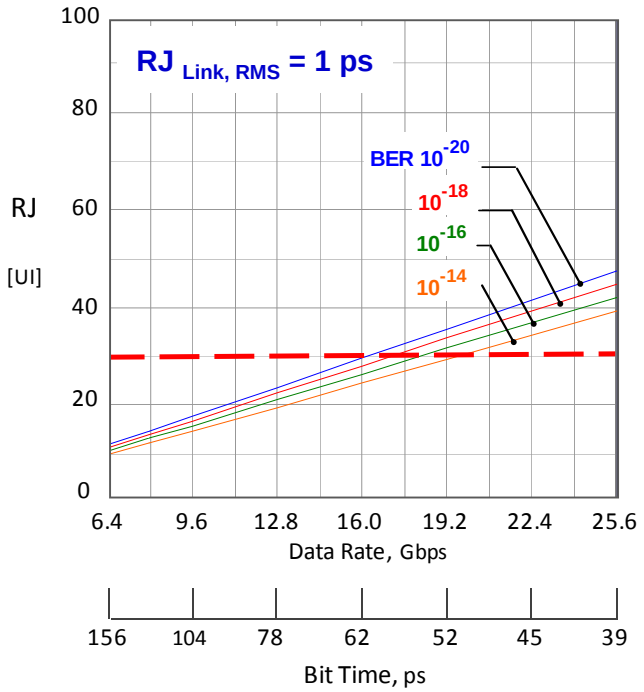

Figure 4: Impact of data rate on bit error rate for $RJ_{Link,RMS}$ = 1 ps and RJ = 30% UI.

VI. A Model of Clock Jitter Propagation

The data and reference clock paths described in Figure 1 can be used to construct a phase jitter propagation model for the reference clock shown in Figure 5. The clock jitter in the received data stream depends on

- Phase noise profile of reference clock,
- Transfer function of Tx PLL, H_{Tx} ,
- Transfer function of Rx PLL, H_{Rx} , and
- Difference in propagation times along the data and clock paths, T_d.

The input of the transfer function is the phase noise profile of the reference clock. The output is the residual clock phase noise. The effect of H on the input noise is like that of a band pass filter as shown qualitatively in Figure 5.

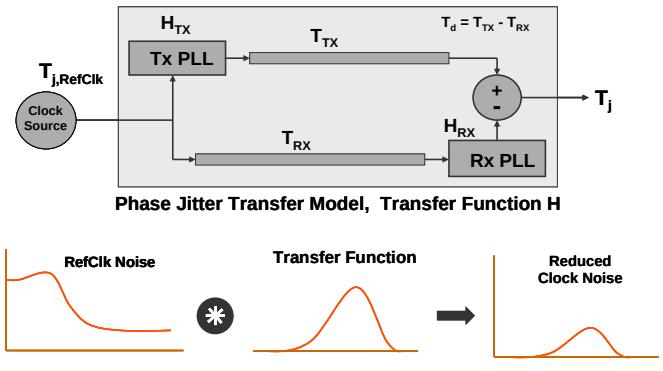

Figure 5: A model of clock jitter propagation.

Treating the two PLLs as second order linear devices [4], the band pass filters are calculated for two different combinations of Tx PLL and Rx PLL loop bandwidths. Peaking is assumed to be 3 dB and Td 1 ns.

The red filter in Figure 6 is for the loop bandwidths of 15 MHz and 20 MHz, the blue filter for 15 MHz and 30 MHz. Larger difference in loop bandwidth results not only in a wider band pass filter, but also gain at some frequencies. Therefore, programmable PLL loop bandwidths are necessary for controlling the degree of noise reduction, and adjusting small enough differences in the LBWs to avoid gain.

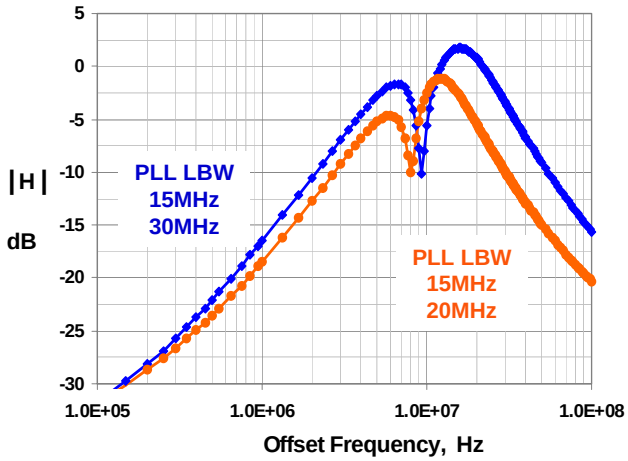

Figure 6: Band pass filters for two pairs of Tx PLL and Rx PLL loop bandwidths.

VII. Clock Jitter Reduction by Adjusting PLL LBWs

A. Phase Noise of Reference Clock

The reduced RMS random clock jitter, RJCLK, can be determined by applying the transfer function H of the jitter propagation model to the phase noise of the reference clock. Figure 7 is a typical phase noise profile with a -138 dBc/Hz [1] noise floor on the right portion of the curve.

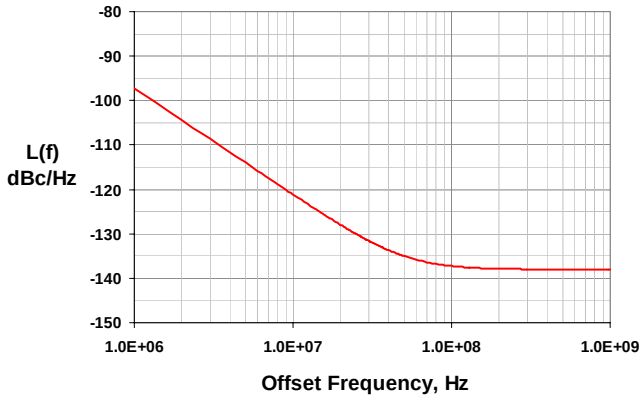

Figure 7: A typical phase noise profile of reference clock source.

B. Adjusting the Loop Bandwidths of Tx PLL and Rx PLL

There are two steps in adjusting the loop bandwidths to reduce clock jitter. First, minimize the difference between the

LBWs of the Tx PLL and Rx PLL to make the effective band pass filter narrower. Second, put the filter as close to the noise floor of the clock as possible to reject the stronger jitter components at the low frequencies. In the following analysis, the position of the filter is defined by the mid-point between the LBWs of the two PLLs. This point is called the nominal LBW of the band pass filter herein. Figure 7 is the reference clock noise profile for calculating the reduced random clock jitter.

The numerical results in Figure 8 suggest that the reduced random clock jitter (RJ_{CLK}) will decrease as the nominal LBW of the band pass filter moves to the higher frequencies. This trend is true for both filters used in this analysis and for clocks having noise profiles similar to Figure 7. For a given threshold value of RJ_{CLK}, the smaller filter is allowed a wider range of nominal LBWs, while the large filter is limited to the nominal LBW at high frequencies. That means the Tx PLL and Rx PLL must have faster LBWs if the minimum of their LBW difference is large.

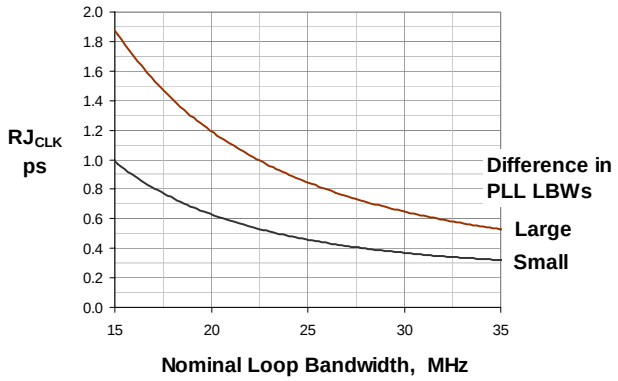

Figure 8: Reduced RMS random jitter of a 500 MHz reference clock for different band pass filters.

VIII. Detecting Band Pass Filter of a Data Link

When sinusoidal jitter of a known frequency is injected into the reference clock, it may partially appear in the received data stream if its frequency is within the pass band of the filter. Here data window in %UI is the signal quality matrix for detecting the filter.

The measured data windows of a 5 Gbps data link for a range of jitter frequencies are shown in Figure 9. The nominal window with no added jitter was at 83% UI. When a low frequency sinusoidal jitter (e.g. 1 MHz or less) was injected, the data window was closed to or slightly less than 83%. This process was repeated for a number of frequencies up to 130 MHz. The data shows that the peak of the band pass filter is between 50 and 60 MHz where the injected jitter causes the biggest drop in %UI.

Experiments were also performed on parallel data links. The jitter source was a toggling data pattern from another link. Figure 10 presents the %UI of an 8-link interface when the injected noise was a toggling data stream at 156 Mb/s. The data show that the responses of the links are different. The evaluation of the interface should be focused on the link which suffers the biggest drop in %UI and the link that has the smallest %UI.

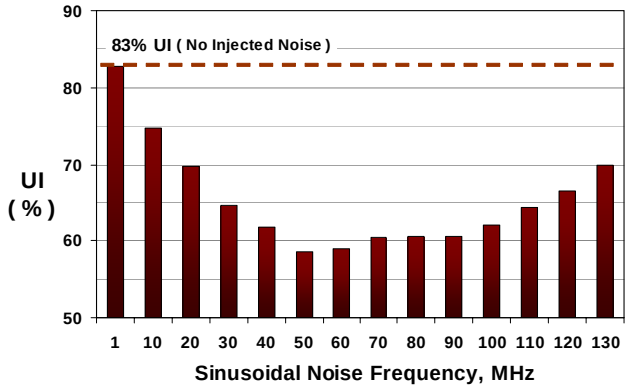

Figure 9: Data window in UI% of a 5 Gbps link for 1 to 130 MHz sinusoidal jitter added to the reference clock signal.

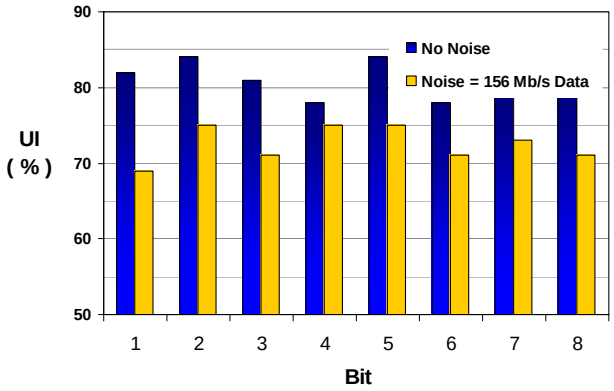

Figure 10: Data window in UI% of an 8-bit interface when the added jitter is a 156 Mbps toggling data stream.

IX. Band Pass Filters of a 16 Gb/s Data Link

Two band pass filters of a 16 Gbps data link have been measured using the approach of sinusoidal jitter injection described above. The data link includes a controller which has two PLLs in cascade. The other end of the link is an emulated DRAM with a LC PLL.

When the 500 MHz reference clock enters the controller, it is routed to a LC PLL which in turn outputs an intermediate clock signal to a ring PLL. The resulting clock signal is at 8 GHz. In the emulated DRAM, the LC PLL multiplies the reference clock by a factor of 16 to 8 GHz. More information about the architecture and circuit of the data link can be found in references [5], [6] and [7].

Since the LC PLL in the controller has a slower loop bandwidth, it is the primary low pass filter for the phase noise of the reference clock. Its transfer function and that of the LC PLL in the emulated DRAM together form an effective band pass filter for the reference clock that drives the data link.

Experiments were performed to observe the change in the data windows when jitters of various frequencies were injected. The measurements together form a normalized band

pass filter as shown in Figure 11. In the first experiment, the difference in the loop bandwidths of the Tx PLL and Rx PLL was large, producing the red band pass filter in Figure 11. In the second experiment the loop bandwidth of the Tx PLL was set to a higher frequency, thus narrowing the pass band. The data windows increased in %UI because more of the injected jitter was filtered. The resulting band pass filter is shown in blue in Figure 11. The data support the fact that the architecture of the 16 Gbps data link is effective in reducing reference clock jitter. The amount of filtering is adjustable by altering the loop bandwidths of the Tx PLL and Rx PLL and their difference.

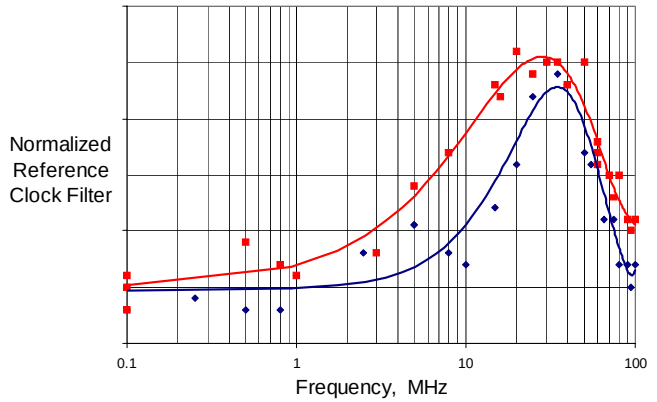

Figure 11: Measured band pass filters of a 16 Gbps data link for two pairs of Tx PLL and Rx PLL loop bandwidths.

X. Conclusion

This study has demonstrated that reduction of reference clock jitter is achievable in 16 Gbps data links by narrowing the difference in the loop bandwidths of the Tx PLL and Rx PLL. This alleviates the need for very clean clock source to supply a reference timing signal for 16 Gbps data links. The results also indicate that the model of phase jitter propagation is sufficient to explain the mechanism of clock noise reduction.

This study successfully used the technique of sinusoidal jitter injection to detect the effective band pass filtering of clock noise. When applied to links with programmable loop bandwidths PLLs, the technique can determine the various band pass filters inherent to the link architecture. Such information is useful to the designers of high speed links.

Acknowledgement

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Author Biography

Tsunwai Gary Yip joined Rambus Inc. in 2000 and is currently a Senior Principal Engineer. He developed many system clock solutions for LabStation test platforms, and the temperature control for maintaining test chips between -40°C and 125°C without using a temperature chamber. His interests are in the areas of EMI/EMC of mobile systems, low phase noise clocks for 10 - 30 GHz data links, phase noise analysis of PLLs, and thermal analysis of system and components. He is also active in new technology trends in mobile handsets and platforms, consumer electronics and PC graphics. Dr. Yip is an Associate Fellow of the American Institute of Aeronautics and Astronautics. He was a recipient of the Ralph Teeter Award from the SAE International for outstanding young educator in aerospace technology and was recognized as a Recent Outstanding Alumnus by the University of Illinois, Urbana, where he received his Ph.D. and M.S. degrees.