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Control of Clock Jitter in High Speed Data Links

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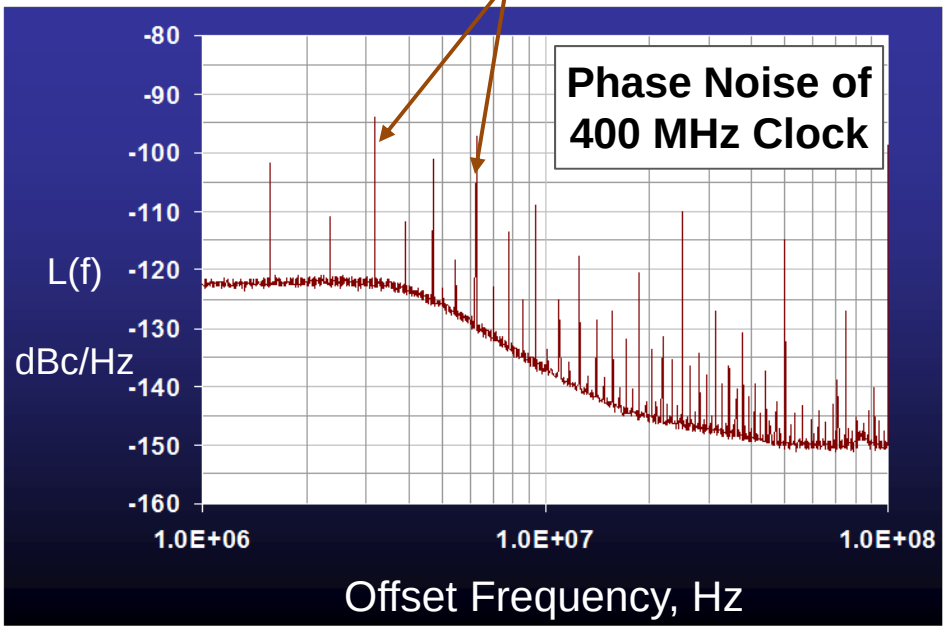
Outline of Presentation

- Random Jitter and Phase Noise
- Impact of Reference Clock Noise
- Sources of Phase Noise
- A Model of Clock Jitter Propagation
- Clock Jitter Reduction by Link Architecture
- Detecting Band Pass Filter in 5 Gbps and 16 Gbps Data Links

Relationship Between Random Jitter & Phase Noise of Clock Signal

Spurs contribute to deterministic jitter (DJ)



Spur-less phase noise profile contributes to RMS random jitter

$$RJ_{RMS} = \frac{1}{2\pi f_c}\left[\int_0^{f_c/2} 2\,L(f)\,df\right]^{1/2}$$

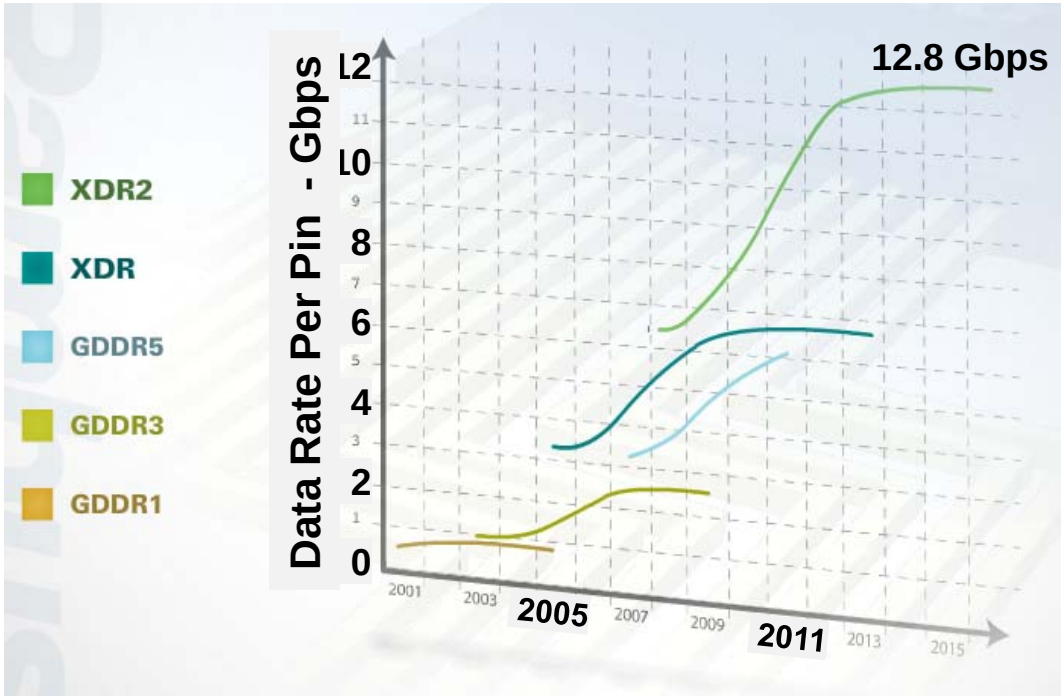
(No Spur)

BER	α
10^{-12}	14.069
10^{-13}	14.698
10^{-14}	15.301
10^{-15}	15.883
10^{-16}	16.444
10^{-17}	16.988
10^{-18}	17.515
10^{-19}	18.027
10^{-20}	18.525

$$\text{Total Jitter} = DJ + \underbrace{\alpha\ RJ_{RMS}}_{RJ}$$

α is determined from error function

Data Rate Roadmap of Memory Interfaces



Data Rate (Gbps)	Bit Time - 1 UI (ps)
20.0	50.000
16.0	62.500
12.8	78.125
9.6	104.17

Timing Budget of 16 Gbps Data Link

Random Jitter (RJ) = 30%UI

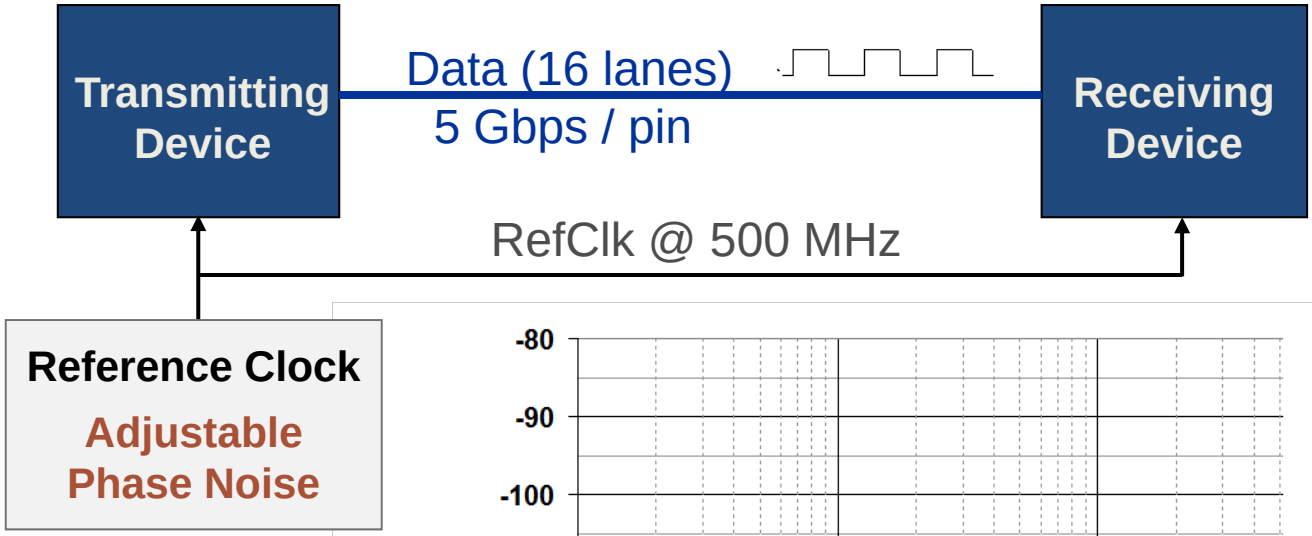
RJ_{Link} = 0.3 * 62.5 = 18.75 ps

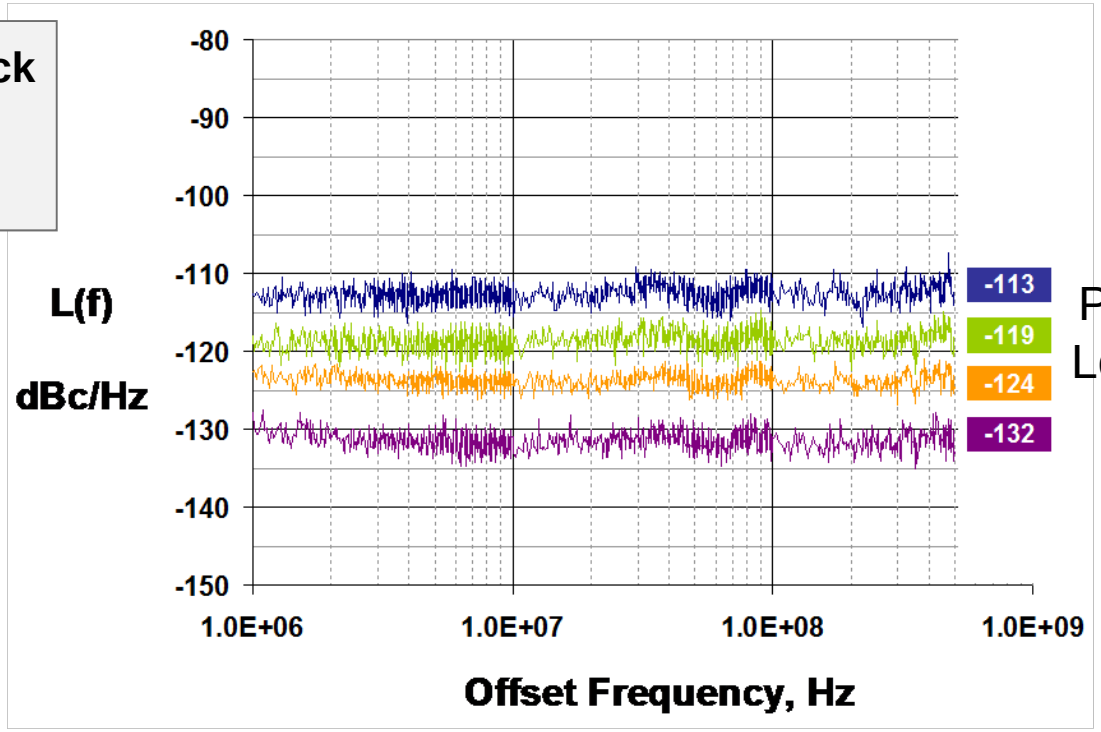
Bit Error Rate = 10^{-20}

RJ_{Link} = 18.53 * $RJ_{Link,RMS}$

$RJ_{Link,RMS}$ ~ 1 ps

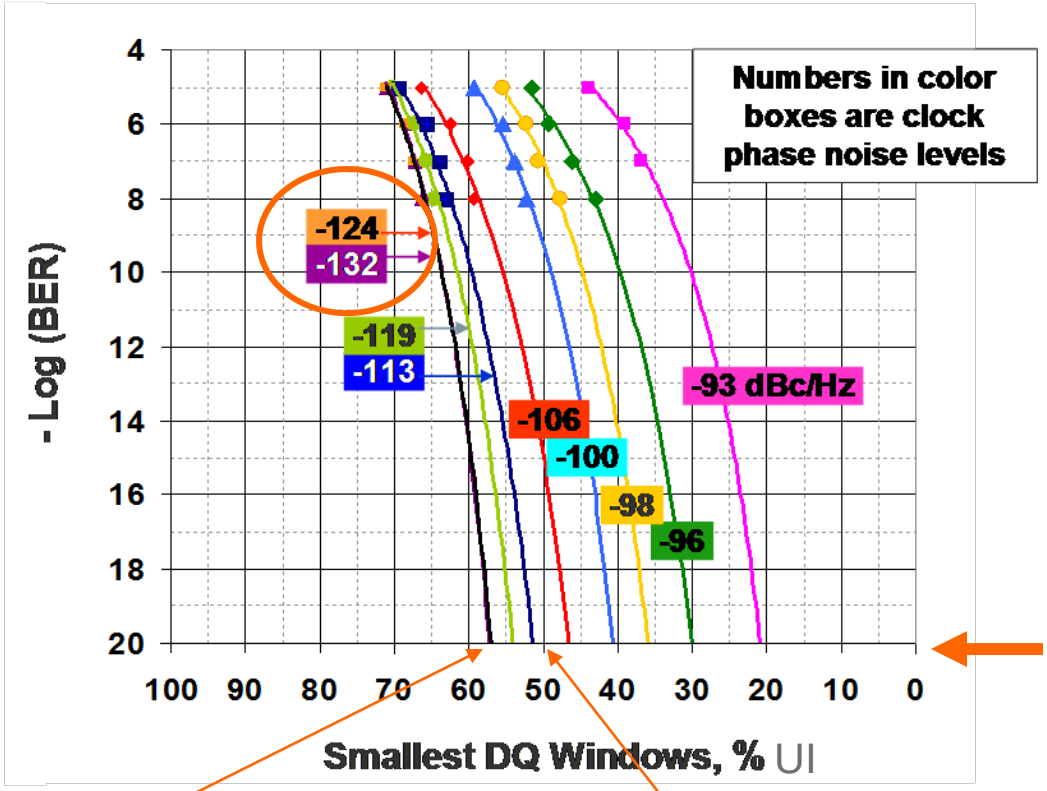
Effect of Clock Noise on Data Window





Phase Noise Levels of 500 MHz Clock

DQ Window vs RefClk Phase Noise



BER 10^{-20}

No improvement

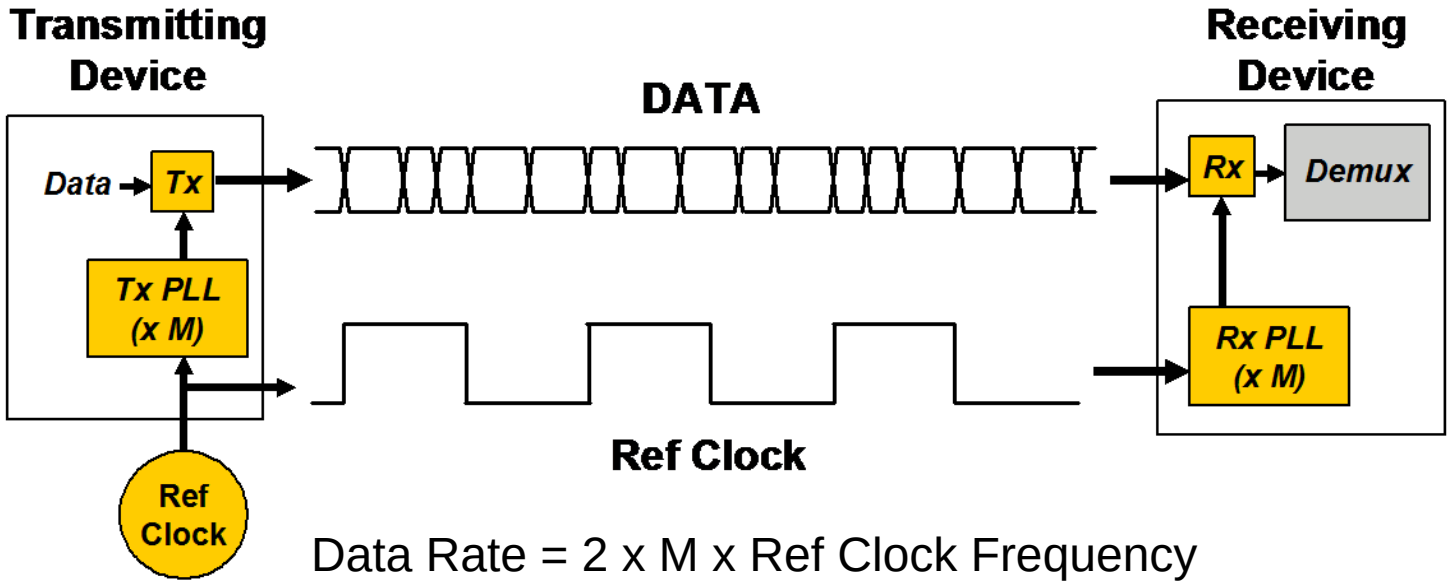
L(f) < -124 dBc/Hz

50% UI @ BER 10^{-20}

L(f) < -110 dBc/Hz

Sources of Phase Noise

Clock & Data Paths in a High Speed Data Link



Data Rate = 2 x M x Ref Clock Frequency

$$RJ_{Link,RMS} = [\, RJ_{TxPLL}^{2} + RJ_{RxPLL}^{2} + RJ_{CLK}^{2} + RJ_{Tx}^{2} + RJ_{Rx}^{2} \,]^{1/2}$$

Estimating The Random Jitter of Link Components

Very Small

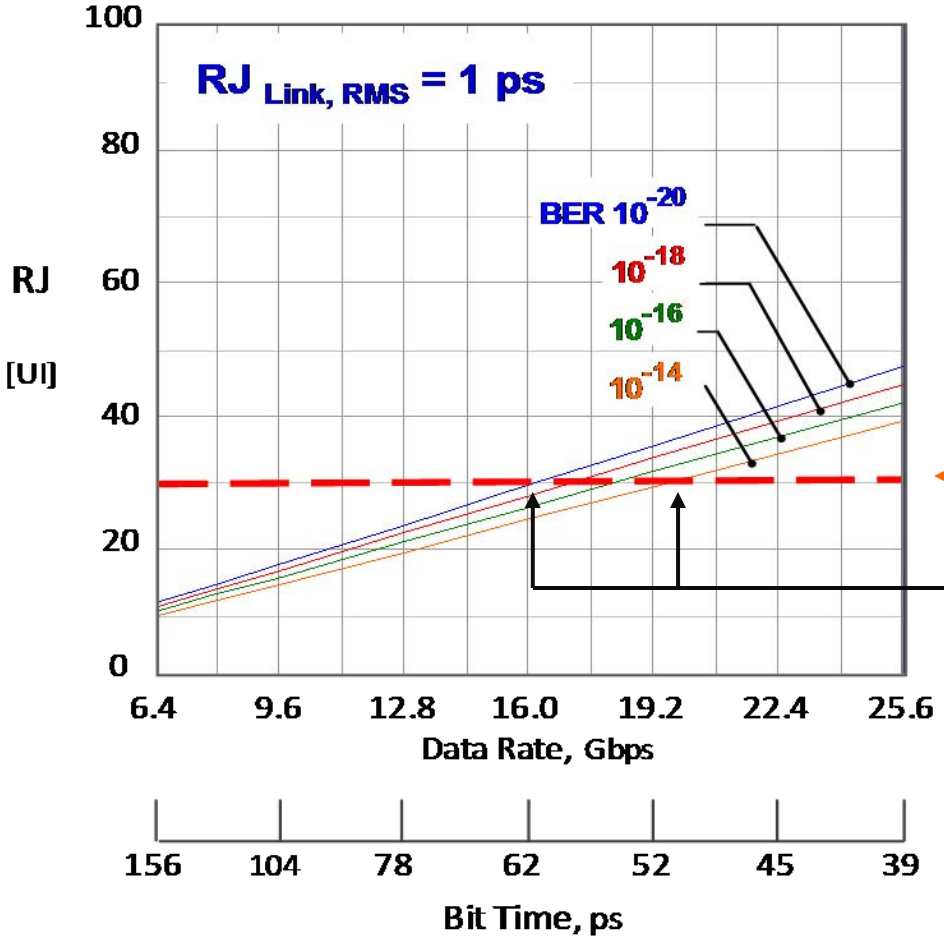
$$RJ_{Link,RMS} = [\, RJ_{TxPLL}^{\,2} + RJ_{RxPLL}^{\,2} + RJ_{CLK}^{\,2} + RJ_{Tx}^{\,2} + RJ_{Rx}^{\,2} \,]^{1/2}$$

$$RJ_{Link,RMS} = [\, RJ_{TxPLL}^{\,2} + RJ_{RxPLL}^{\,2} + RJ_{CLK}^{\,2} \,]^{1/2}$$

Assuming $RJ_{TxPLL} = RJ_{RxPLL} = RJ_{CLK}$, for $RJ_{Link,RMS} = 1$ ps

$$RJ_{TxPLL} = RJ_{RxPLL} = RJ_{CLK} \sim 0.6 \text{ ps}$$

Impact of Data Rate on Bit Error Rate



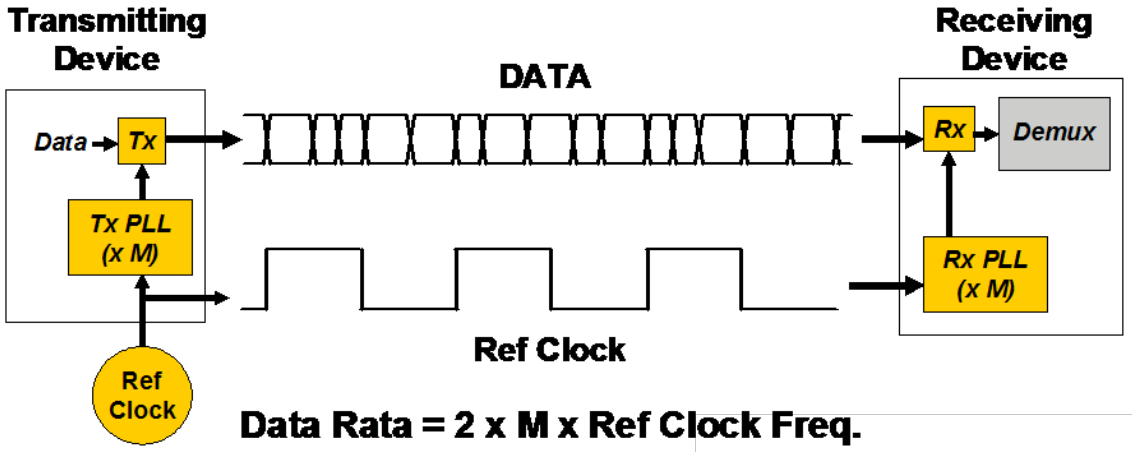
RJ = 30% Link Budget

16 Gbps, BER @ 10^{-20}

20 Gbps, BER rises to 10^{-14}

Reduce component RJ to below 0.6 ps to achieve lower BER

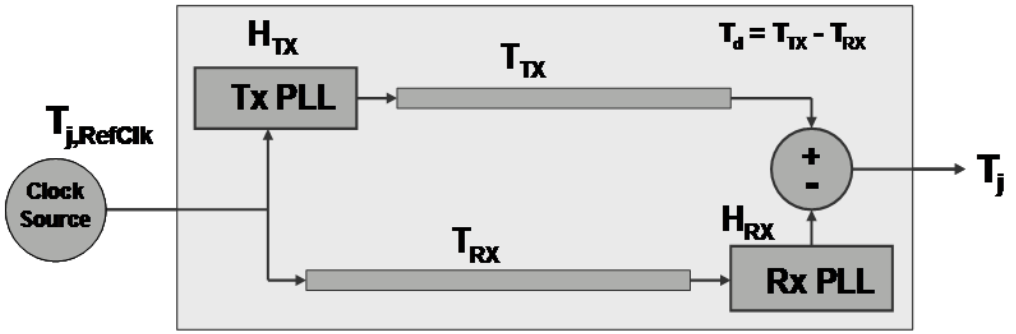
Model of Clock Jitter Propagation



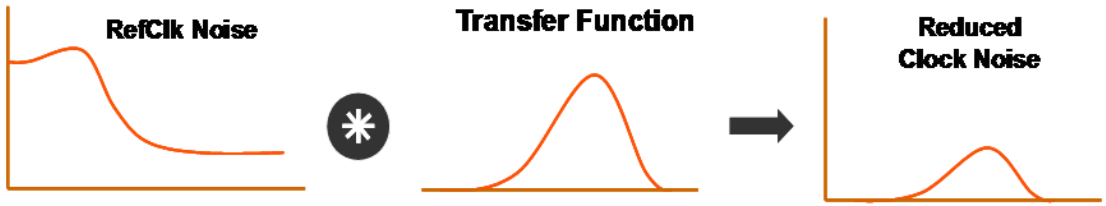
Data Rata = 2 x M x Ref Clock Freq.

Link Architecture Reduces Clock Noise

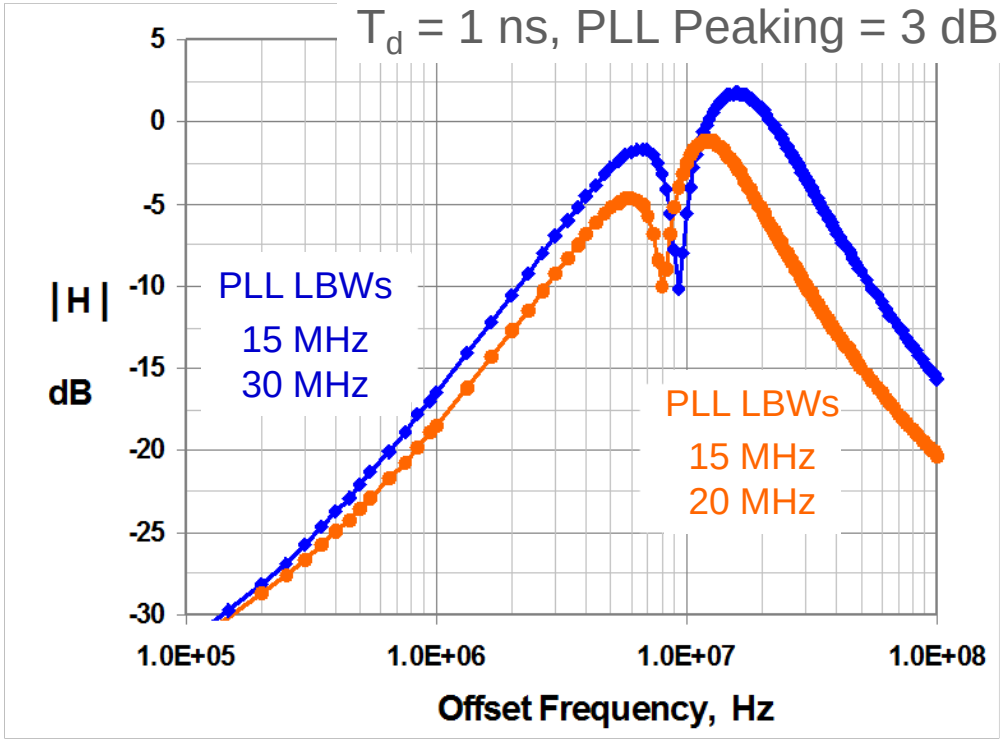
PLL Peaking
PLL LBW
Delay Time Mismatch



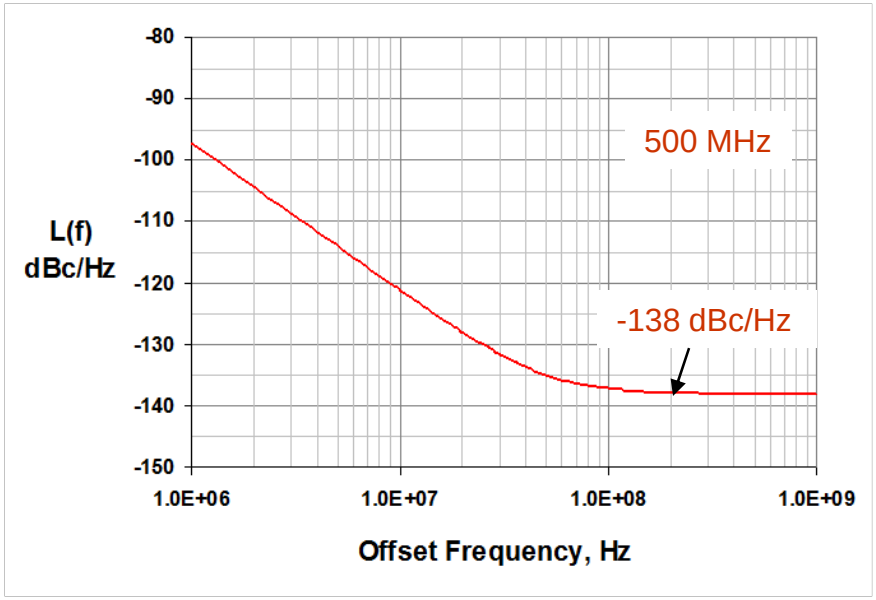
Phase Jitter Transfer Model, Transfer Function H



Band Pass Filters for Two Sets of PLL Loop Bandwidths



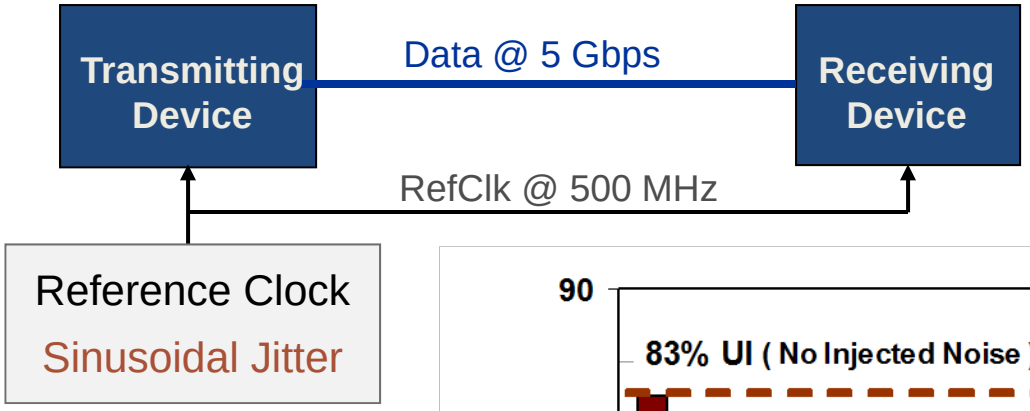
Filters for Two Pairs of PLLs

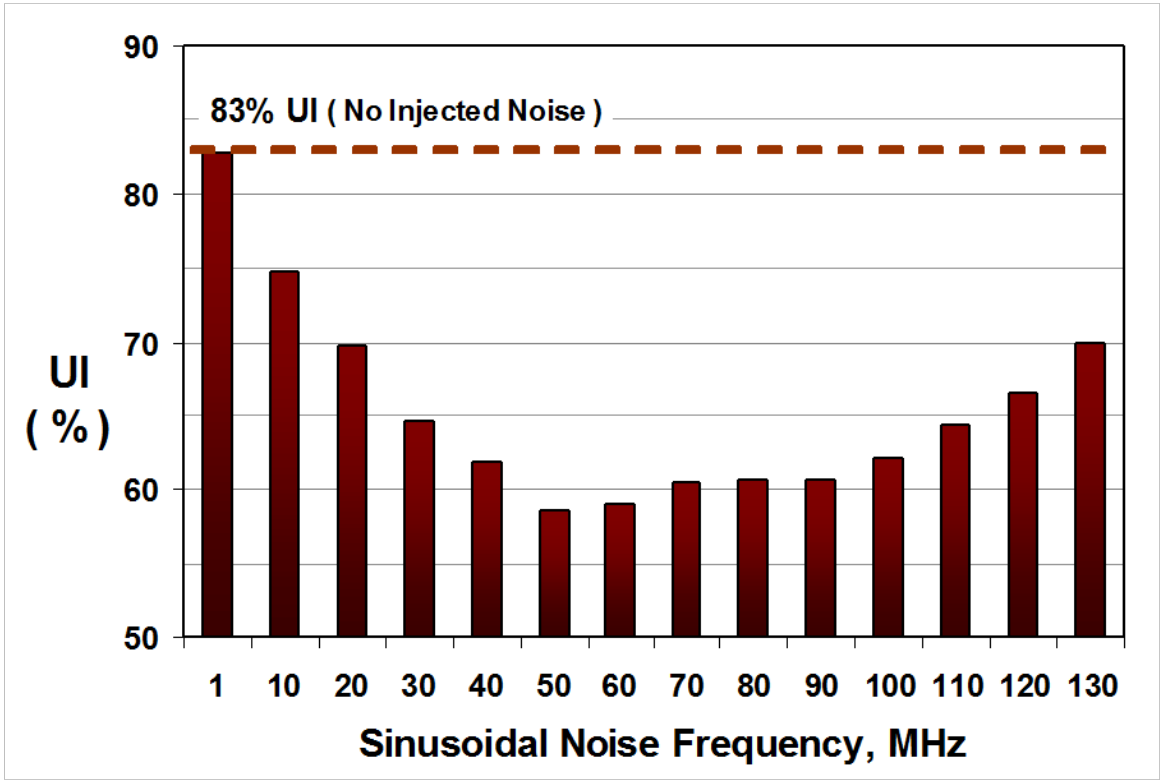


Phase noise profile of HV Production Clock

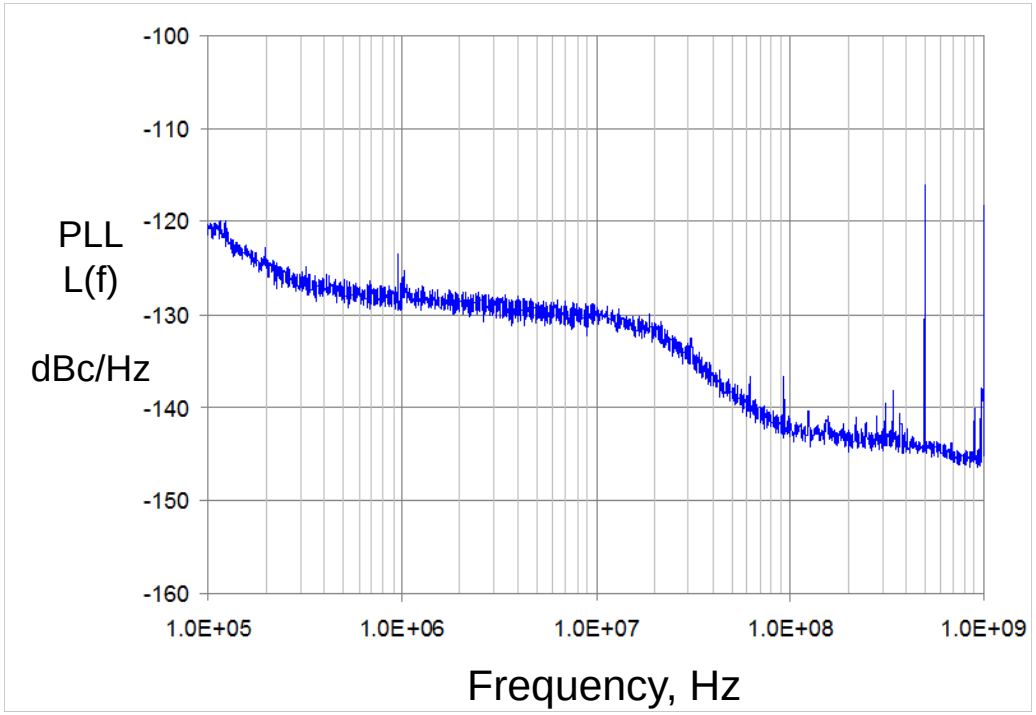
LBWs of Tx PLL an Rx PLL control clock noise filtering

Detecting Band Pass Filter

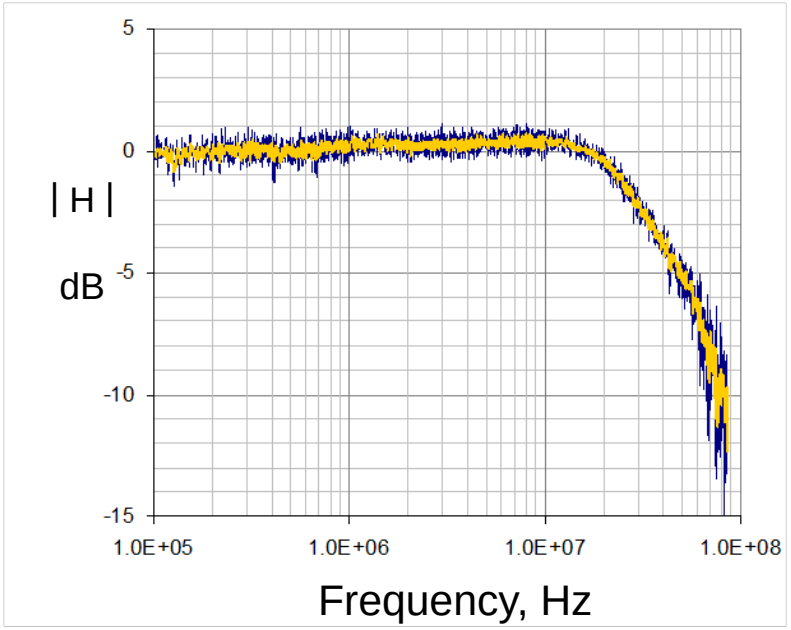




16 Gbps Link of a TB/sec Memory System

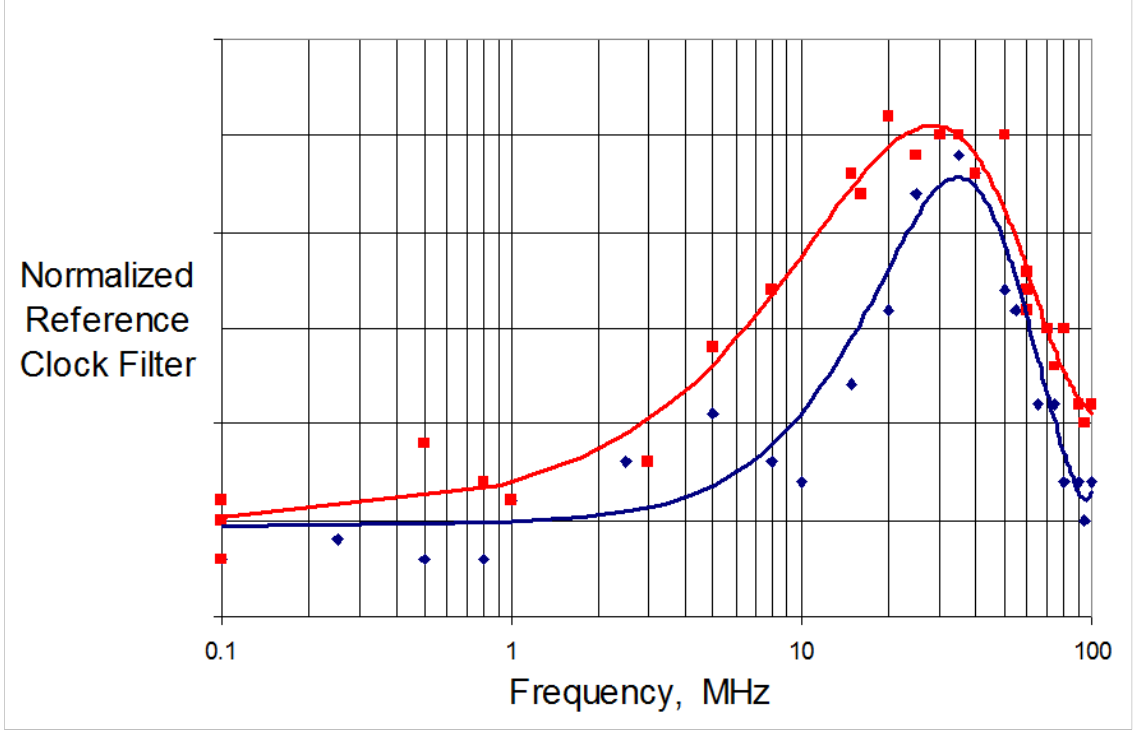


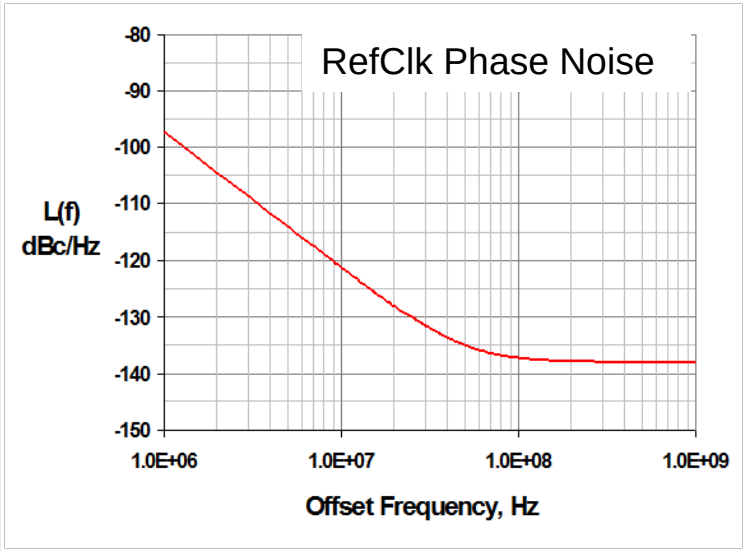
PLL Phase Noise



PLL Transfer Function

Band Pass Filters of a 16 Gbps Data Link





Red Filter: RJ_{CLK} ~ 0.35 ps

Blue Filter: RJ_{CLK} ~ 0.2 ps

Low cost clock chip can support 16 Gbps data link

Conclusion

- Reduction of RefClk jitter is achievable by
  - Narrowing LBW difference of Tx PLL and Rx PLL
  - Setting the filter to a higher frequency to avoid low frequency jitter in RefClk
  - Minimizing PLL peaking
- Low phase noise clock chips that are already in high volume production can support 10 Gbps and faster data links