Impact of DFT on Test
Douglas Kay, Cisco, dKay@cisco.com
Any common goals?
Quality Level Prediction

- defect level = \( \frac{\text{#bad parts}}{\text{#parts passing the test}} \)
- Theoretical predictions
  - Williams & Brown (1981): \( DL = 1 - Y^{(1-f)} \)
  - Seth & Agrawal (1982): \( DL = \frac{\frac{1}{k} (1-f)(1-Y)e^{-(n_0 - 1)f}}{Y + (1-f)(1-Y)e^{-(n_0 - 1)f}} \)

IT C 1991 P. Maxwell & et al
Early stage D & T conflicts

Fig 1: Need for DFT

Fig 2. DFT was a hard sell

Note: Figures are from one of ITC tutorials and Design & Test Spring 1994 article by B. Bennetts, respectively
DFT Solutions Timeline

- **(70’s & 80’s)** μ technology
- **(90’s)** Sub μ technology
- **(00’s)** nano technology

- Ad-hoc DFT
- Full Logic Scan
  - Memory BIST
  - JTAG
- Partial Logic scan
- At-speed BIST
- Advanced DFT

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Pure Functional doesn’t scale

Pure Structural

Transition to Structural Test.
ATPG/Automation, Defect Models, FaultGrading

* Reference: “Narrowing the gap between functional and Structural test” by Han Ta and Matthais Kamm at ATE2020, 2009
Cost for Digital ATE system

<table>
<thead>
<tr>
<th>Year</th>
<th>Functional ATE</th>
<th>Structural ATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>2000</td>
<td>High Pin Count</td>
<td>Low Pin Count (Jtag)</td>
</tr>
<tr>
<td>2010</td>
<td>High Speed</td>
<td>Medium Speed (250Mhz)</td>
</tr>
<tr>
<td></td>
<td>High Complexity</td>
<td>Low Complexity</td>
</tr>
</tbody>
</table>

ASIC DFT
Yields high ROI due to reuse during bring-up, on ATE, in field and for fast failure analysis
Switching moment to at-speed

Improving Test Quality -- At an Increasing Cost

More and newer tests

Where is my defects?

ASIC cross section

- Metal 8
- Metal 7
- Metal 6
- Metal 5
- Metal 4
- Metal 3
- Metal 2
- Metal 1

Bugs
Stacked via
Transistor

VOLUME OF TEST DATA (Relative)

180 nm
2M Gates
150 nm
5M Gates
120 nm
15M Gates
90 nm
30M Gates
65 nm
30M Gates

PROCESS TECHNOLOGY / GATE COUNT

100
80
60
40
20
0

Gate Delay
Sum of Delays, Al & SiO2
Sum of Delays, Cu & Low κ
Interconnect Delay, Al & SiO2
Interconnect Delay, Cu & Low κ

Gate with Al & SiO2
Gate with Cu & Low κ
Gate

Delay (ps)

Generation (nm)

Gate with Al & SiO2
Gate with Cu & Low κ

Al 3.0 μΩ/cm
Cu 1.7 μΩ/cm
SiO2 κ = 4.0
Low κ κ = 2.0
Al & Cu .8 μ Thick
Al & Cu Line 43 μ Long

Silicon Valley Test Conference 2010
DFT Solutions Timeline

(70’s & 80’s)  
μ technology

(90’s)  
Sub μ technology

(00’s)  
nano technology

Ad-hoc DFT

Partial Logic scan

Full Logic Scan
Memory BIST
JTAG

At-speed BIST

Advanced DFT

- Using PLL on-chip clock control
- Heavily BISTed for various IP’s
Test Methodology Timeline

Pure Functional (doesn’t scale)  Pure Structural

Transition to Structural Test. ATPG/Automation, Coverage, FaultGrading, Process

We have a problem…

Unmodeled Defects / Noise, cross-talk lack of margin…

NTF

* Reference: “Narrowing the gap between functional and Structural test” by Han Ta and Matthais Kamm at ATE2020, 2009
Difficult test problems in focus

• In-system test & debug cost very expensive
  – 10x rules, stage to stage

• Test gap exists
  – standalone vs in-system test
    • standalone: structural test
    • in-system: functional test

• Different test condition
  – TVF, boot-up sequence, Avdd ramp, noise
Overall Test Strategy

- **DFT based ATE Test**
  - **Pass?**
  - **Y**
  - **N**
  - **FA or Yield Loss**

- **Component ATE test**

- **Board test**
  - **Pass?**
  - **Y**
  - **N**
  - **XRAY/ICT/Boundary Scan**
    - MBIST
    - IOBIST
    - LBIST

- **System test**
  - **Pass?**
  - **Y**
  - **N**
  - **Ship Product**
  - **Diagnosis or replacement**

Reference from ITC06 paper by T. Vo and et al
Two methods to access built-in test features:

1. JTAG for board test
2. CPU to all ASICs for on-line/off-line system test
DFT for ASIC

Test features can be accessed by CPU I/F or JTAG I/F
Closing the test gap

At board/system test
1. Debug system failure through both functional and structural test
2. Duplicate the failure using socketed system if needed

At ATE test
1. Develop same functional test vector access-able via JTAG
Other Benefits

• Test Cost Reduction at Board/System Test
  – e.g.) Ext Memory BIST
    • less than 1 min test time vs 8 hour in traditional functional test

• Help test correlate subtle defects
  – Cross clock domain defects
  – Missing coverage between IP’s
  – Defects dues to SI,

• Extra debug capabe at ATE and board/system
  – ATE : margin check using shmoo plots
  – Board/System : performance measure at system env
Eyeing on yield beyond testing

- Defect level can be minimized not only by Test coverage, but also by Yield.
- Newer process technology doesn’t look promising for a good yield.
- Stringent test means low margin to the ASIC suppliers.
- Helping suppliers to increase their yield is an ultimate win-win solution!
Summary

• Reviewed key DFT techniques and timeline, which helped test to advance with test cost under control
• New DFT techniques are required in both ASIC and board/system level to resolve difficult test problem
• Test correlation using new DFTs helped to close the gap between standalone and in-system test
• The win-win solution beyond mere test screening is under way.