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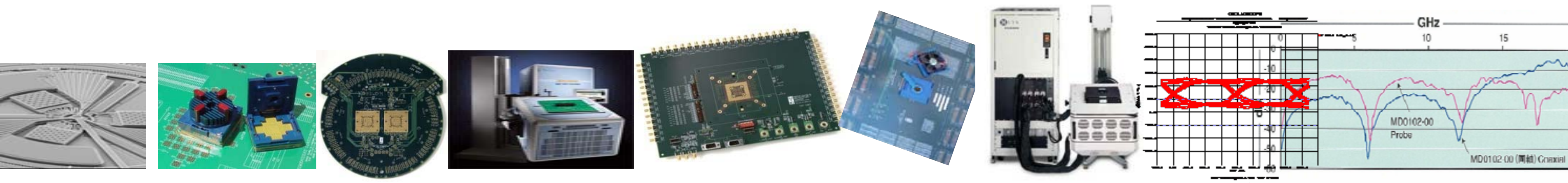
Silicon Valley TEST Conference & Expo San Jose Nov. 8-9, 2010 www.svtest.com



Resurrecting Dated ATE for High Speed Serdes Testing

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Problem Statement

- SerDes is making its way to all device classes
  - Technological reasons: chips run faster, cooler
  - Market reasons: HD Video everywhere
- SerDes testing is difficulties:
  - Complex “digital” protocols
  - Subtle “analog” measurements
  - Measuring noise and noise tolerance

Problem Statement

- Traditional ATE approach to SerDes test is too expensive for Consumer device market
  - Expensive instruments for high-end server and communications markets
- Installed Base ATE has insufficient capability
  - Legacy ATE: No OEM support vs. new system sales
  - In-house ATE: Big development to add capability
  - OSAT: Same issues as In-House ATE

Proposed Solution

Legacy ATE

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OR

Focused SerDes Port Tester

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Optimized Test Solution

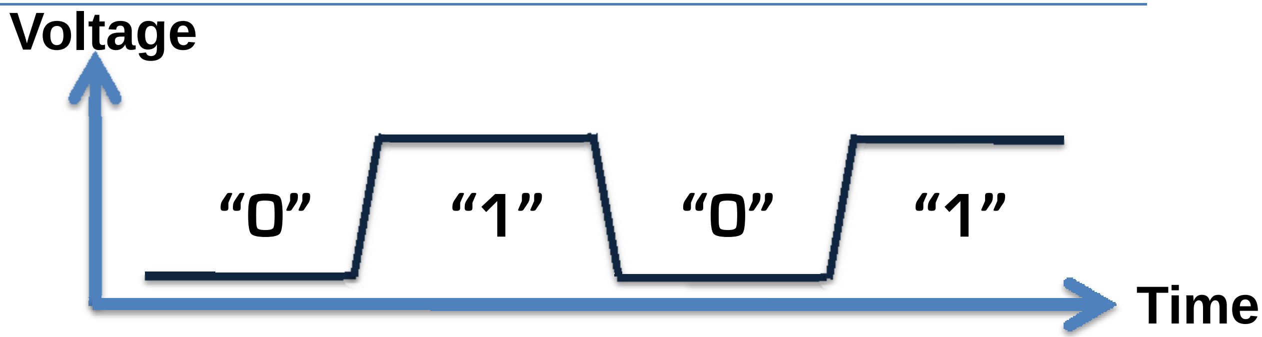
- Benefit from the cost of legacy ATE
- Benefit from the flexibility of modern SerDes Port Tester

Agenda

- The need to "connect" to SerDes
  - Plug-and-play testing
- Focused SerDes port tester description
- Experimental Results and Correlation with Bench Equipment
- Case Study: 800 Mbps MIPI wafer-level test on 40 MHz ATE
- Conclusion

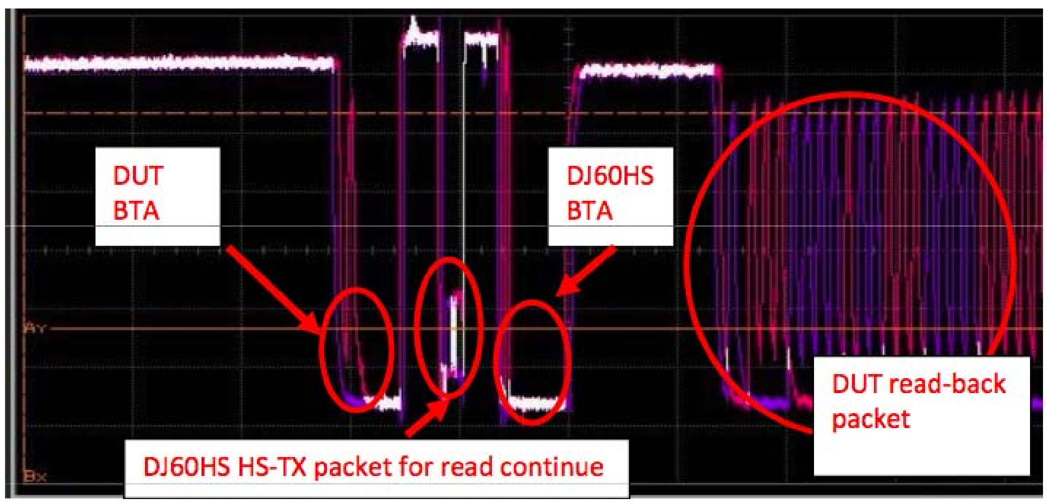
The Need to “Connect”

Legacy Digital Signal



Modern interfaces need a complex hand-shake before they can be tested!

Typical Modern Signal (MIPI)



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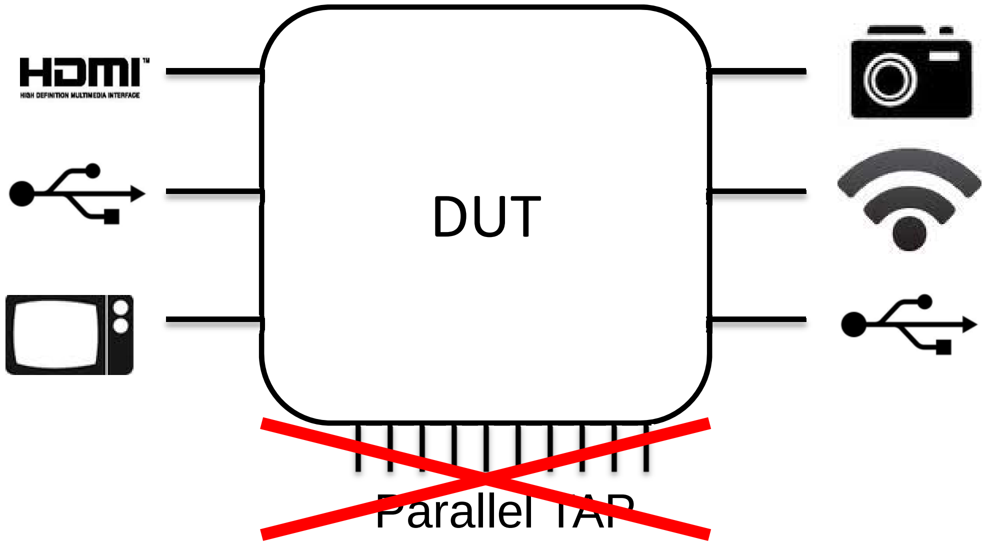
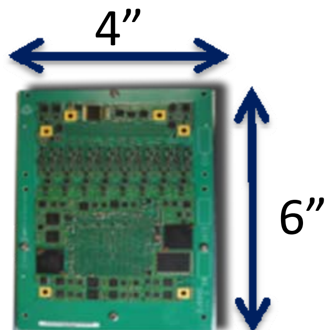
The Need to "Connect"

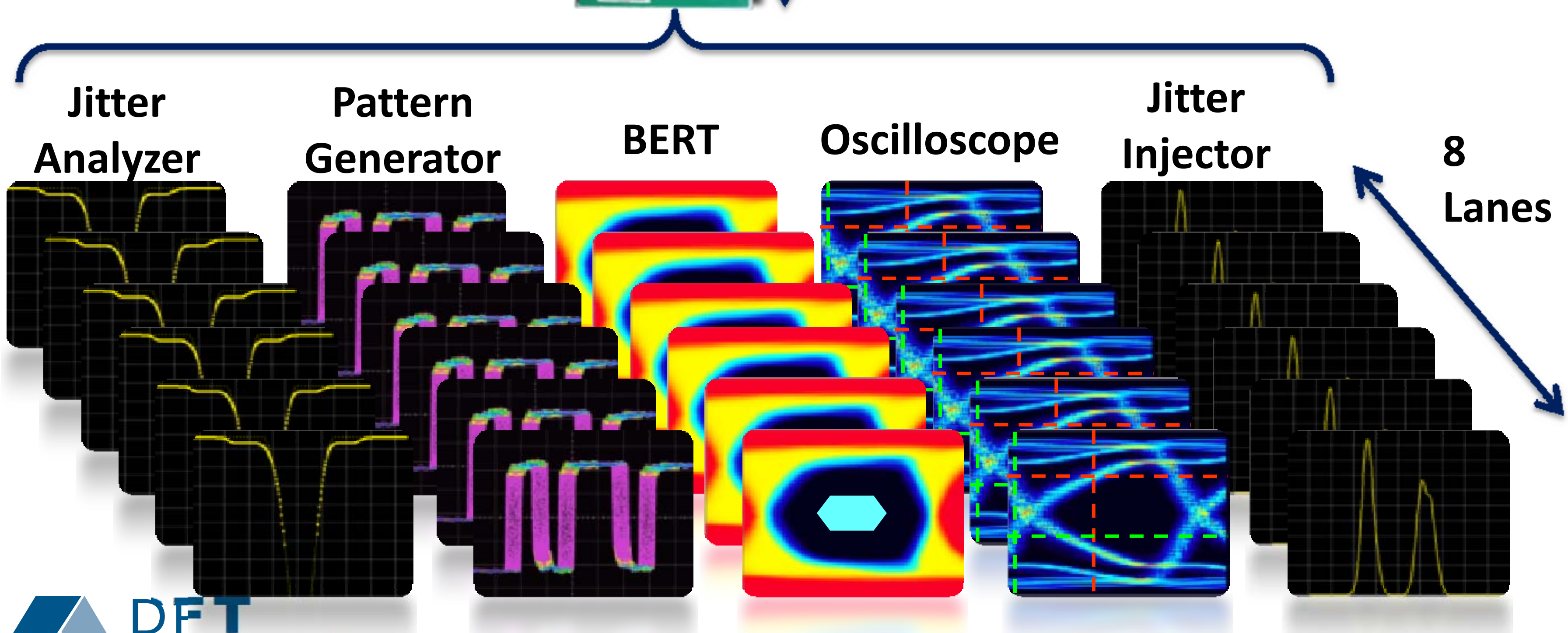


- Test access ports are disappearing due to high integration levels
- Testing the transistors inside the "core" of the device has to occur through the protocol

6.4 Gbps SerDes Port Tester



Natively capable of PHY tests due to integration of AC parametric circuitry



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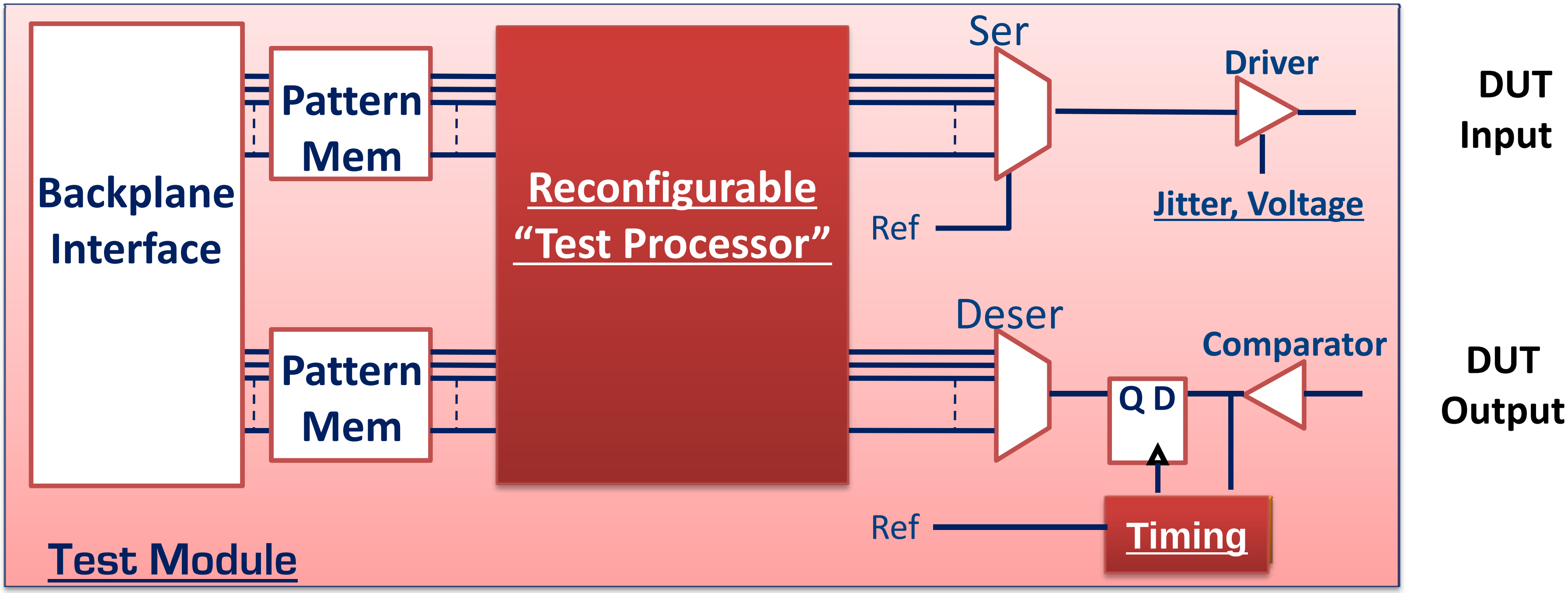
Flexible Architecture



- Maintain the usual digital pattern handling capability that we expect from a digital ATE

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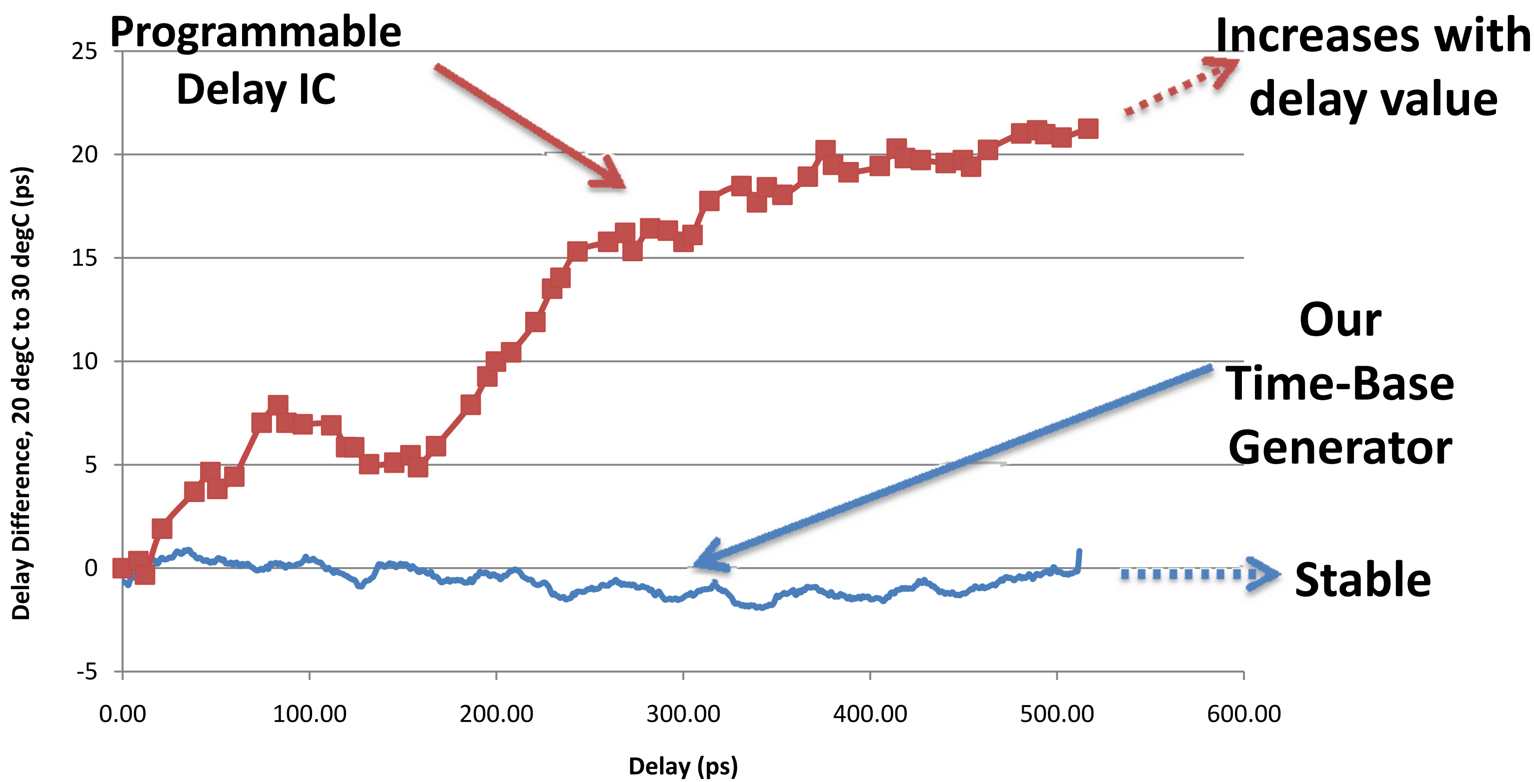
Key Technologies

Temperature-Stable Timing Generator



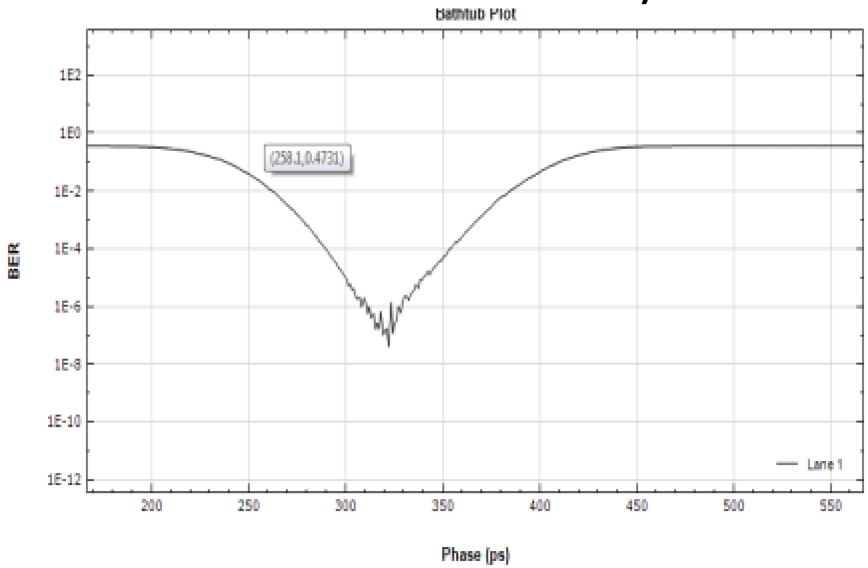
- **For each time-base generator delay setting, the change in delay due to a 10ºC rise in temperature is displayed**

Key Technologies

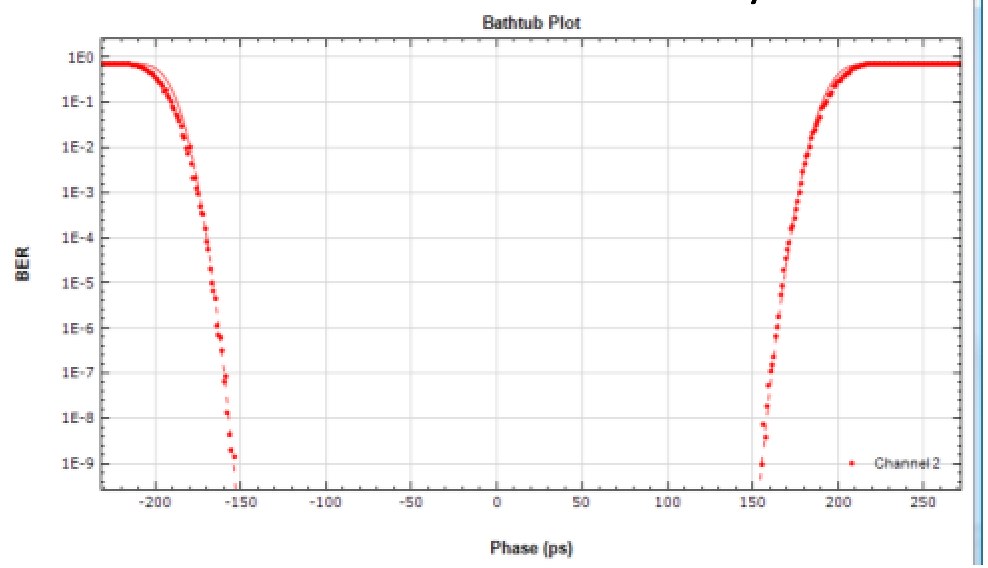
Clock Recovery

- **Single DUT response measured with and without clock recovery**
- **Low frequency jitter is completely tracked with internal Clock Recovery**

No Clock Recovery



Internal Clock Recovery



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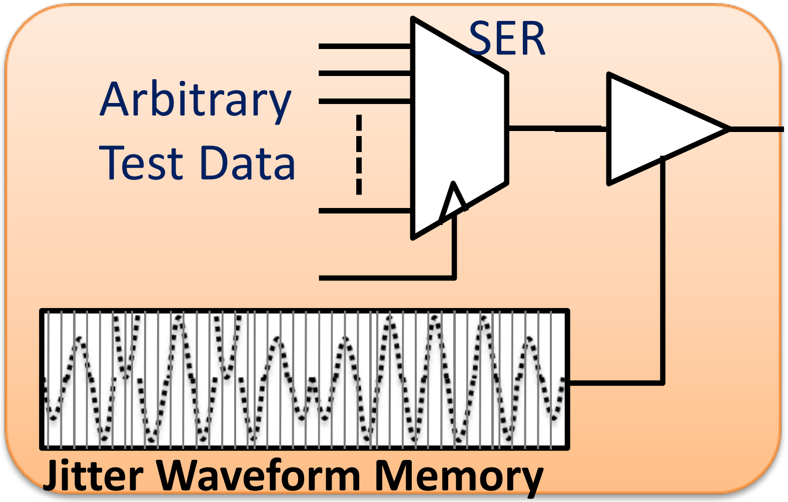
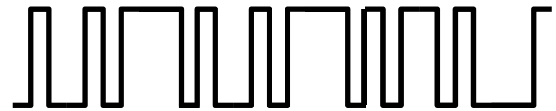
Key Technologies

Waveform-Based Jitter Injection

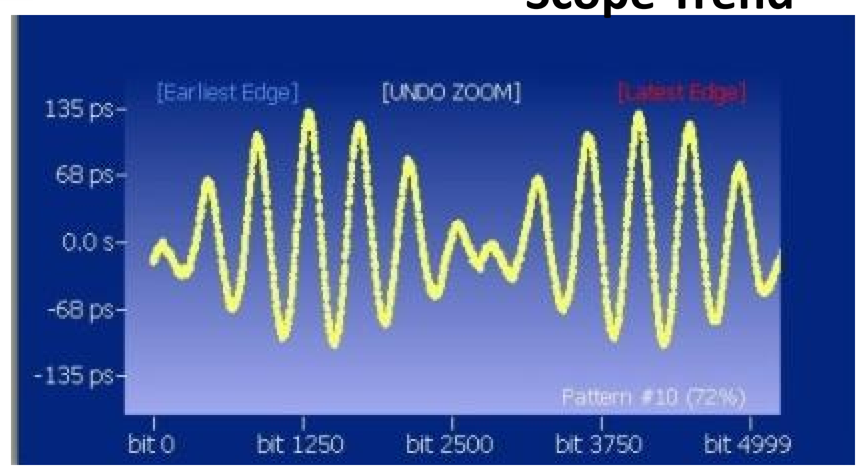


Behavioural Model



Jittered High-speed Data or Clock

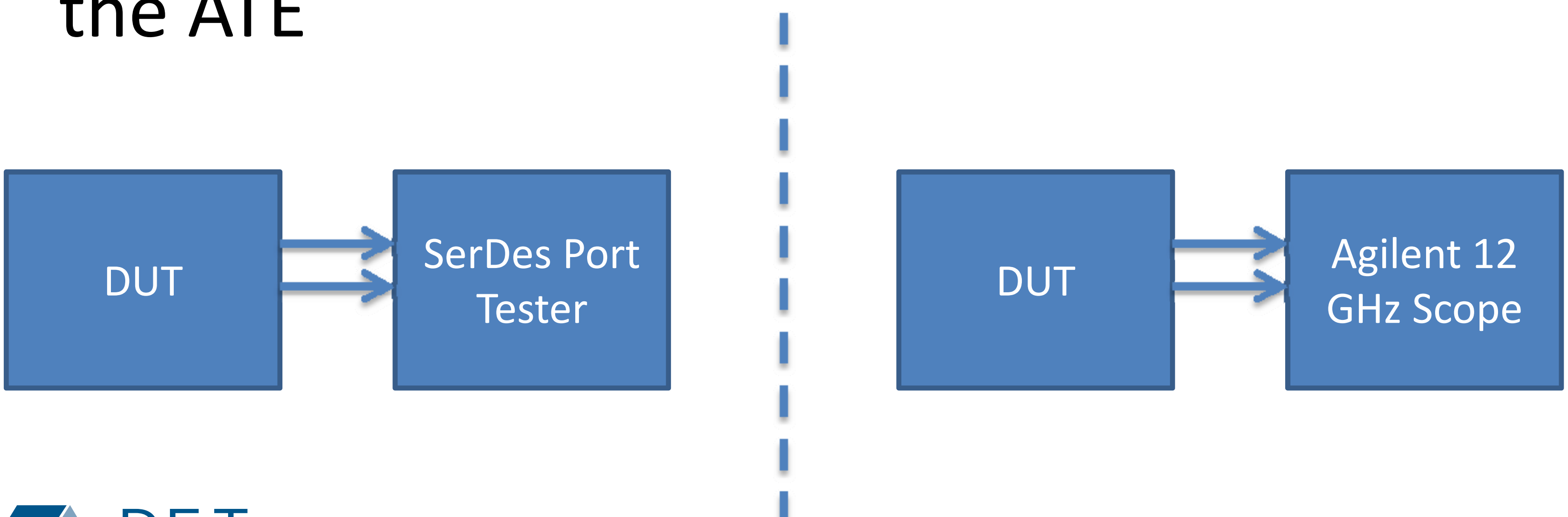
Scope Trend



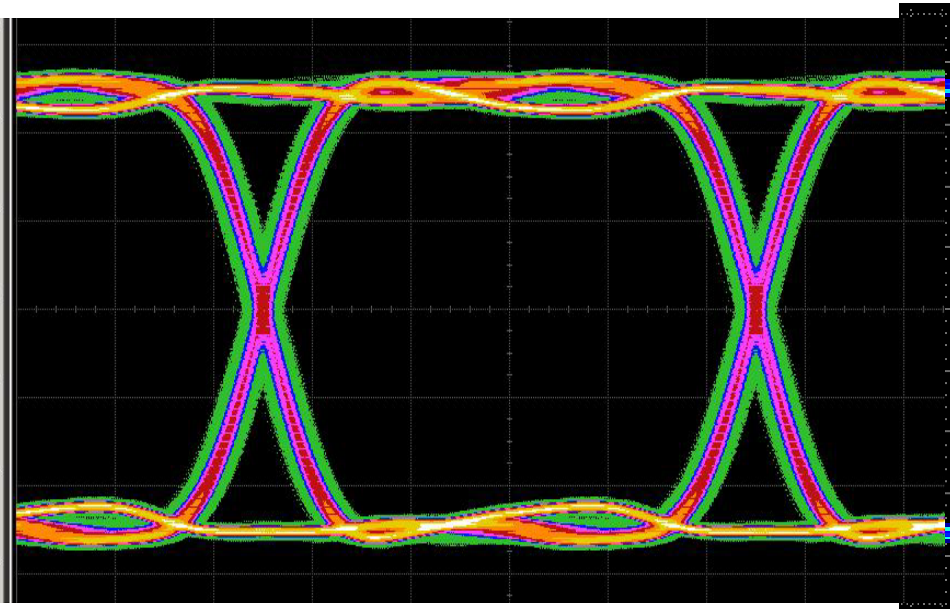
- **Like time-base generator, jitter injection logic is high purity and compact**

Experimental Results

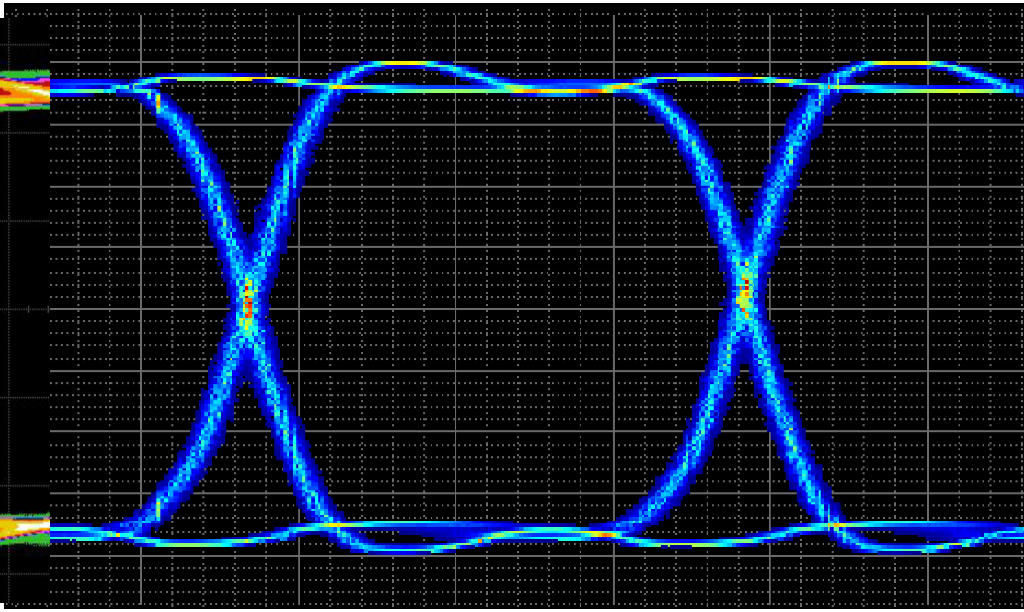
- A single DUT was measured using the SerDes port focused tester and using an Agilent Infiniium DSO81304B 13 GHz oscilloscope
- The objective was to evaluate signal fidelity on the ATE



3.2 Gbps Eye Comparison



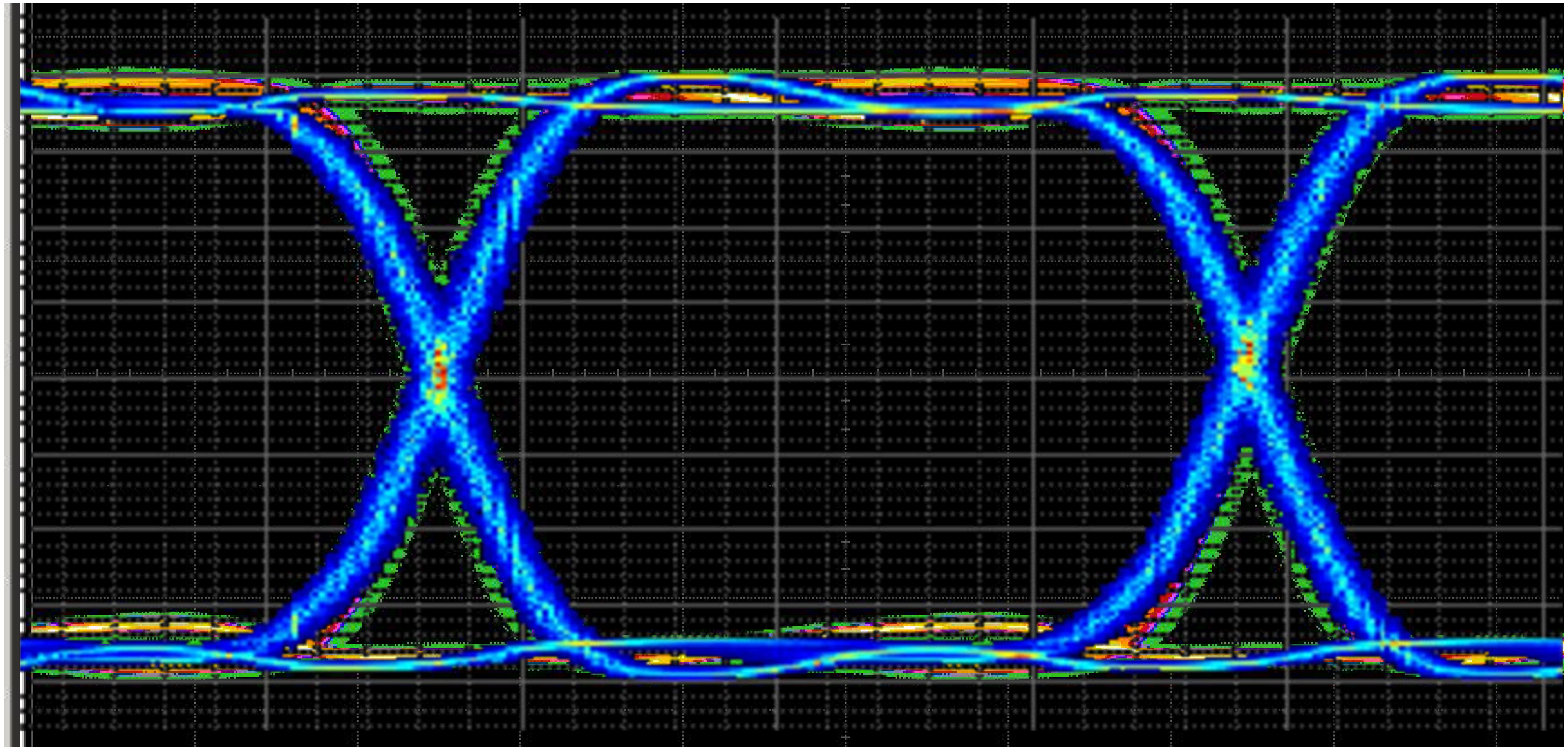
Agilent DSO capture



SerDes Port Tester capture

3.2 Gbps Eye Comparison

Overlay



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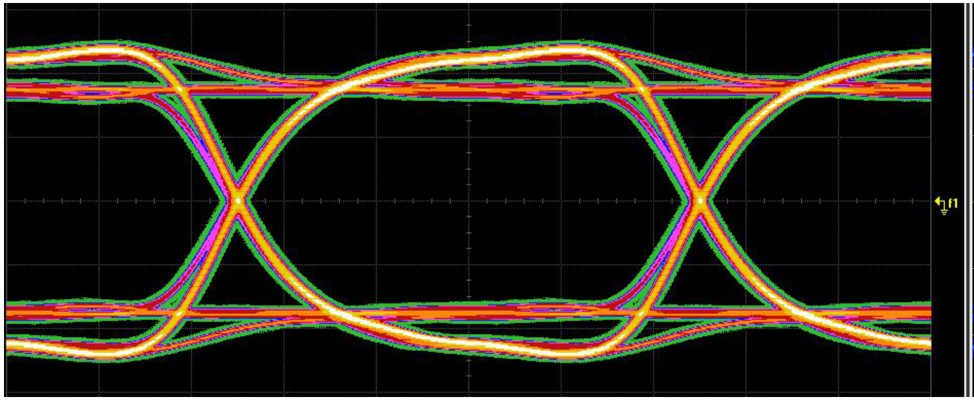
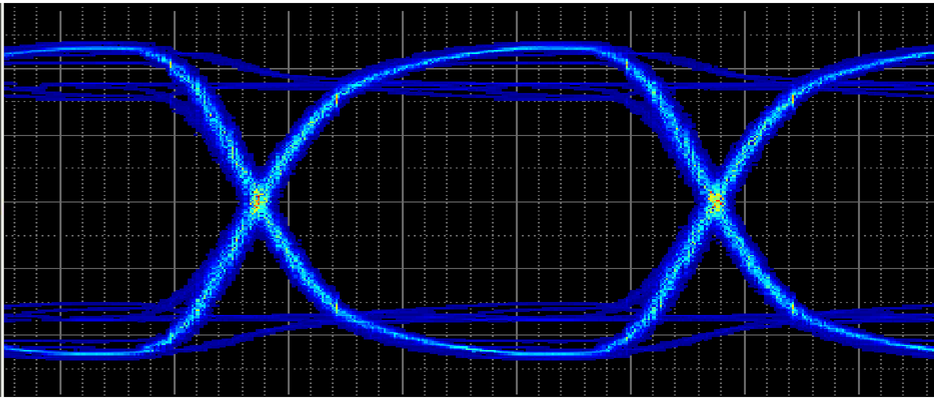
PCIe Comparison



Agilent DSO capture



SerDes Port Tester capture

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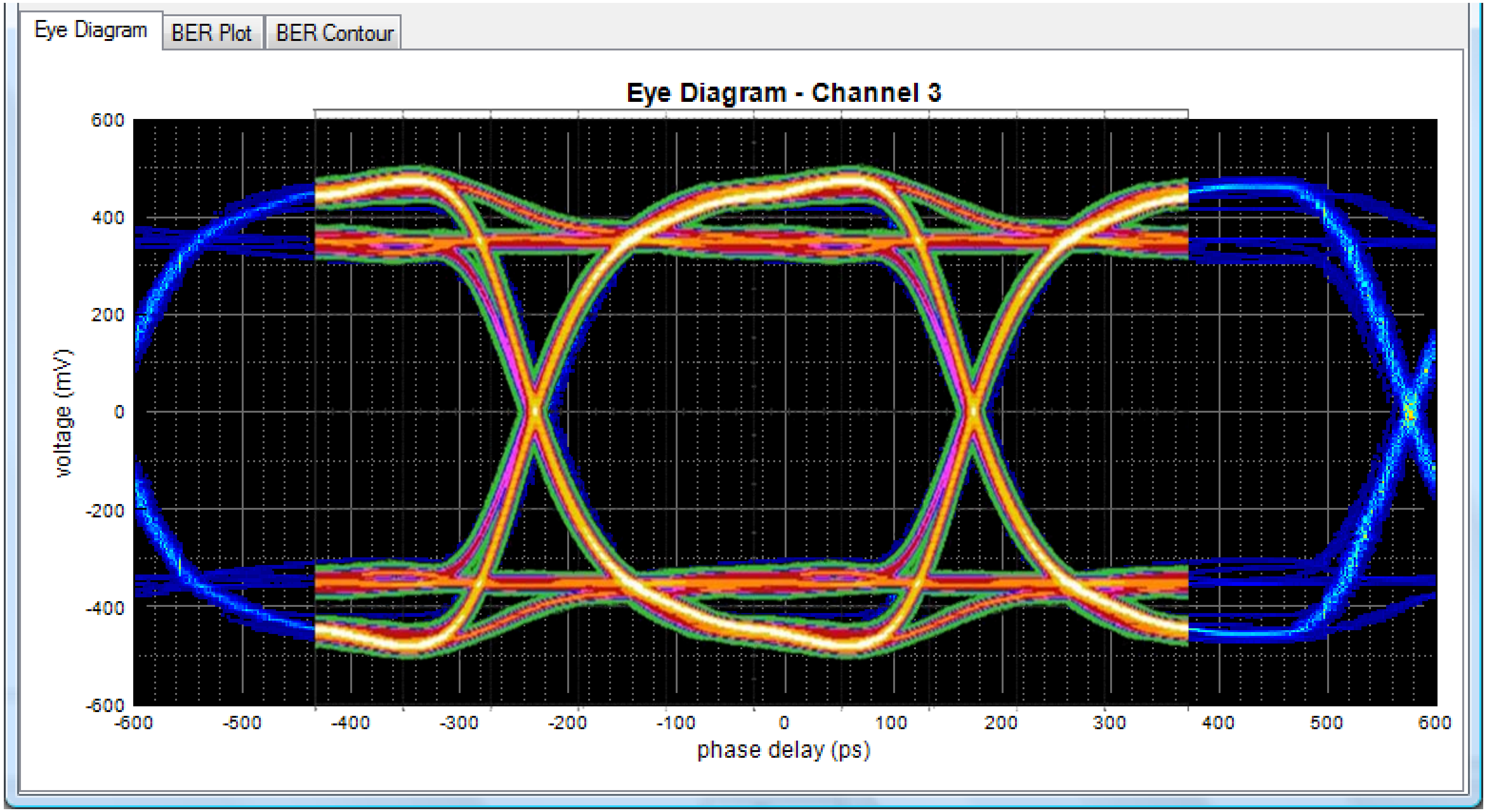
PCIe Comparison

Overlay



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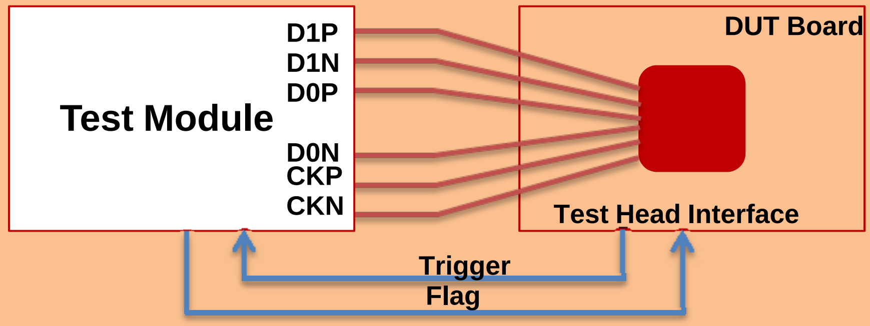
Case Study: MIPI DSI

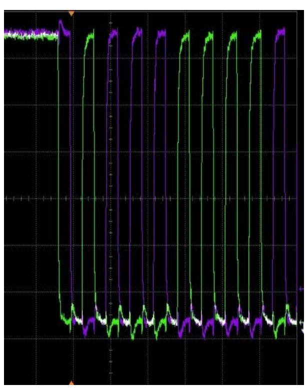
CITY OF SAN JOSE
CAPITAL OF SILICON VALLEY

Objective: Memory Test of Display Device

- Fully-autonomous handshake through the DSI protocol (D-PHY)
- I/O test is only secondary to <u>full memory test</u>
- Need a protocol exerciser on ATE!

Connection Diagram





LP Data Transmission

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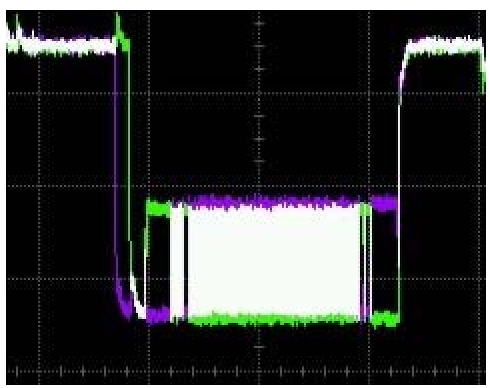

HS Data Transmission

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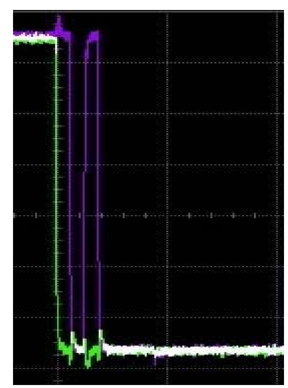

Bus Turn-Around

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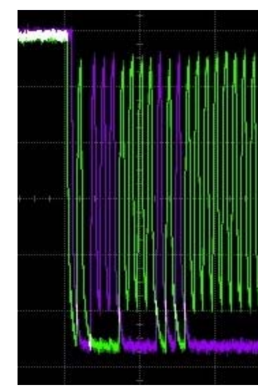
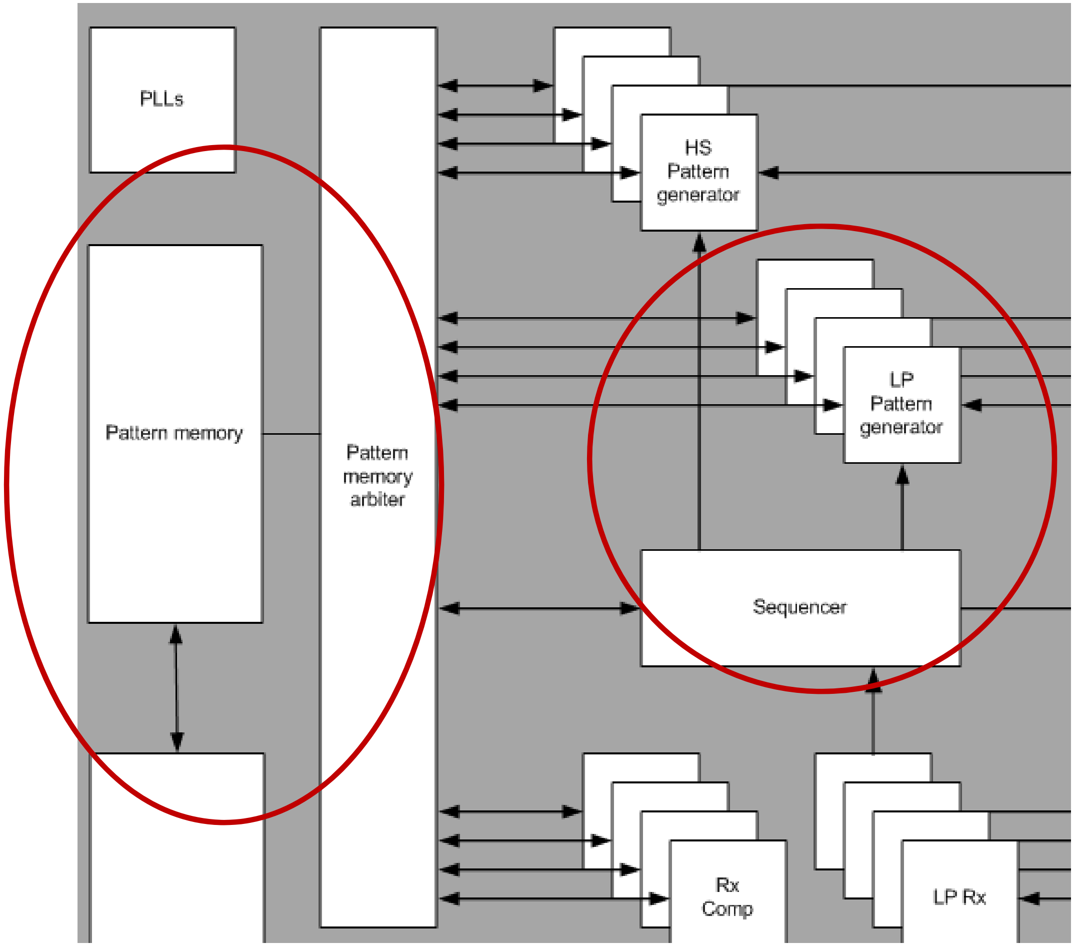


LP Data Capture

Customized Test Processor

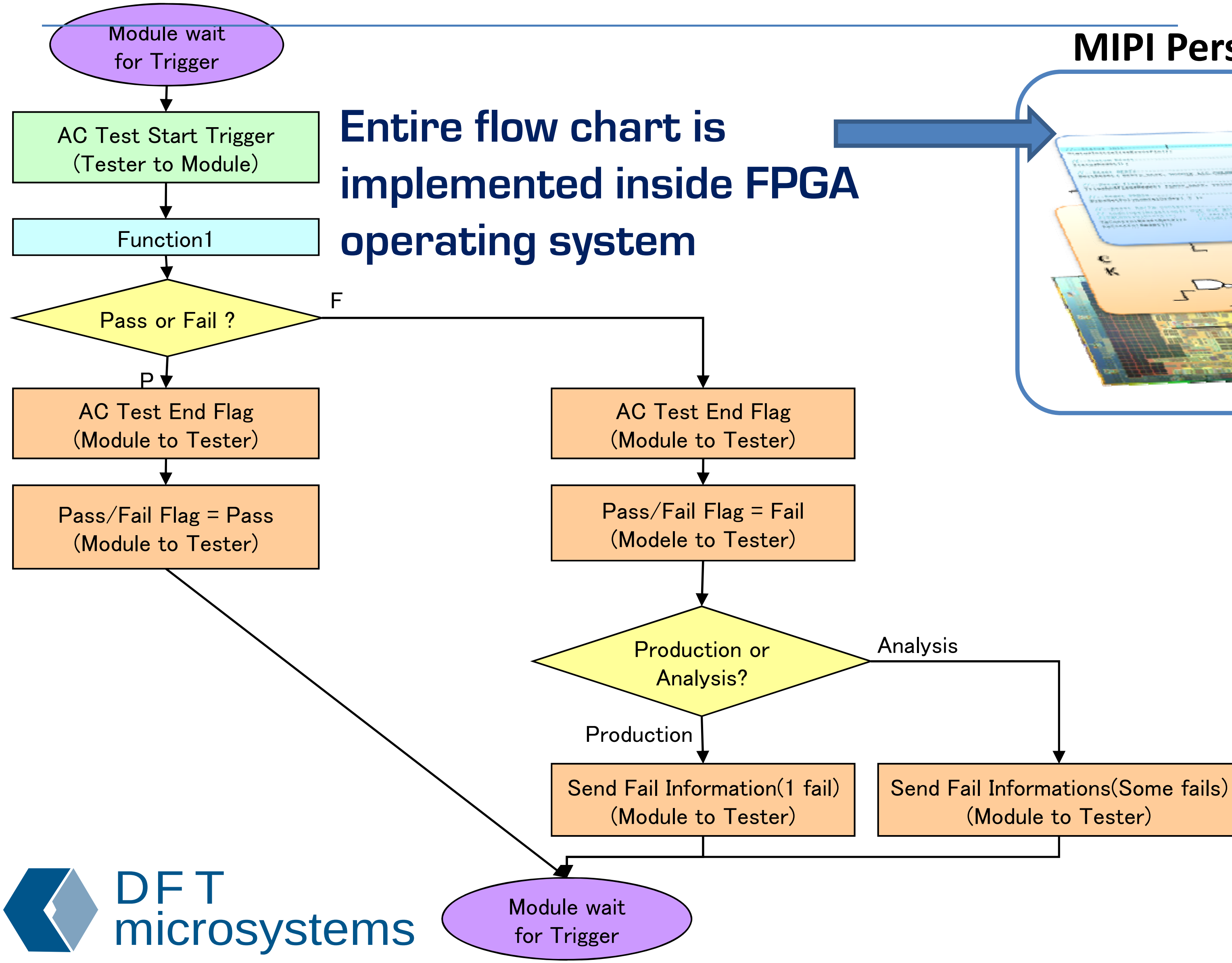
Main pattern memory



Additional LP and sequencer blocks

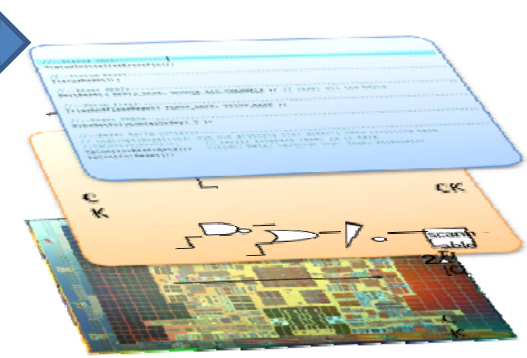
Additional LP Rx compare

Simplified Flow Chart



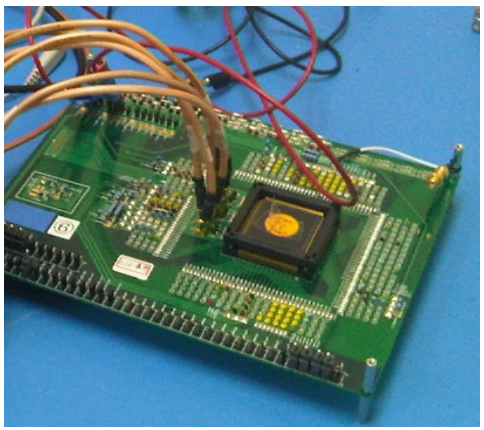
Entire flow chart is implemented inside FPGA operating system

MIPI Personality



Programming Model

Step 1: Develop program on bench (high-level commands in CSV format)



State	*MIPI Data Value*		*Description*
CTRL	**EME**		
CTRL	**LPDT**		
LP-TX	29	1	**DI=29 (Generic Write, Long)**
LP-TX	5	2	WC(0)=05
LP-TX	0	3	WC(1)=00, WordCount = 0005 = 5 bytes
LP-TX	25	4	ECC
LP-TX	D0	1	MCSON (D0h)
LP-TX	1	2	parameter 1 = 01 = MCS function ON
LP-TX	5A	3	parameter 2 = 5A = hardcoded, part of command
LP-TX	A5	4	parameter 3 = A5 = hardcoded, part of command
LP-TX	6C	5	parameter 4 = 6C = hardcoded, part of command
LP-TX	B0	0	checksum (CRC)
LP-TX	5B	0	checksum (CRC)
CTRL	**Mark-1**		
CTRL	**EME**		
CTRL	**LPDT**		
LP-TX	13	1	**DI=13 (Generic Write, 1 parameter)**
LP-TX	B5	2	Data(0)=B5 (DISSET3, AREFOFF=1)

Step 2: Compile csv program and store on test module

- **Simple interpretation is performed inside the FPGA for executing the test**

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Conclusion

- We have presented a mechanism by which low-speed ATE can test high-speed digital interfaces
- The solution is based on a SerDes test module that offers low cost and high flexibility
- We have provided experimental results and case studies to demonstrate (a) the need for a new way to test high-speed digital interfaces and (b) a proven solution for doing so