“Edge to Edge” – Pre-Silicon Test Pattern Verification Tool

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AGENDA

- PROBLEM STATEMENT
- OBJECTIVE
- BENEFIT
- ROOT CAUSE
- TOOL FLOW
- RESULTS
- SUMMARY

Is your Test Program Ready ?

PROBLEM STATEMENT

Long lead times in test pattern validation

- Multiple cycles of learning
- Communication Issues : Logic, Documentation
- Different Functional Domains
- Minimal development time (Ineffective communication)
- Minimal standardization (Different types of devices)

OBJECTIVE

Develop a simulation platform to verify ATE stimulus on FULL CHIP netlist :

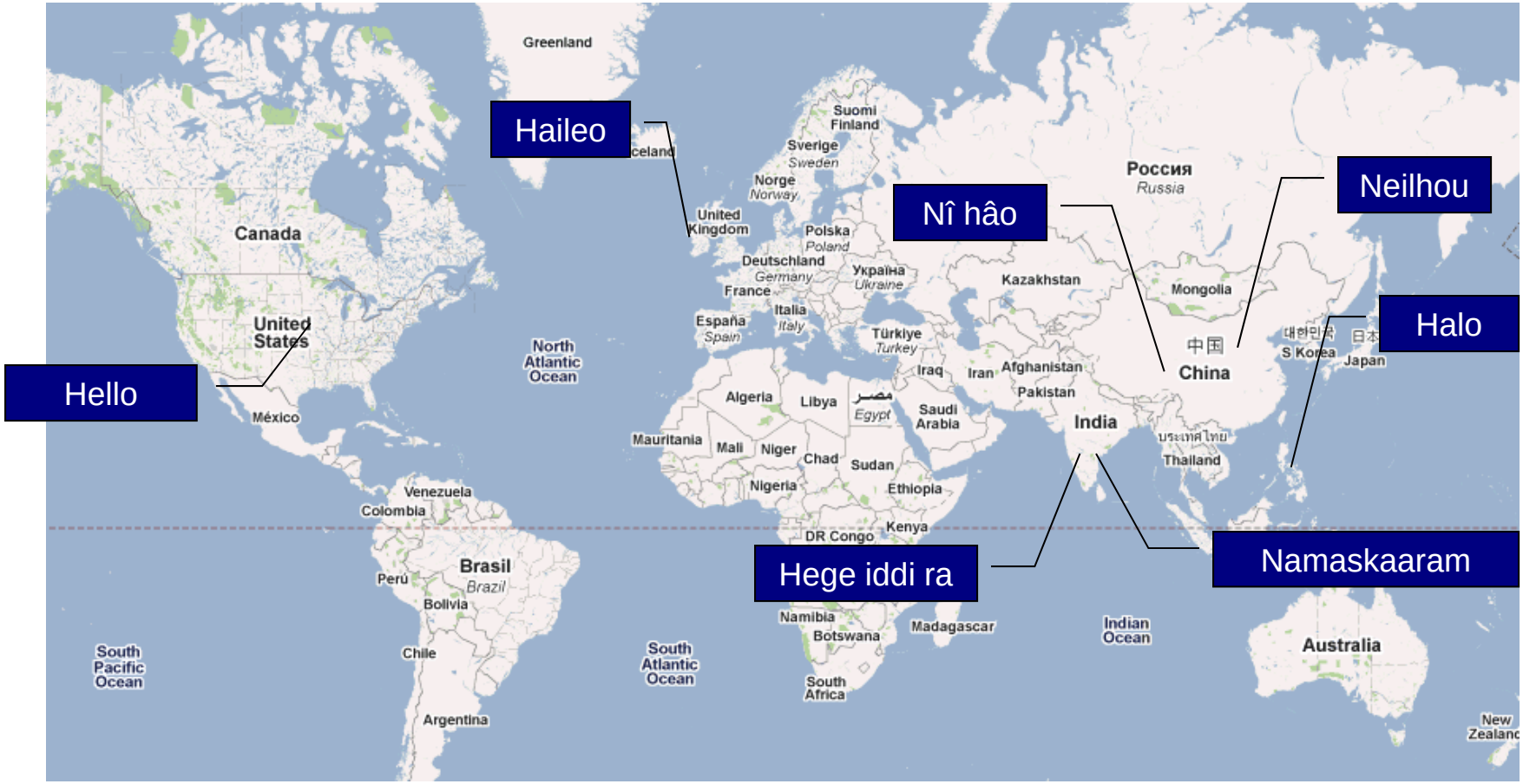
- Identify DFT issues.
- Identify pattern issues prior to tapeout
- Create generic interface for any device
- Emulate all test setups
- No Manual interpretation.
- No fixed functions in RTL/Gate level setups

BENEFITS

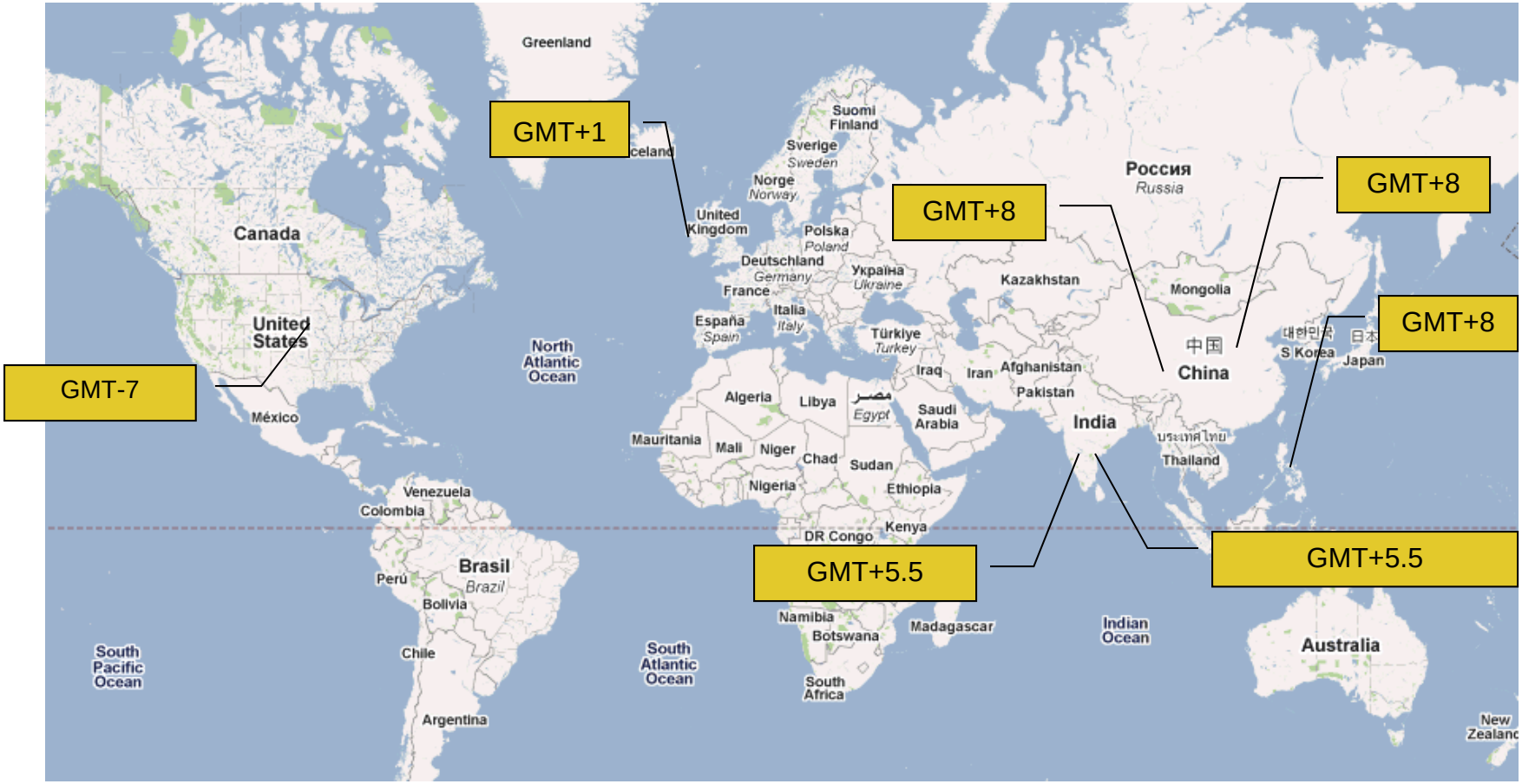
Enable Pre Silicon Validation for all Test Patterns

- Predictable cycle time (1st Silicon – Production)
- Improved First Pass Yield
- True DFT Verification
- Realistic Timing Sims
- Standardized output format

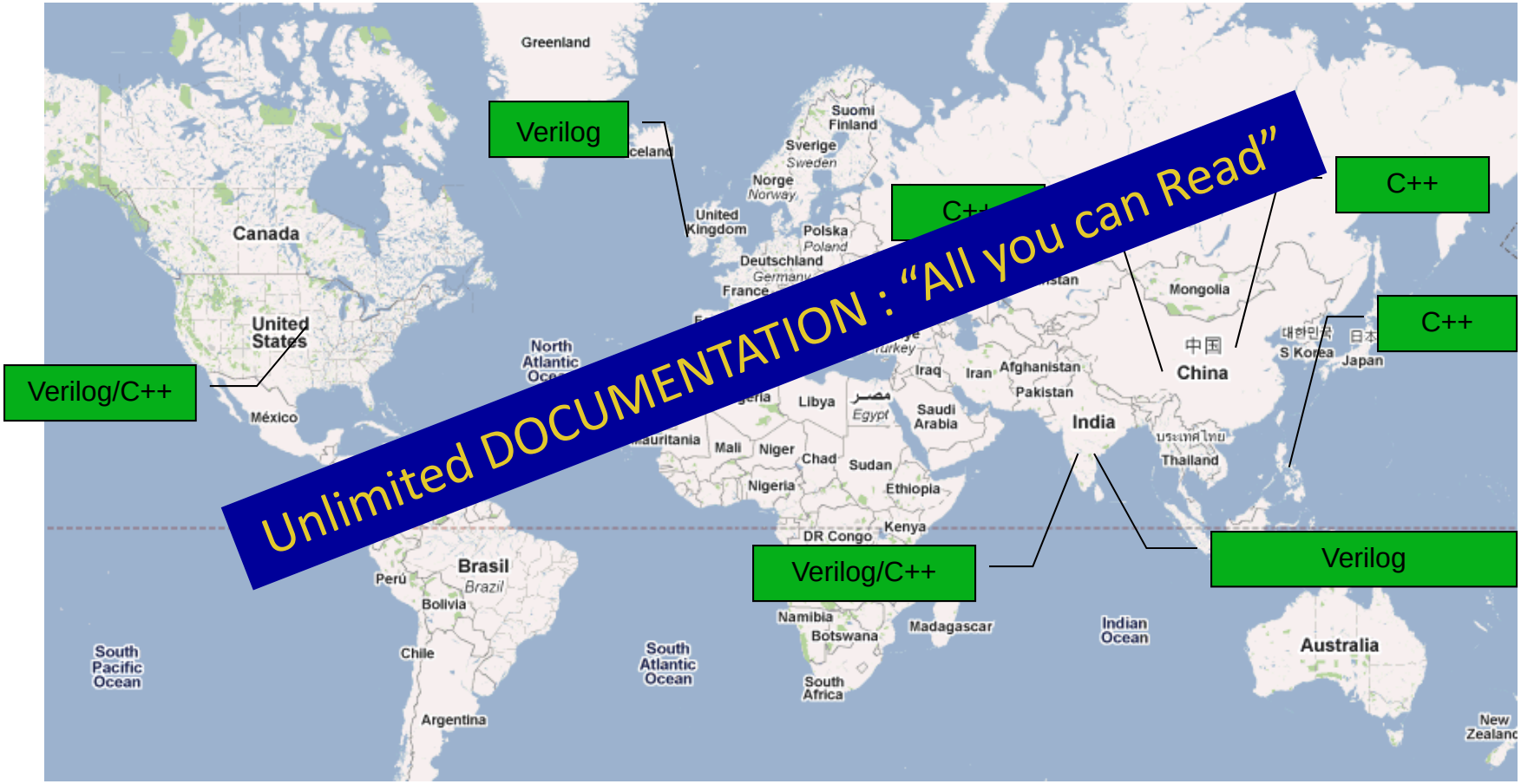
REASON : Communication



REASON : Communication

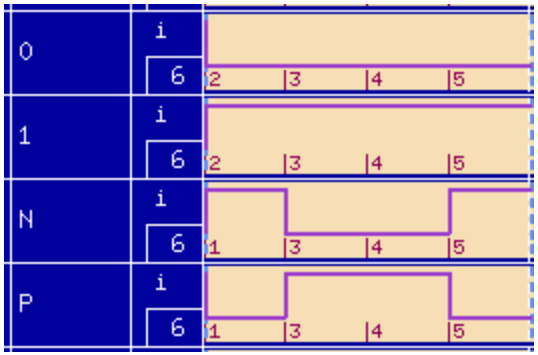


REASON : Communication

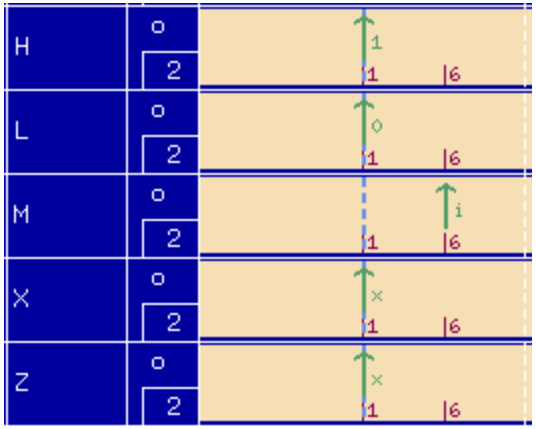


REASON : Drive/Compare Formats

Design Verification Setups : Support Limited Formats

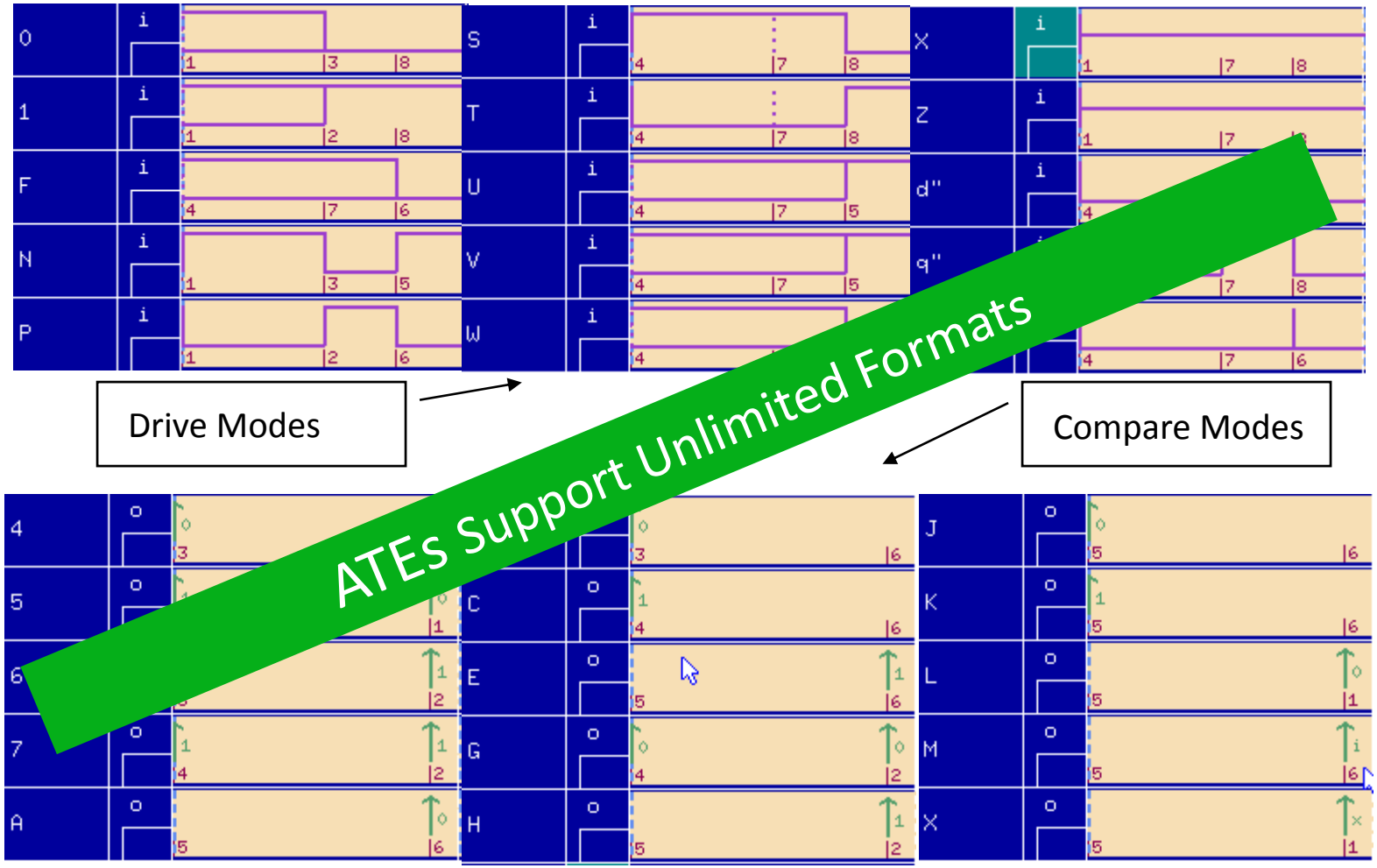


Drive Modes



Compare Modes

REASON : Drive/Compare Formats

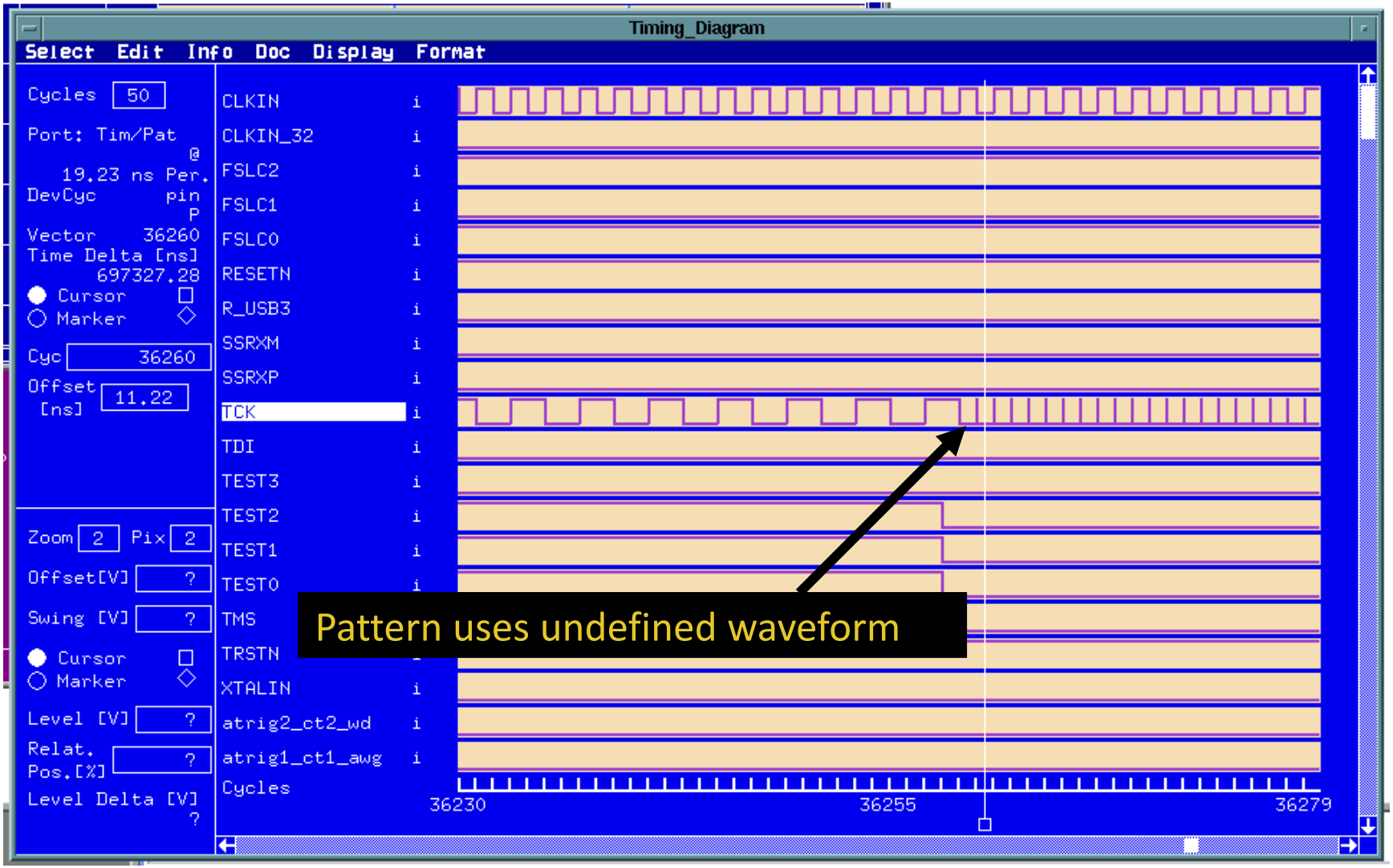


REASON : Timing Equation Validation

Edge Control

- Error in Timing Equation
- Misplaced Search Window
- Pattern does not provide active edge control
- Misinterpreted timing setups

REASON : Device Cycle Mismatch

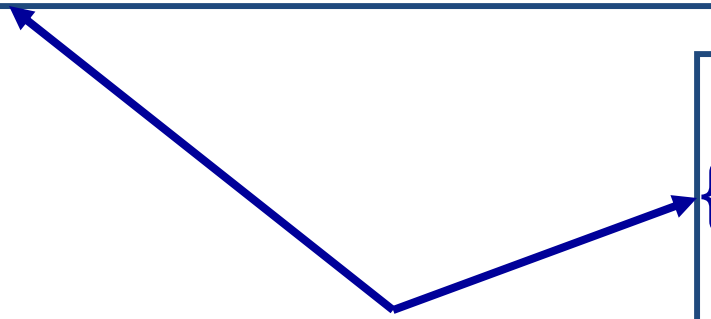


Device Cycle = Waveform/Pattern Character

REASON : Interpretation Errors

Wrong Timing Setups

```
PINS dedi_ins dedi_trigs
0       "d1:FN0 d2:0"                          "0"    # NRZ : 0
1       "d1:FN0 d2:1"                          "1"    # NRZ : 1
e       "d1:F1N d4:F0N"                        "S"    # RC  : 0
f       "d1:F0N d4:F1N"                        "T"    # RC  : 1
10      ""                                     "X"
17      "d1:F10 d3:F00 d5:F10"                 "N"    # SBC : 0
18      "d1:F00 d3:F1N d5:F00"                 "P"    # SBC : 1
brk     ""
```



```
PINS dedi_ins dedi_trigs
PINS ac_pport_ins
d1=0.00*PER
d2=0.00*PER
d3=0.00*PER
d4=0.50*PER
d5=0.50*PER
```

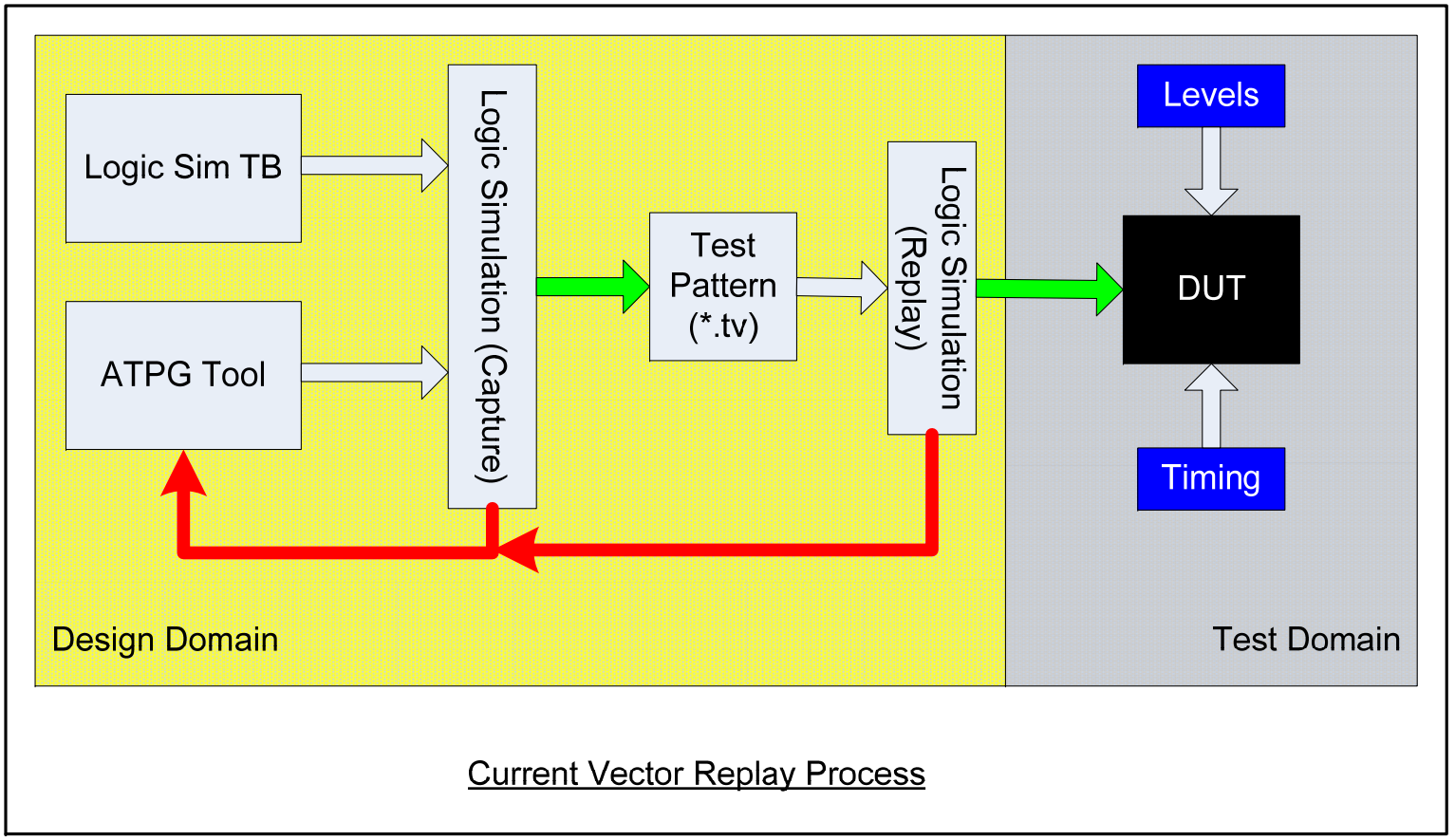
REASON : Interpretation Errors

REASON : Pattern Setup

Top Level Setup Conditions :

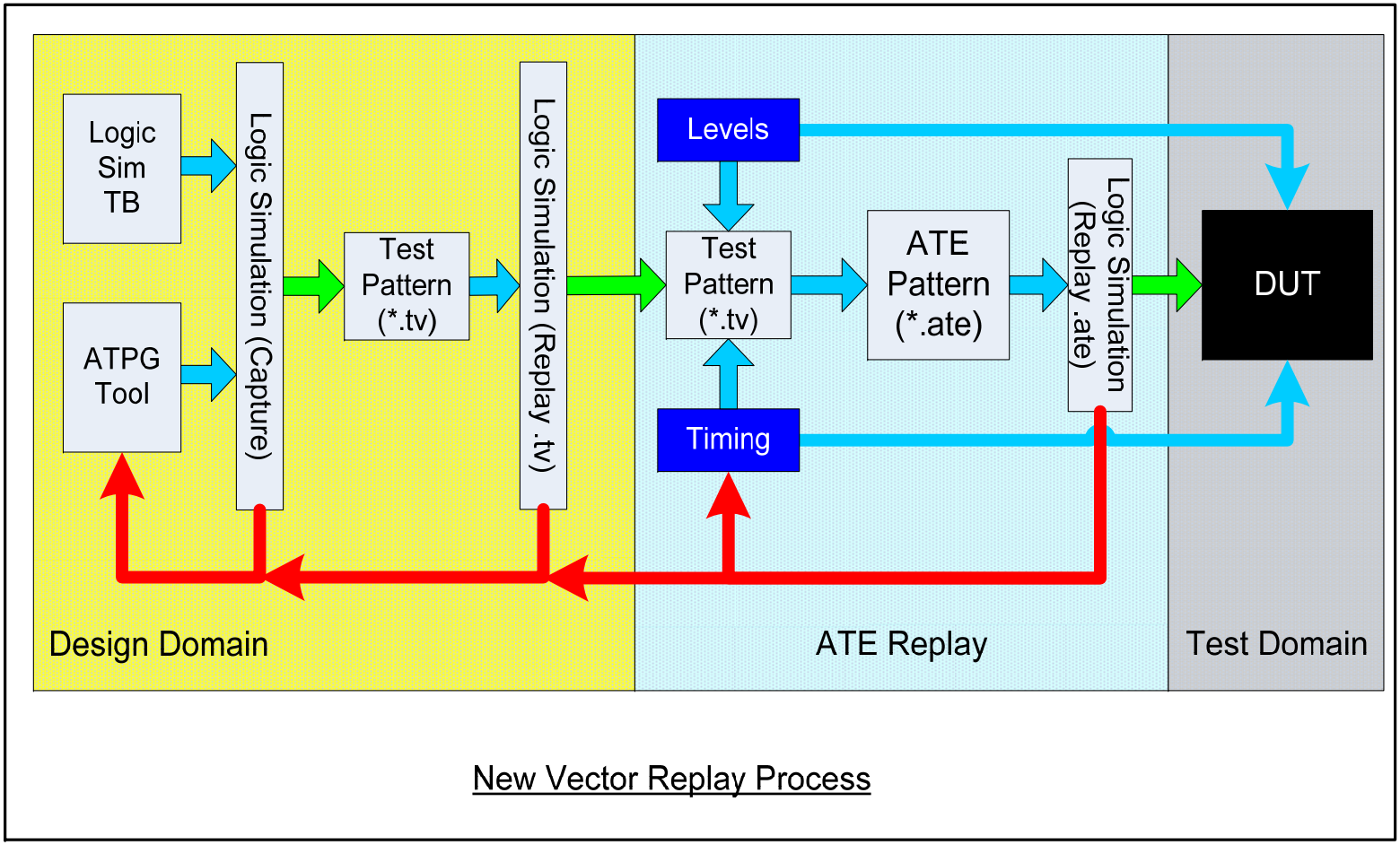
- Pattern Run Frequency
- Capture/Sample Frequency
- External Clocks
- Bond Options
- Reset Pulse Widths
- PLL Lock times
- XTAL Frequencies

Current Process Flow



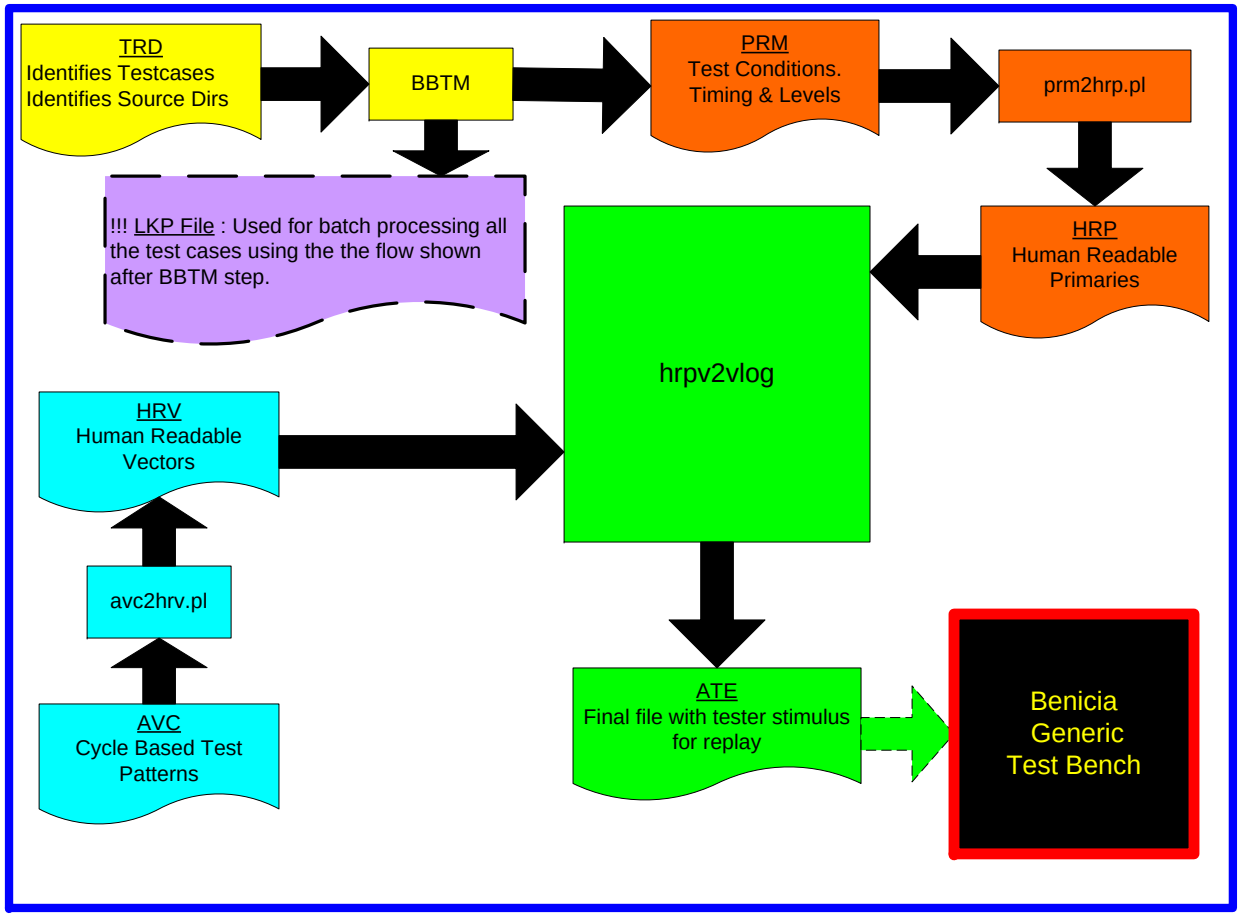
Current Vector Replay Process

Proposed Process Flow



New Vector Replay Process

Tool Flow


TRD
Identifies Testcases
Identifies Source Dirs
BBTM
PRM
Test Conditions.
Timing & Levels
prm2hrp.pl
!!! LKP File : Used for batch processing all the test cases using the the flow shown after BBTM step.
HRP
Human Readable
Primaries
hrpv2vlog
HRV
Human Readable
Vectors
avc2hrv.pl
AVC
Cycle Based Test
Patterns
ATE
Final file with tester stimulus for replay
Benicia
Generic
Test Bench

Test Bench Features

- RTL/Gate Level Simulations
- Supports external bond options
- Synchronous/Random external clocks
- Generic Test Bench for multiple devices
- Sectional Dump file generation
- Internal Node comparison

Simulation Types

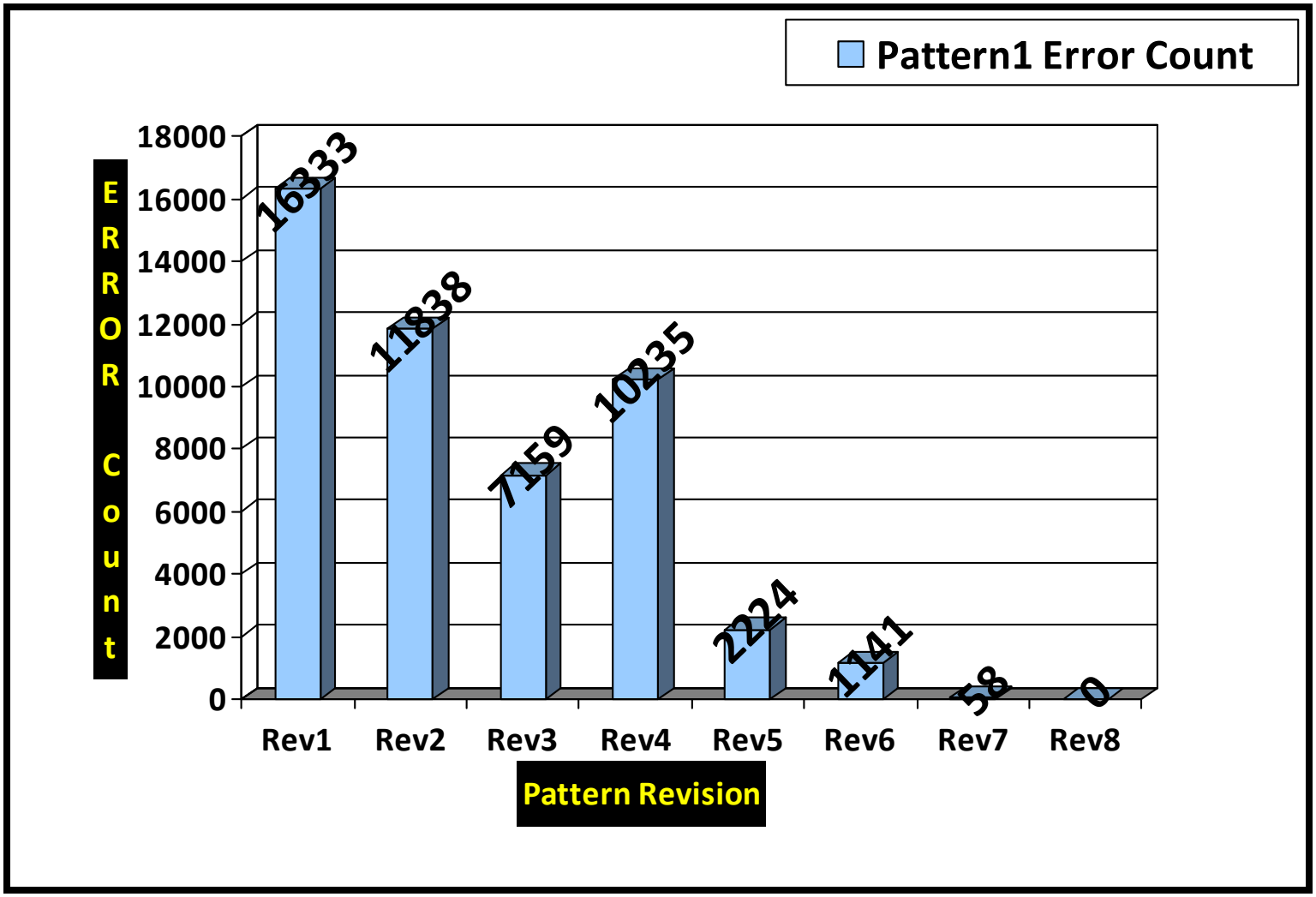
+RTL SIM : Functional Verification of AC patterns

Test Index	Pattern	Timing	P/F
2001	pattern1	tim131	PASS
2002	pattern2	tim141	PASS
2003	pattern3	tim121	FAIL
2004	pattern4	tim111	PASS

+ GATE SIM : AC Verification

Test Index	Pattern	Timing	Spec	AC Testable	Min Spec	Nom Spec	Max Spec
4001	pattern1	tim112	tS	YES	FAIL	PASS	PASS
4002	pattern1	tim113	tH	NO	PASS	PASS	PASS
4003	pattern1	tim114	tCO	NO	FAIL	FAIL	FAIL
4004	pattern1	tim115	tOH	YES	PASS	PASS	FAIL

RESULTS


Pattern1 Error Count
ERROR Count
18000
16000
14000
12000
10000
8000
6000
4000
2000
0
16333
11838
7159
10235
2224
1141
58
0
Rev1
Rev2
Rev3
Rev4
Rev5
Rev6
Rev7
Rev8
Pattern Revision

RESULTS

Average cycles per initial pattern : 6

Types of errors

- Capture Issues
- RTL
- Timing Pattern mismatch
- Wrong Configuration
- Timing Strobe Issues

"Simple bugs" to "Show stoppers"

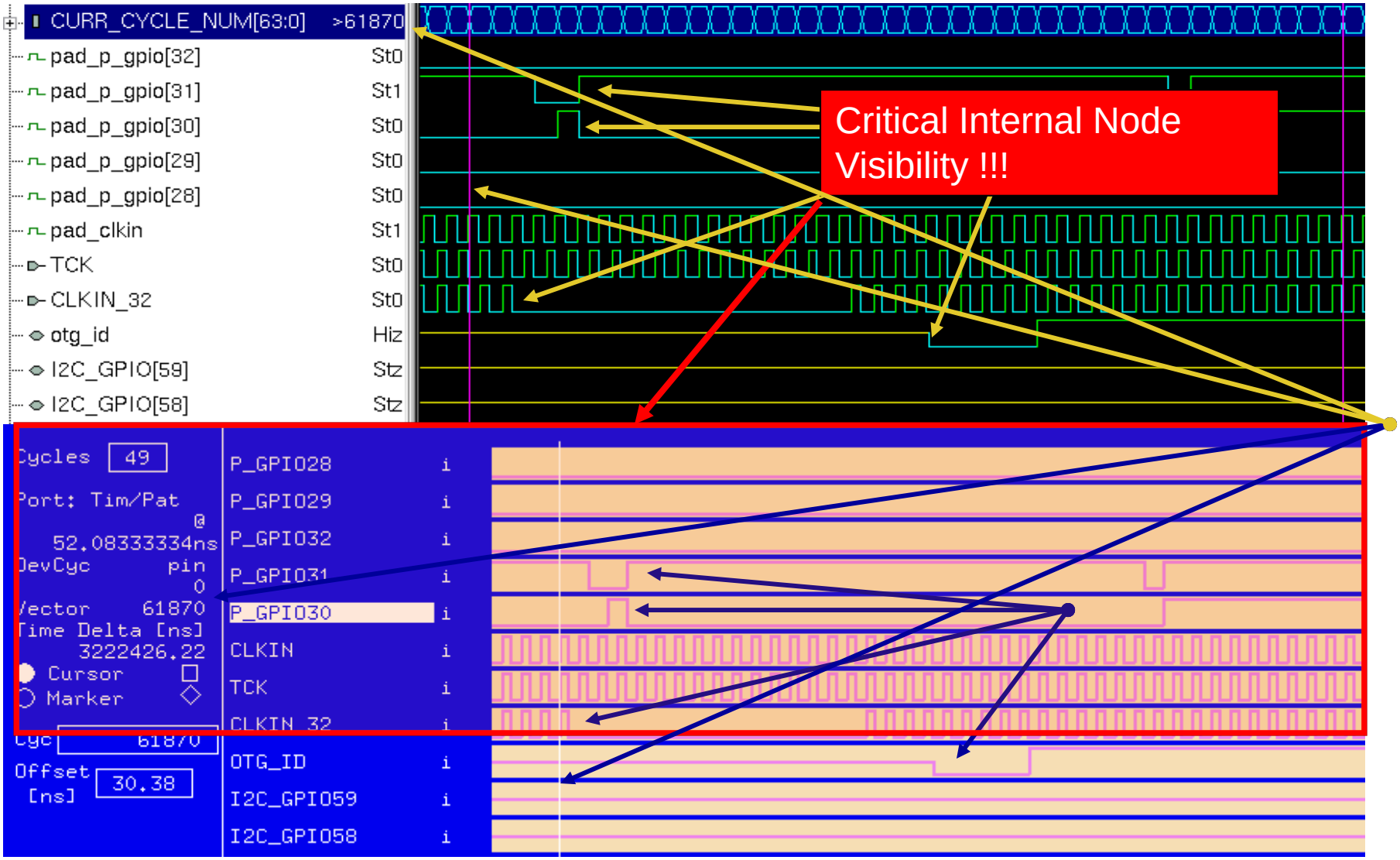
Other Benefits

Identifies bus contention

Better debug through internal node access

Failure Portability

Failure Portability



Failure Portability

Time to Relay the Information

S.No	Task	Manual Process (min)	Edge to Edge Process (min)
1	Functional/Spec_Search Reports a Failure	5	0
2	Capture the Failing cycles	5	0
3	Get the Vector tool to map the failure to a vector number	15	0
4	Call the Designer. Relay the failure information verbally/email	15	0
5	Map the vector number to a line in *.tv file	15	0
6	Open the waveform in the design environment	5	5
7	Vector Number mismatch ?	go back to step 3 or 5	N/A
8	Need ATE setup info	oops ! Call TE	Embedded !

Summary

- 50% improvement on published schedule
- Several setup bugs identified & fixed
- Few show stopper RTL bugs identified & fixed
- TEST simulation platform established
- Communication in common (Design) Language
- Common platform to compare multiple ATE programs
- Expecting to have >90% FPY (pattern)