"Edge to Edge" – Pre Silicon Test Pattern Verification Tool

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***Abstract*—In the current semiconductor environment, the development cycle of any chip consists of mainly Pre & Post Silicon stages. For complex devices, the schedule for post-silicon verification has become the critical path; Post-silicon verification is mainly associated with characterization and production release of the device. The success of this phase is mainly dependent on the accurate merger of the design verification patterns with ATE timing setups. The cycles of learning required to debug these ATE tests can delay the project's revenue stream. In the past, this debug could not start without functional silicon. In this paper we describe a new tool that jump starts the process by providing a platform to validate the merger of patterns and custom ATE timing setups during the pre-silicon design phase. This new process guarantees 100% correct functional patterns and timing in the ATE environment prior to first silicon.**

BACKGROUND

A semiconductor development cycle consists of different phases that can be categorized as the pre & post Silicon. As the name refers, post silicon cycle starts with the first physical silicon.

The pre silicon phases consists of the following tasks

- Device Definition (incl. DFT)
- Design
- Functional and Timing Verification
- Tapeout

The post silicon phase consists of the following tasks

- Characterization Test
- Production Test
- Qualification
- System Verification
- Manufacturing

The product revenue is highly dependent on the post silicon phase as much as the pre silicon design cycle. In today's semiconductor world, any improvement in the cycle time will help the product to be in time to market and be successful. The process presented in this paper helps to compress the post silicon cycle time.

INTRODUCTION

The most critical task after 1st silicon is the Test Program development. The program development consists of pin, levels and timing definitions combined with patterns. The patterns for these programs are generated using verilog models, test benches, atpg and hand generated scripts.

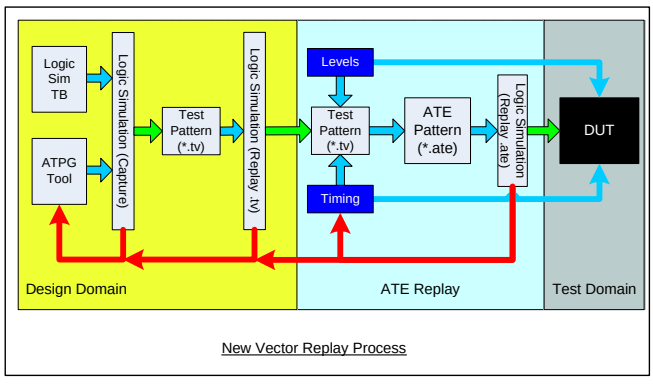
These patterns are translated to the ATE environment and applied to the 1st silicon to perform different kinds of tests. The tests vary from a simple DC and SCAN to more complex AC and Analog tests. This pattern development and implementation process involves multiple variables that can cause the test setups to fail at the first implementation.

Several factors limit first pass yield (FPY) of the test patterns, causing multiple development cycles. The patterns are developed and simulated in design environment which may vary from the test setups developed by the test engineer who may interpret or apply the timing differently from the designer. The first silicon is the real test vehicle where the merger of the patterns and the timing will be validated to move further with the characterization needs. Today's SOCs may have ~500 parameters resulting in ~300 patterns. The sheer magnitude makes the schedule unpredictable and will put the revenue stream at high risk.

The fundamental mismatches between the pattern and timing setups can be caused by several issues. Some of them are listed below:

- ✓ Communication : Logic, Documentation, Cultural
- ✓ Information transfer between different functional domains
- ✓ Minimal development time (Tapeout to First Silicon)
- ✓ Impossible to standardize between devices
- ✓ Simulation sampling schemes under-use the ATE capability
- ✓ Misinterpreted Test Setups
- ✓ Pattern setup conditions
- ✓ Inefficient DFT sims

It is highly desired to develop a new platform to simulate the ATE setups in the design environment to eliminate these barriers. The fundamental advantage of this kind of process is that it enables debug of test vectors in parallel with the design phase, and this helps to have a smooth transition from first silicon to volume manufacturing. The main benefit of this process is that FPY approaches 100%. The new process brings the ATE setups into the design environment for simulation as shown in the following figure.



New Vector Replay Process

IMPLEMENTATION

"Edge to Edge" platform is generic work across multiple ATE platforms and is targeted for use across several device families. The initial implementation is to support on 93K test platform and is targeted on a device that is 1.5 million gate SOC (Logic, Memory, Analog, High Speed Serial).

The current flow is embedded into cypress Block Based Test Methodology (BBTM) flow such that all the test cases are simulated as actually implemented in the final test program. The following are the several components of this new platform

1. BBTM-TRD (Technical Requirements Document) : This is a simple csv file that is used to specify and direct the actual production and characterization test programs. This flow enables the user to choose the tests that need to be run at different steps in manufacturing. The E2E process is treated as one of the manufacturing steps in the TRD. The user enables the cases that need to be simulated by marking them for inclusion in the "E2E test flow." The BBTM shell generates the timing and levels files (PRM) required for all the regression cases and also generates a lookup file with a list of the cases that need to be simulated

2. PRM -> HRP: This tool reads a tester specific PRM file and creates HRP files that are a tester independent format for the tester's Timing and Levels settings.

3. AVC -> HRV: The avc files are cycle based text format vector in 93k "ascii" format. In this stage all the required avc files will be converted to a tester independent format defined for the E2E process. This process is tester dependent and requires a tester specific translator

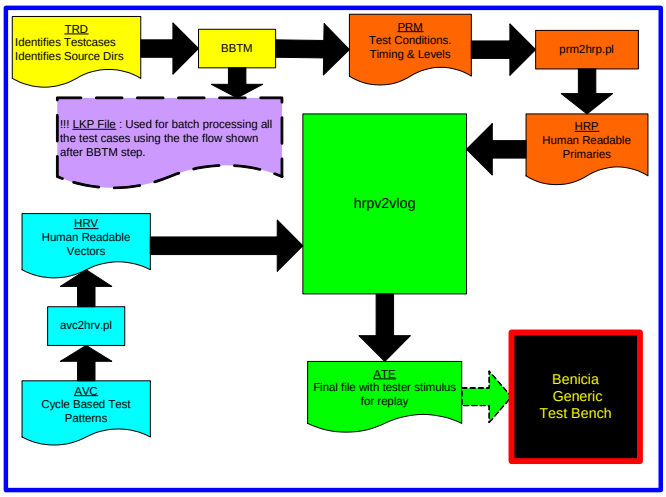
4. HRP & HRV -> ATE: The ATE file is a stand alone file that contains the merged information of pattern, timing and levels. It is generated from the HRP & HRV files for all test cases based on the lookup file.

5. Testbench: A generic test bench is developed such that it is portable across device families. All the variables are defined as a setup/config files. Only the power and ground nets are initialized. All the internal states such as reset, pll lock etc., are left uninitialized, and respond only to the actual tester input activity, and the device model. The test bench includes signals that indicate the exact tester cycle to help locate problems in the tester vector files, that are found in the simulation waveforms.

6. Simulation: ATE files are used to apply the stimulus using the generic test bench on the top level netlist. This platform supports RTL and Gate level netlists for simulation. It allows the user to use external clocks, bond options to emulate real test setups.

7. Output: Simulations will generate a dump file and fail log that can be used to trace the failures back to source pattern files. The dump files can be used to explore the fail conditions and trace it back to root cause based on the state of internal nodes.

The process flow is as shown in the figure below, the source of the stimulus is derived from a completed test program which is applied on the complete net list. The result is "Edge to Edge" match of every event on every pin of an ATE test case on design environment. This will eventually push the FPY closer to 100%.



RESULTS

This simulation platform provides an excellent solution to checkout the test patterns and test setups in the design environment before the 1st silicon. This helped us understand and resolve multiple design and test program errors prior to tape out. These errors range from simple test coding bugs to critical DFT architectural problems. Based on the results we are expecting 50% improvement on published post-silicon schedule. The RTL & Gate Level simulations provide functional verification and proves that the test cases are useful for device timing parameter characterization.

CONCLUSIONS

This process improves cross-functional communication by allowing the test engineers and design engineers to collaborate on test development and debug in a common environment. The success of this software can be measured by the smooth transition from 1st silicon to manufacturing. The many bugs that were identified and fixed before silicon using the E2E process is phenomenal and provides a compelling case for using this process across all future products at Cypress.