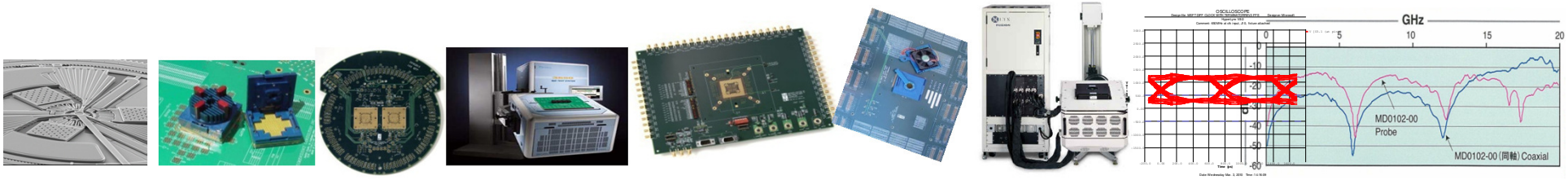
PRESTO Engineering

Silicon Valley TEST Conference & Expo San Jose Nov. 8-9, 2010 www.svtest.com



First-Silicon Encounters

Frank Sauk, VP of Engineering and Co-Founder
Presto Engineering, Inc.
frank.sauk@presto-eng.com
www.presto-eng.com

Presto Engineering--Who are we?

Our mission is to support our customers

in accelerating new products release

and in improving product yields

We provide test and analysis solutions complementary to internal resources

…where expertise is scarce or unique

…where capabilities are costly or unusual

We deliver DESIGN SUCCESS ANALYSIS™

PRESTO Engineering

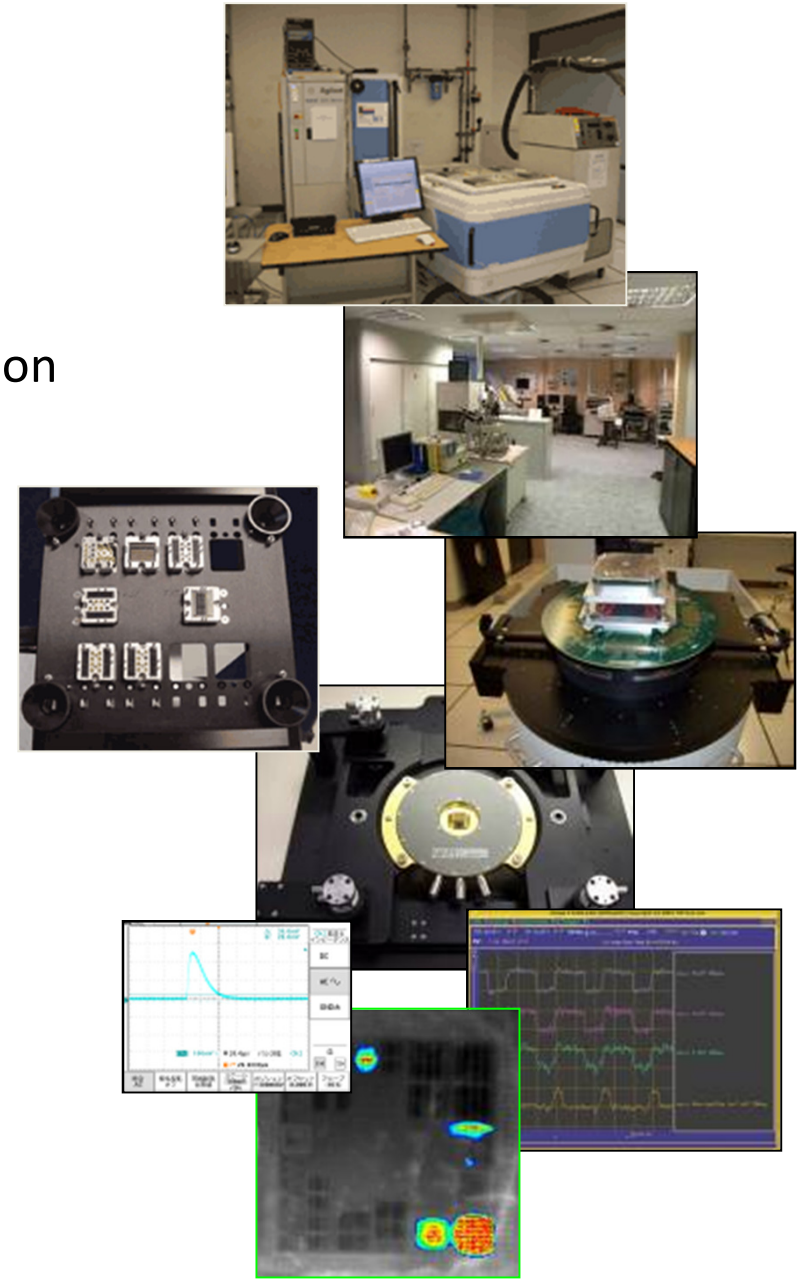
Presto Engineering

- **Silicon Valley Hub (San Jose, CA)**
  - Test, Reliability, Failure Analysis
  - ISO 9001
  - CPU, GPU, FPGA, memories
  - Two patents filed
- **Caen Normandy Hub**
  - Test, Reliability, Failure Analysis
  - ISO 9001 (17025 Q3-10)
  - Advanced RF
  - Modules, SiP, electronics
- **Grenoble R & D**
  - Advanced Test
  - CEA-LETI common lab
  - R&D on 3-D/TSV

PRESTO Engineering

Our Offerings

- **Lab Services**
  - New product validation and qualification
  - Test development and pre-series
  - Product analysis and debug
  - Reliability and failure analysis
- **Lab Products**
  - All lab-related interface solutions
  - Test systems evolutions
  - Specialty thermal assemblies
- **Lab Operations**
  - In-sourcing
  - Comprehensive outsourcing



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First-Silicon Encounters…

the good, the bad and the ugly

First-Silicon Issues
Case Studies 2009-2010

- Scan-chain Failures
- Excess leakage current
- Signal integrity
- Timing

Note: This presentation is based on a whitepaper, available from our website : **www.presto-eng.com**

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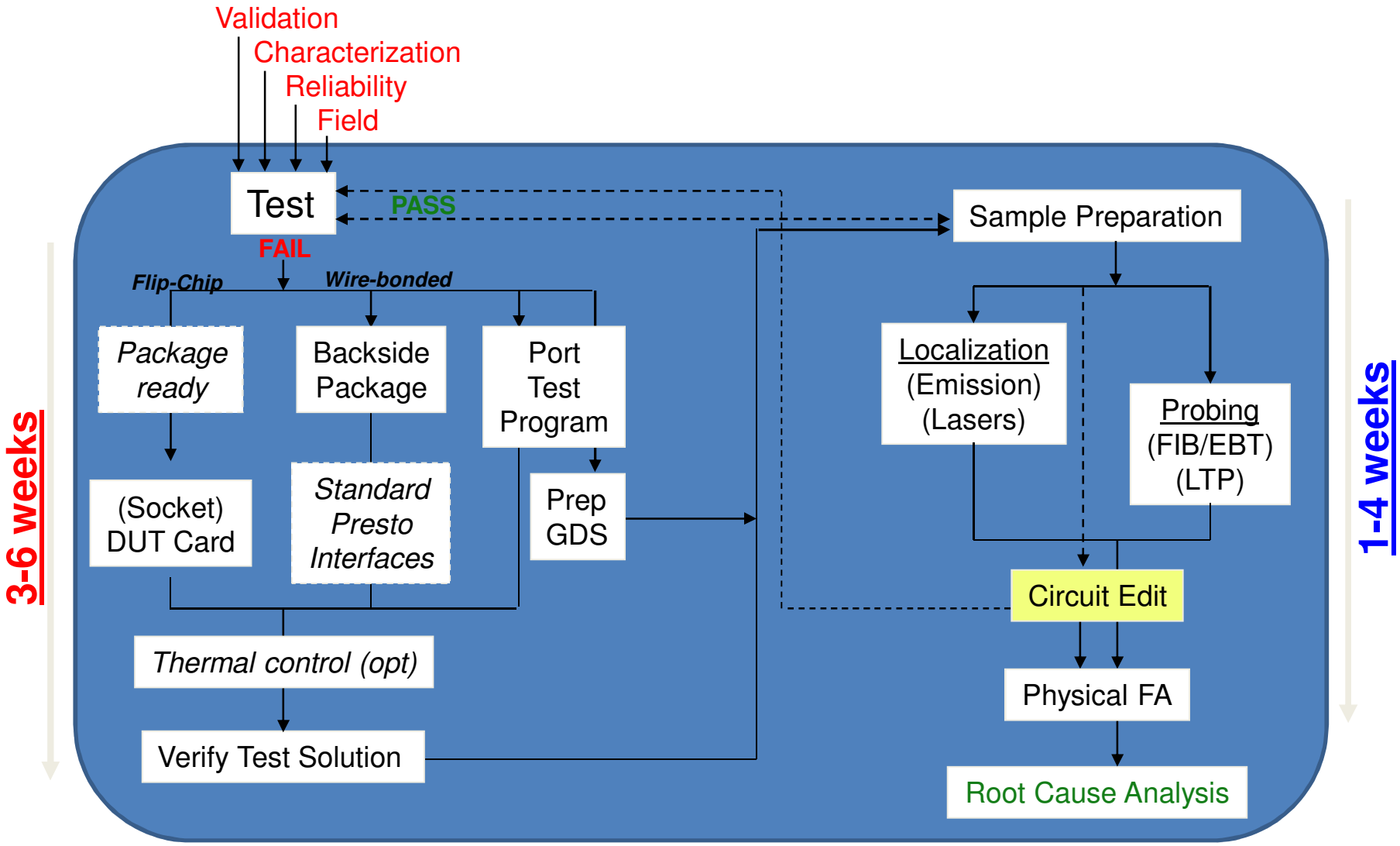
Diagnostic Flow for Debug



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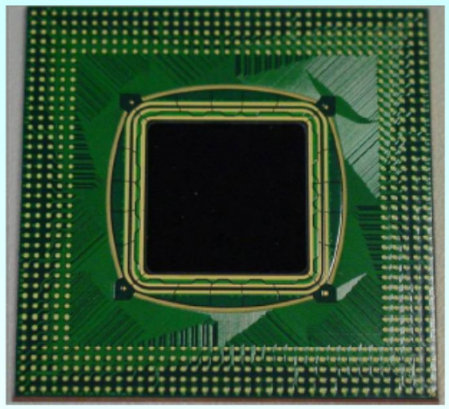
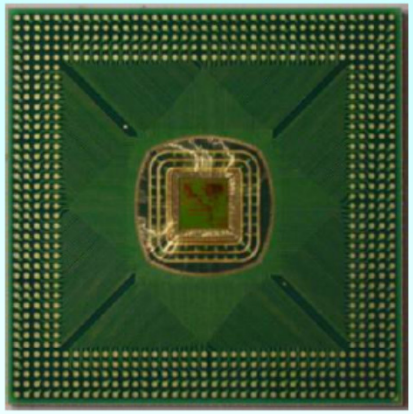
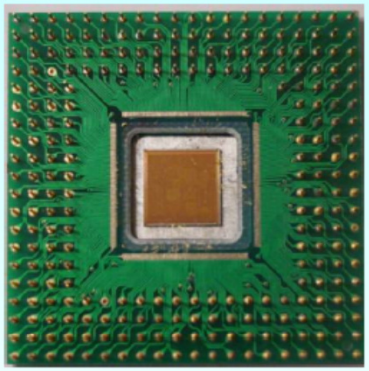
Packaging Options for Back-side Silicon Analysis







	680 BGA	532 BGA	256 PGA
Cavity	15mm	7mm	18mm
Pad opening	23mm	14mm	20mm
# of IOs	476	328	256

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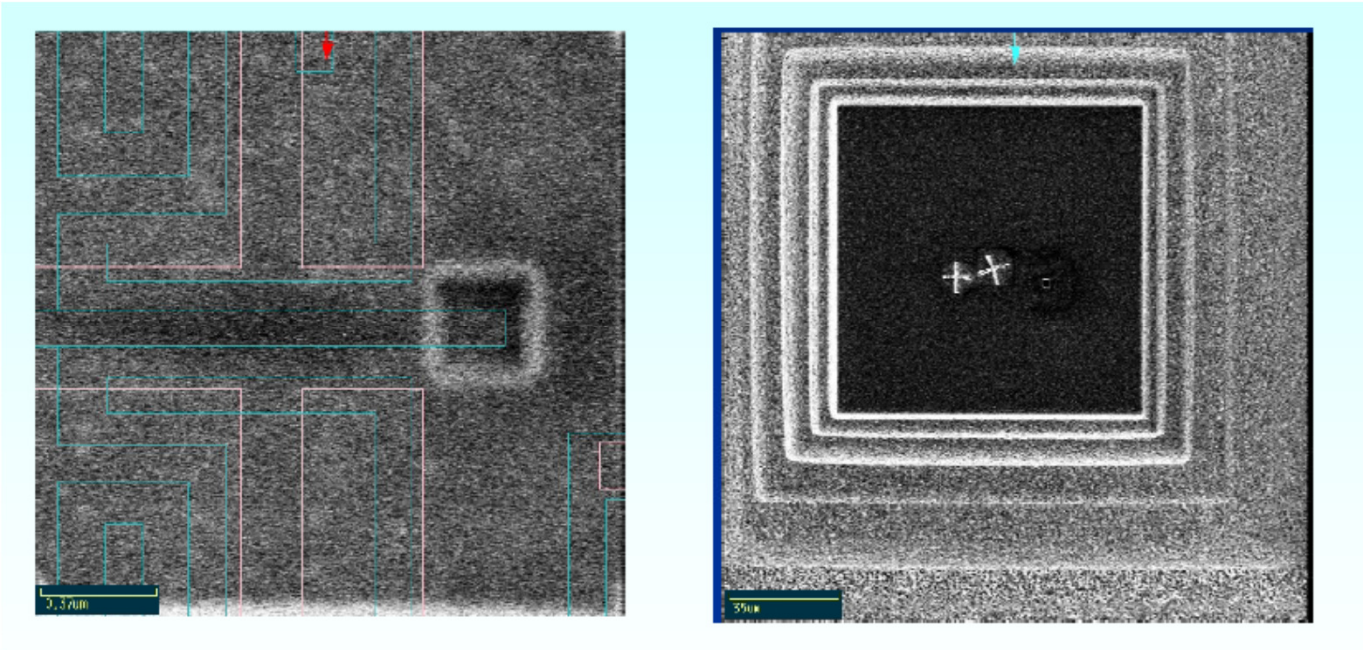
B/s Probe Pads for Debug



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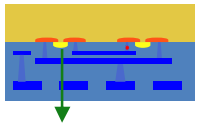
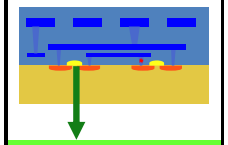
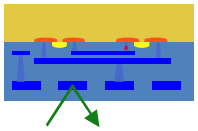
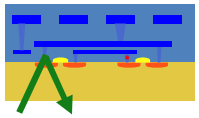
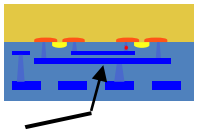
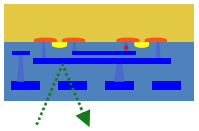
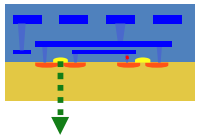
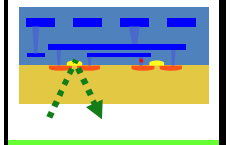
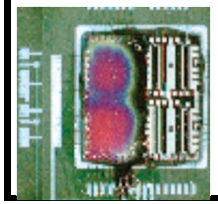
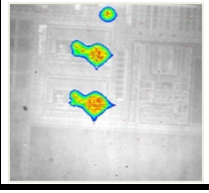
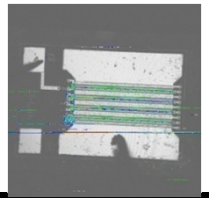
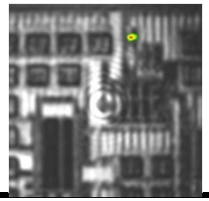
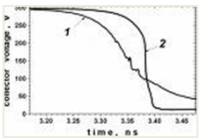
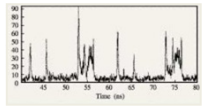
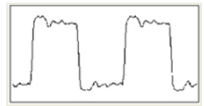
In-Silicon Analysis Techniques

Localization (PFI: global techniques)				Timing/probing (EFA: local techniques)			
Leakage		Interconnect		Metal-Diffusion		Channel	
							
Visible emission	Infra-red emission	Visible laser	Infra-red laser	Mechanical probe	E-Beam	Infra-red emission	Infra-red laser
Photons as a function of current		Optical Beam Induced Current (1064nm) OB Induced Resistance Change (1340nm)		Direct contact	Electrons as a function of voltage	Photons as a function of transient current	Laser modulated by voltage
							

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In-Silicon Timing Signal Acquisition

	Mechanical Probing	E-Beam	LVP	TRE	LTP
		Electron-beam probing	Laser Voltage Probe	Time Resolved Emission	Laser Timing Probe
Preparation	FIB required		Silicon thinning 150um	Silicon thinning < 100um	Silicon thinning ~ 200um
Measurement	**Voltage**	Timing	Timing	Timing	**Timing**
Invasiveness	**Probe points**		Some (1064nm)	None	None (1340nm)
Bandwidth	1GHz	5-8GHz	10+GHz	10+GHz	**10GHz Path to 40GHz**
Jitter	Scope	10ps	10ps	12ps	Scope
V resolution	**µVs**	100mV	Qualitative	N/A	Qualitative
Min V swing	mVs	100mV	400mV	800mV	300-400mV
Process readiness	FIB dependent		65nm w/IL	45nm w/SIL	**40-32nm**
Throughput	4-5 signals/hr	5-10 signals/hr	1 signal/hr	< 1 signal/hr below 1V	10-20 signals/hr

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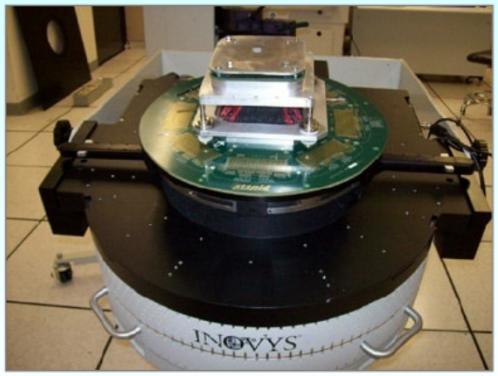
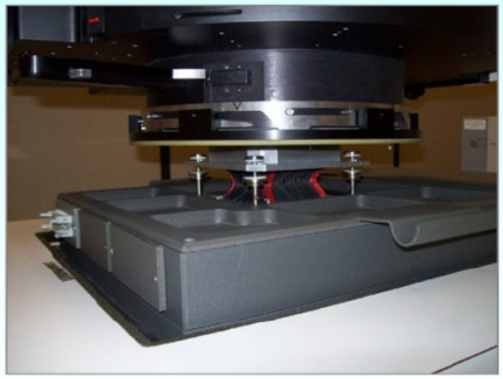
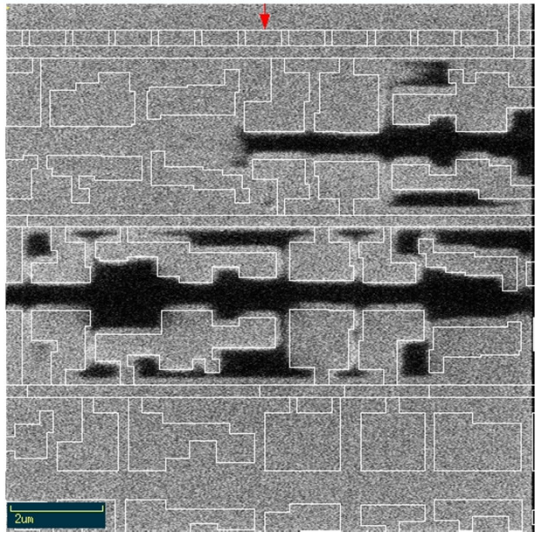
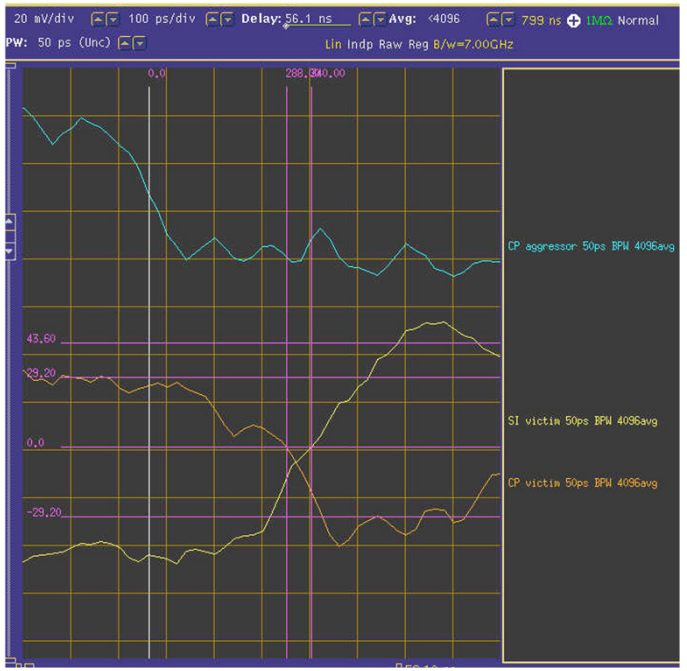
Back-side Silicon Timing Measurements









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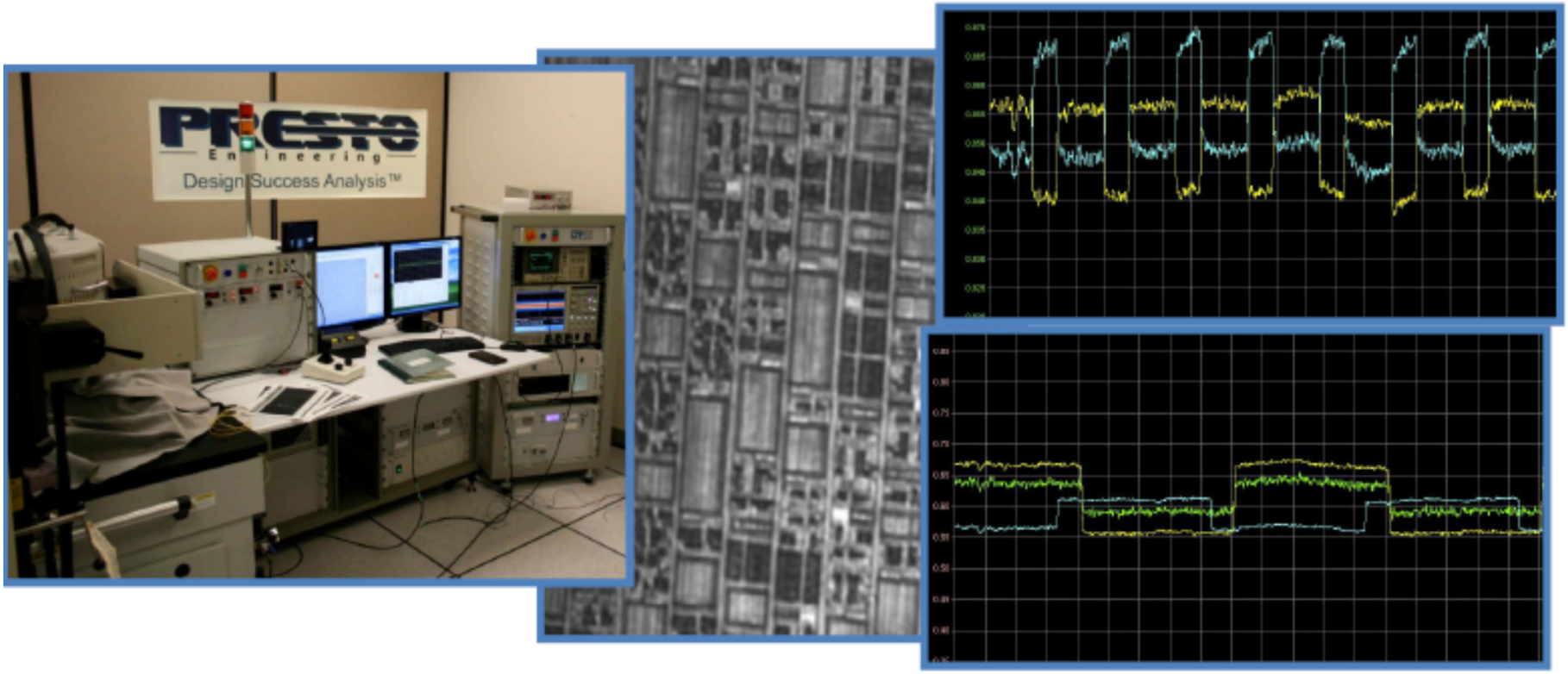

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