



MICROPROBE
Relentlessly Delivering Results

Meeting the Economic and Technical Challenges of Wafer Test

Silicon Valley Test Conference, 11/9/10

Agenda/Outline

- Introduction to MicroProbe
- Meeting the Challenges of Wafer Test
 - Technical innovation delivering improved economics
- Case Study – Increasing the Value of Test
 - Graphics processor yield improvement
- Case Study – Decreasing the Cost of Test
 - Consumer mobile SoC parallelism increase

MicroProbe is a Leading Supplier of Logic/RF/SoC Probe Card Technologies and Products

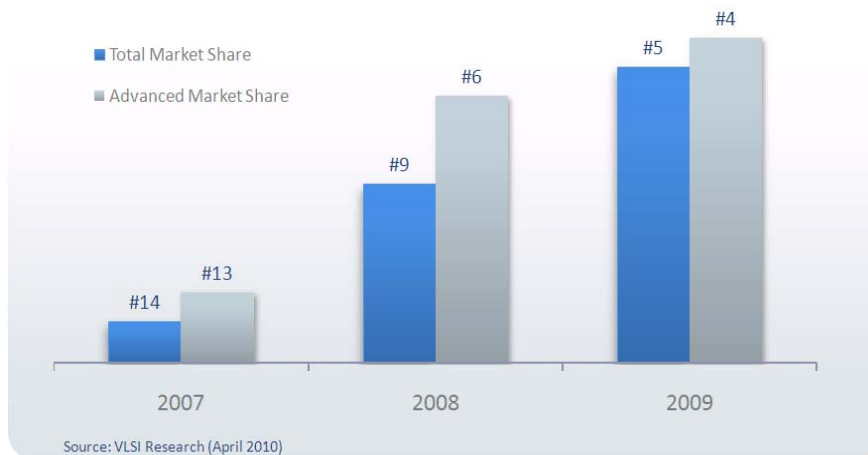
Innovation and Growth

- Technology Leadership
 - >500 MEMS probe cards delivered
- Market Share Growth
 - From #14 in 2007 to #5 in 2009
- Customer Collaboration
 - 35-year history of delivering results are committed



Breadth and Stability

- Broad Product Portfolio
 - Cantilever, Vertical, and MEMS
- Global Presence
 - Major facilities in China, Taiwan, US
- Strong Institutional Investors
 - Flywheel Ventures, Gemini Investors, Intel Capital



The Cost *and* Value of Test

- Continued (and Even Increasing) Focus on the Cost of Test
 - 85% of respondents to ITRS '09 survey expect cost of test to become their biggest concern going forward
- To Maximize ROI, We Must Also Increase the Value of Test
 - Enabling die shrinks, increasing yield, etc.

“A cynic is a man who knows the price of everything and the value of nothing”

- Oscar Wilde

- Capital Cost
- Tooling Cost
- Maintenance

**Lower
Cost of Test**

- Yield
- Die Size
- Chip Reliability

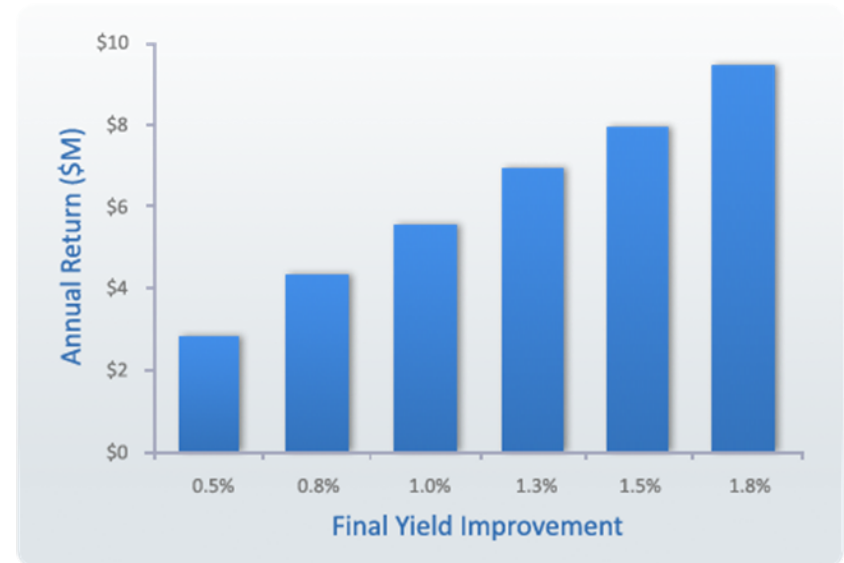
**Increase
Value of Test**

ROI

$$ROI = \frac{\text{Return (Value)}}{\text{Cost}}$$

Case Study – Improving Final-Test Yield Through Tester/Probe-Card Integration

- Problem – Yield Impact
 - GPU failures undetected at wafer sort
 - Frequency above toolset bandwidth
 - Detection at final test only
- Solution – Increase Bandwidth
 - Integration of tester and probe-card
 - Eliminate impedance and transitions



Result: >\$2M Annual Return

- >6Gbps broadband signals accessible at wafer test
- Failure mode detected before packaging and final test
- Enables high-frequency Known-Good-Die (KGD) test (eg, WLCSP applications)

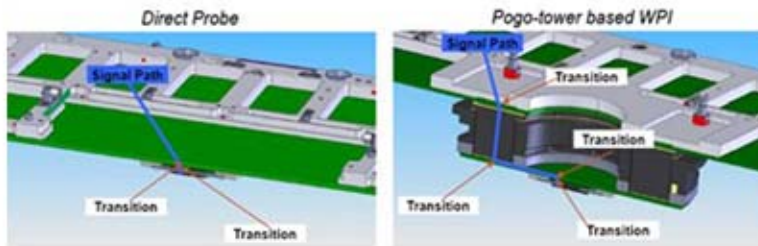
Tester/Probe-Card Integration Increasing Signal Bandwidth and Fidelity

Method

Verigy 93k Direct Probe™ with MicroProbe Apollo

Application Signal Bandwidth

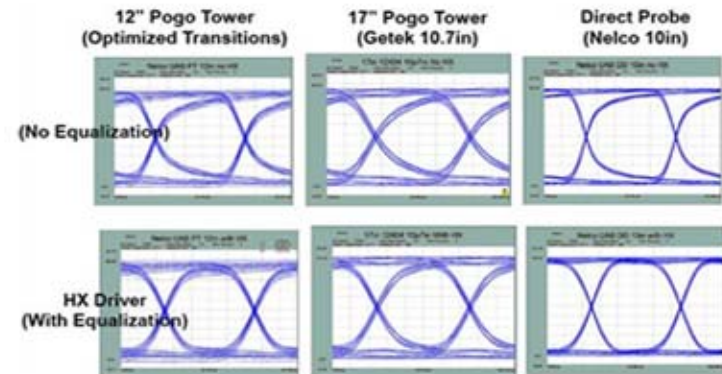
HIGHER BANDWIDTH – Direct Probe reduces the number of signal path transitions between the tester to the probes



Result

Increased Bandwidth to Access >6Gbps Signals

Application Signal Bandwidth (6.4 Gbps)

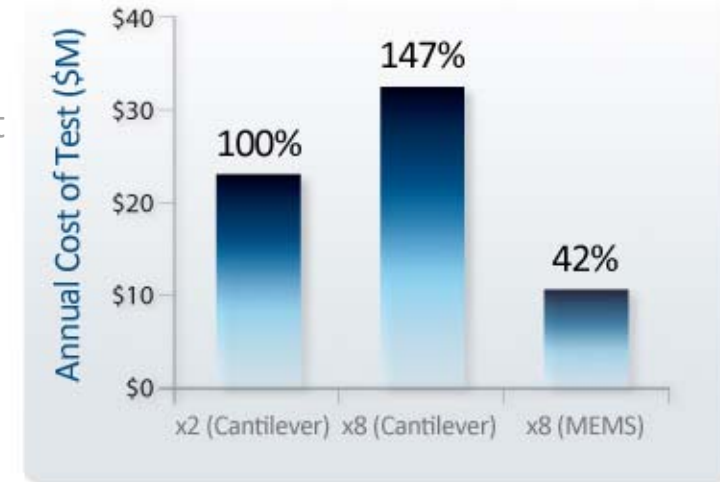


Selected
"Outstanding
Hardware Paper"
at VOICE 2010



Case Study – Improving Cost of Test With Higher Parallelism

- Problem – Cost and Scaling
 - Consumer SoC in competitive market space
 - Existing x2 (2-DUT) testing higher cost than budget
 - Leading edge process & packaging technology
 - 40nm process with 50um pad pitch
- Solution – Increased Parallelism:
 - Mx-FP x8 MEMS probe card
 - Reduced downtime at $\leq 50\mu\text{m}$ pitches



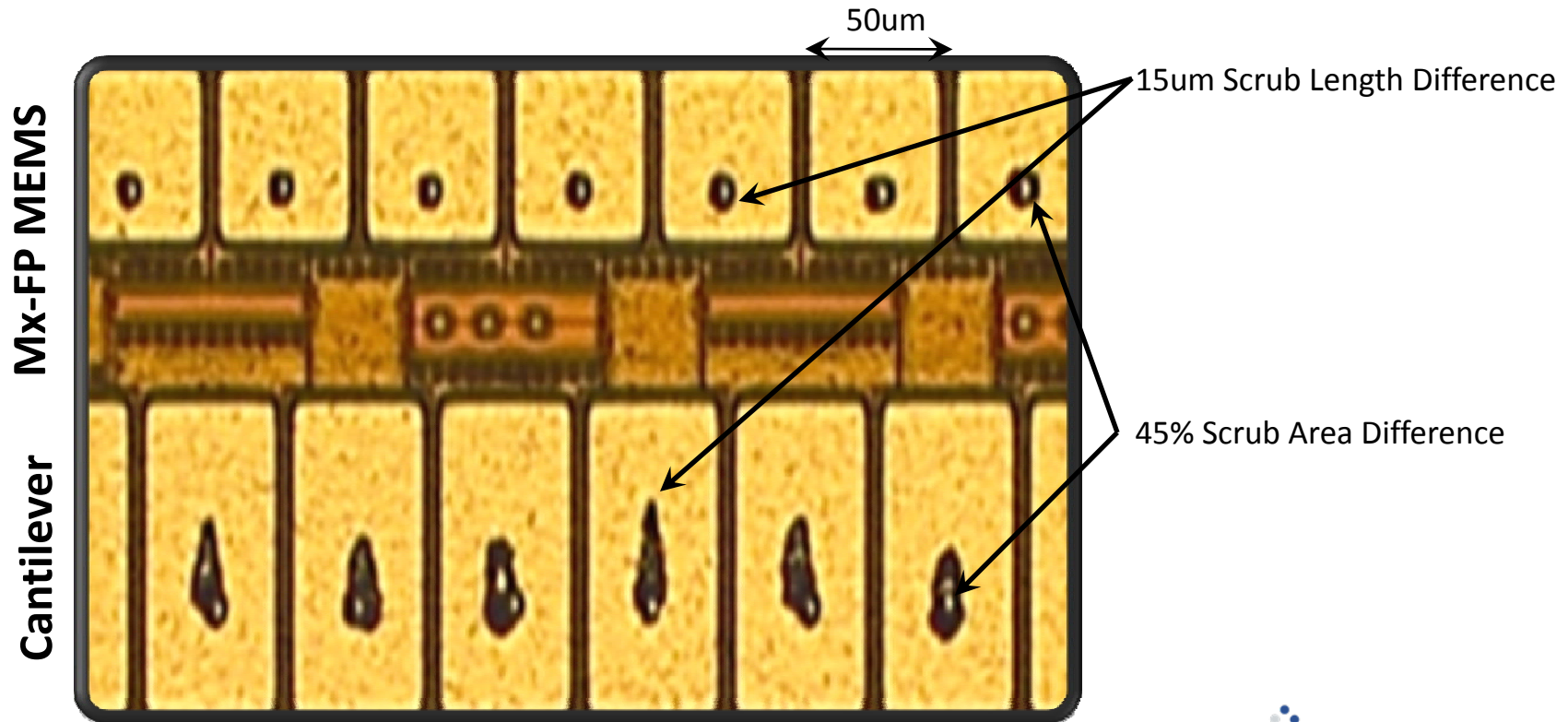
ISMI Model: 10k WSPM @ 3000 DPW, 4 sec/TD
\$80-\$120/hr test cell

Result: 50% Cost of Test Reduction

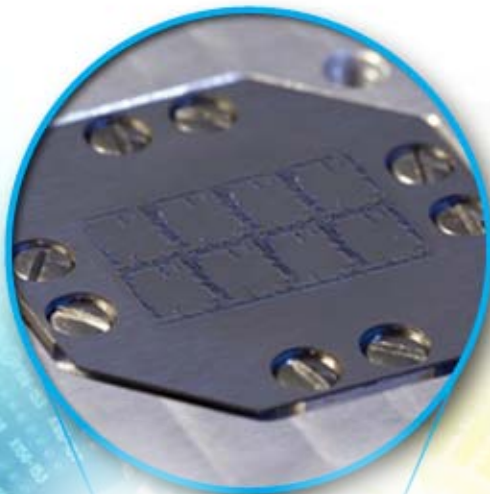
- >\$10M total cost reduction from existing x2 benchmark
- 20 fewer test platforms required

MEMS Probe Card Enables Productive x8 Multi-Site Fine-Pitch Testing

- Pitch/pad-size shrinks demand reduced probe-placement and scrub uncertainty
 - MEMS fabrication provides micron-level accuracy and repeatability
- Cantilever requires significant increase in maintenance at $\leq 50\mu\text{m}$ pitch
 - Results in reduced test cell uptime, increased labor costs



MicroProbe: Collaborating to Improve The Cost and Value of Test



MEMs x8 Probing:

>\$10M Cost Decrease

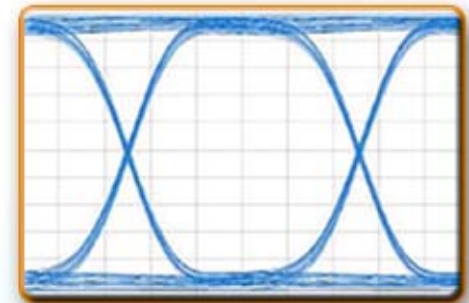


**Increase
Value of Test**

**Lower
Cost of Test**

ROI

Direct Probe Integration:
>\$2M Value Increase





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