A Block Based Test Methodology (BBTM) for Verigy 93K Platform

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AGENDA

- PROBLEM STATEMENT
- OBJECTIVE
- BENEFIT
- OLD METHOD VS. NEW METHOD
- BBTM COMPONENTS
- MONEY SAVINGS

PROBLEM STATEMENT

– Long lead times in test program development
– Complex interface
– Minimal reuse of tIP© (Test IP blocks)
– Personalized coding and localized best practices
– Flex resource allocation not possible
– Redundant learning (different flavors of the same test)

OBJECTIVE

- Develop tIP© reuse system
- Create generic interface for any device

BENEFITS

- Faster development cycle
  - Code re-use and corporate-wide tIP development
- Standardized coding and global best practices
- True flex resource allocation
- Portability
- Efficient knowledge base
  - Example: need to understand only one leakage tIP block
- Standardized production and char functions
- Standardized output format
- Simple, flexible interface

Background : 93k Test Program Requirements

Primaries

- Pin Definitions
- Timing
- Levels
- Test Patterns

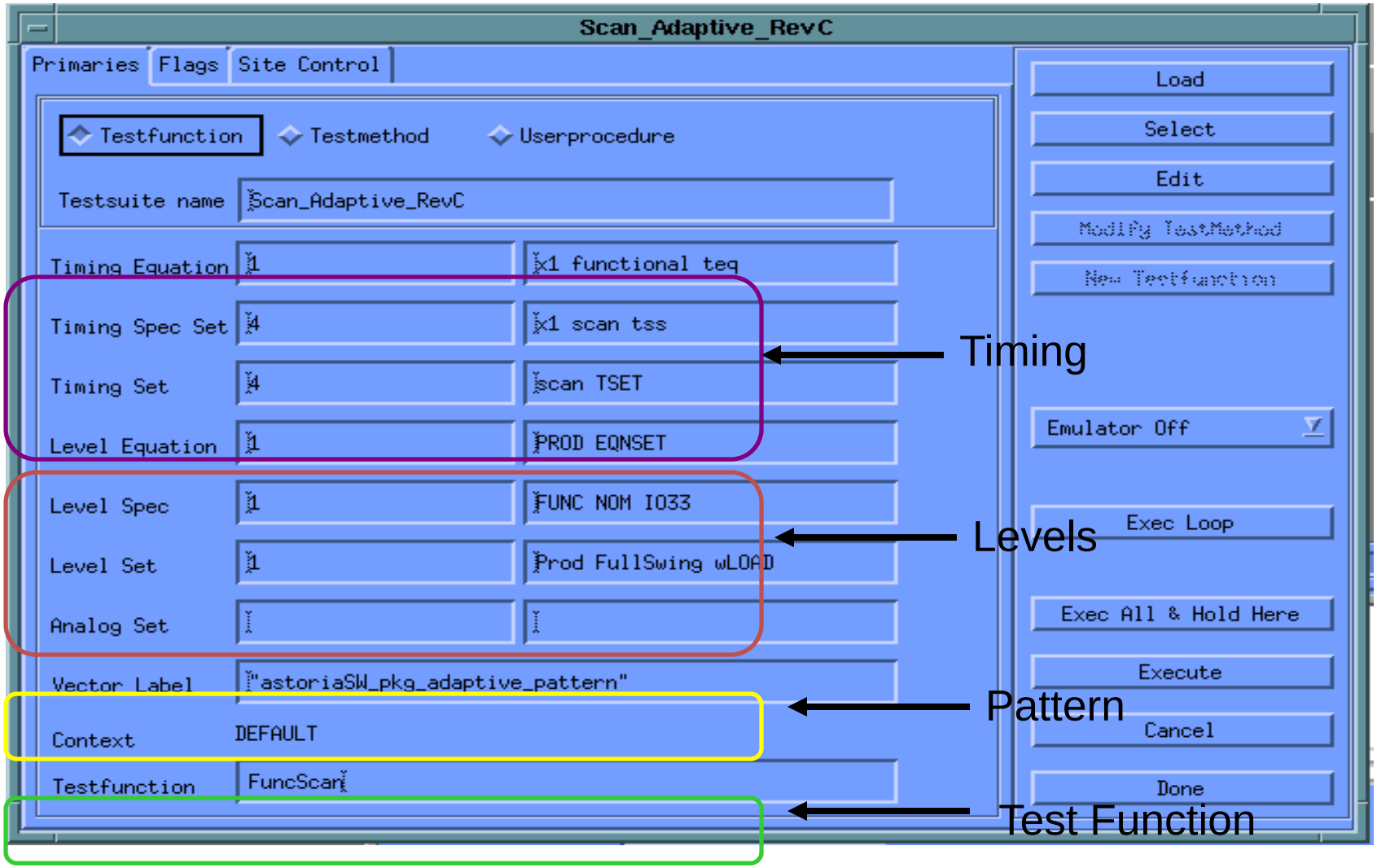
Test Suite

- Test Setup Definition : Basic building block that defines all the setup conditions for a test : Primaries

Test Flow

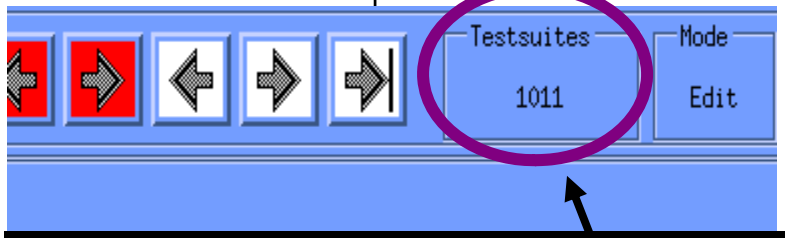
- Multiple test suites from Continuity to Binning combine to make a comprehensive Test Flow

Background : Test Suite

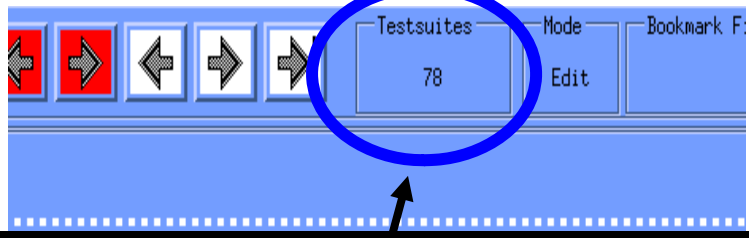


OLD METHOD VS. NEW METHOD : Complexity

Old Method : Device1



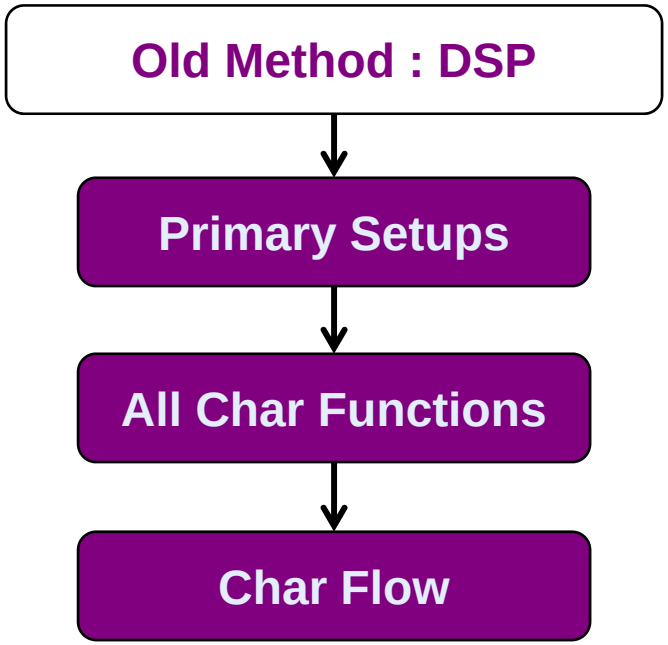
New Method : Device2

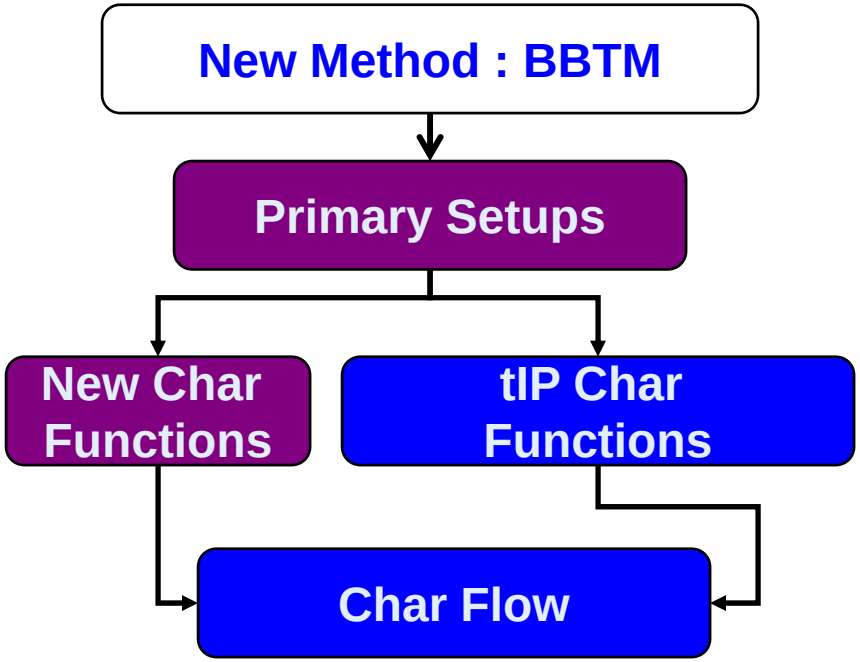


	Device1	Device2	Latest Version
File Size (Bytes)	6256459	56163	7596
Total Pages	2429	40	5
No. of Lines	69854	1814	263
No. of Words	164825	4633	655

	Device1	Device2
PARAMETERS	30	150
VDD COMBINATIONS	6	25
PATTERNS	50	200

OLD METHOD VS. NEW METHOD : Development Cycle





DEVICE-SPECIFIC TESTFLOW

- No reuse of code: flow, testfunctions
- Lack of standardization

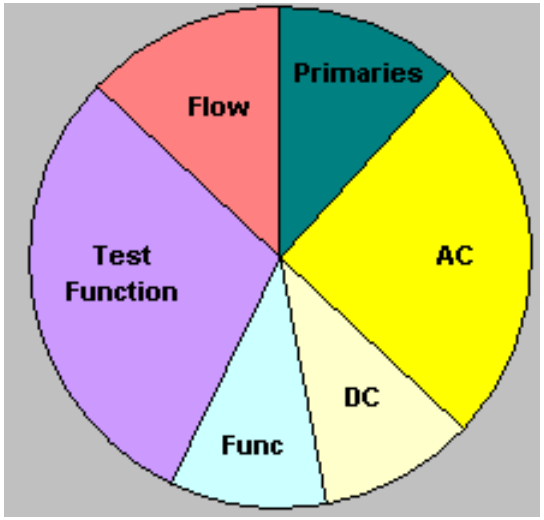
BBTM

- Modular testflow
- Standard char testfunctions
- Databrowser-friendly datalogs
- tIP sharing

Device Specific Program
Shared tIP

OLD METHOD VS. NEW METHOD : Flexibility

Old Method

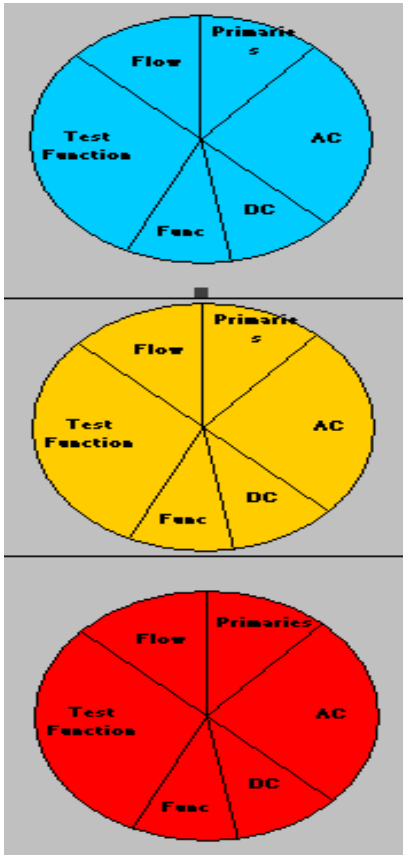


Development Cycle

Device1 : TE1

Device2 : TE2

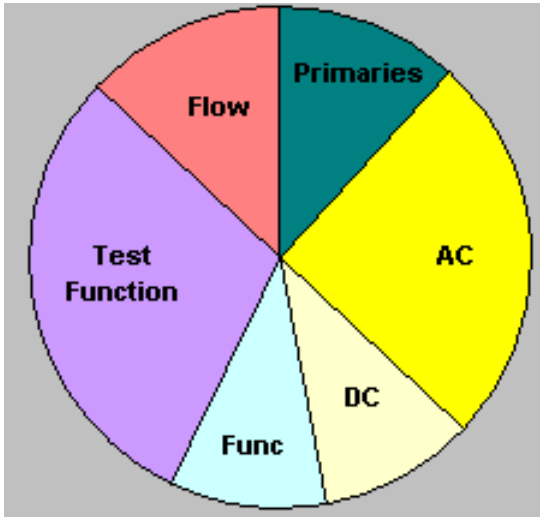
Device3 : TE3



TE1 | TE2 | TE3 | tIP (BBTM) | PE

OLD METHOD VS. NEW METHOD : Flexibility

New Method



Development Cycle

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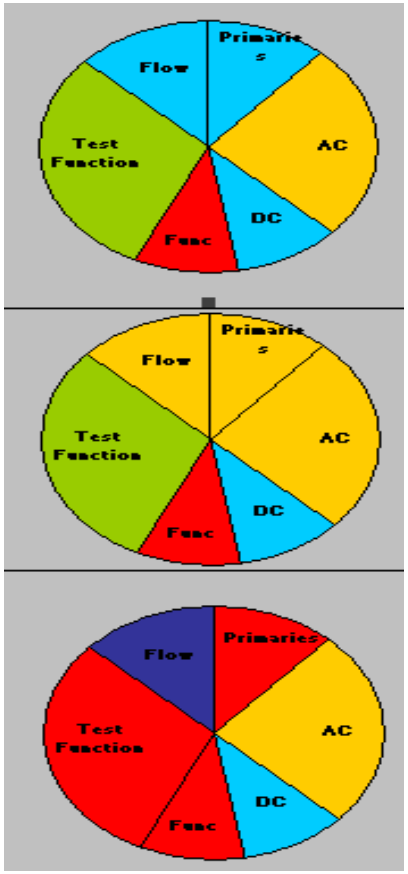
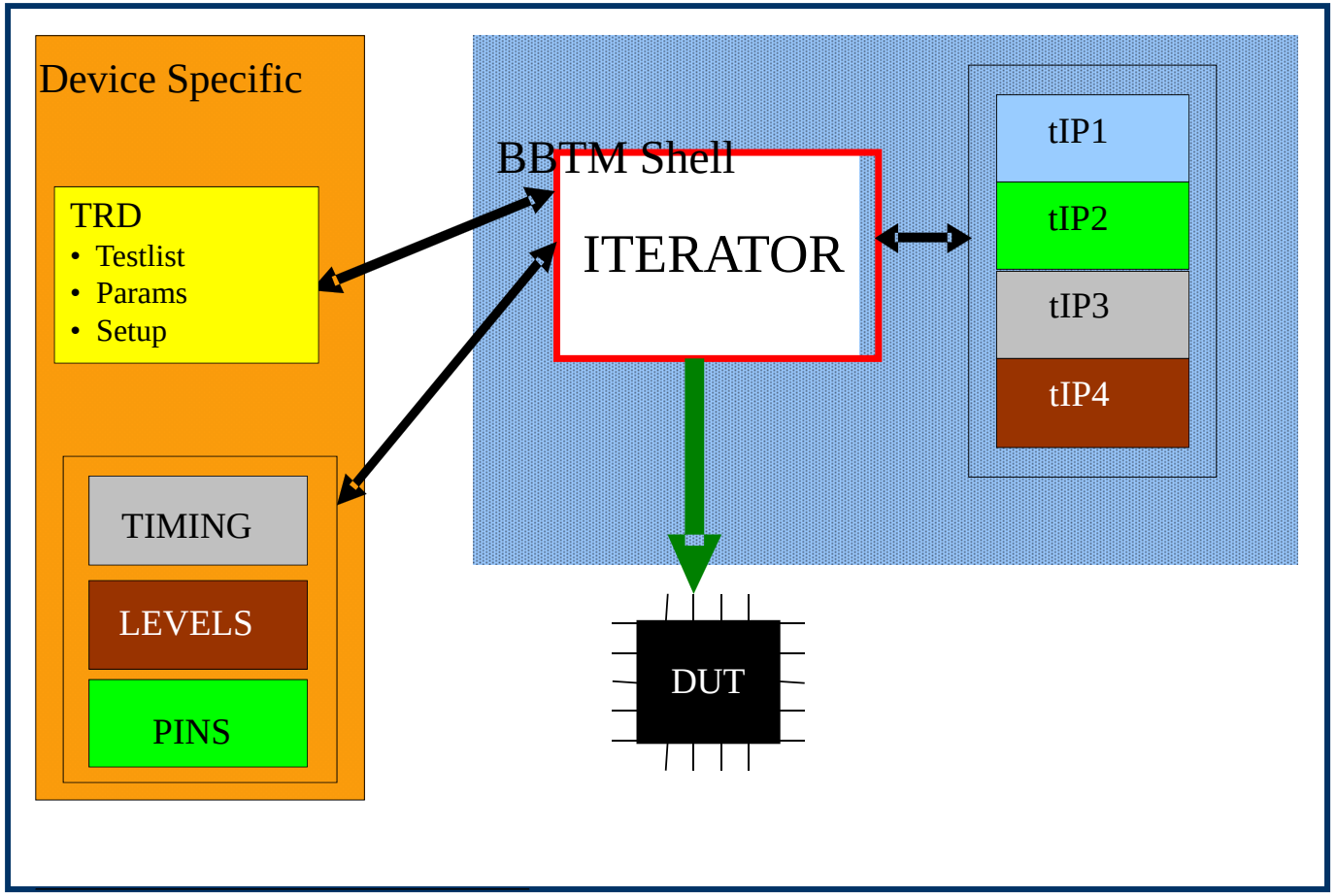


TE1 | TE2 | TE3 | tIP (BBTM) | PE

BBTM Implementation



TRD Components : Test List

- Flow Control
- Single line Test Suite Setups
- Multiple Insert Control
- High Level Documentation

current_index	pass_index	fail_index	long_name	hard_bin	soft_bin	pattern_name	param_list	ip_block	teq	tss	tset	leq	lss	lset	aset	looplssdis	fullchar	dido
1000	next	quit	continuity	10	1000	dont_care	continuity	continuity	1	1	1	1	2	1	1	0	1	1
1001	next	quit	vdd_short	10	1001	dont_care	vdd_short	standby_current	1	1	1	1	2	1	1	0	1	1
1002	next	quit	power_down_current	9	1002	power_down	lpd	standby_current	1	1	1	1	1	1	1	0	1	1
1003	next	quit	leakage	9	1003	power_down	leakage	leakage	1	1	1	1	1	1	1	0	1	1
1004	next	quit	andtree	9	1004	ANDTREE_vector	func_test	functional	2	1	1	2	1	1	1	0	1	1
1005	next	quit	ortree	9	1005	ORTREE_vector	func_test	functional	2	1	1	2	1	1	1	0	1	1
90001	next	quit	looplss_start	15	99	dont_care	func_test	looplss	31	1	1	2	1	1	1	0	1	1
90002	next	quit	spec_clktCO_sdhs	9	90002	u30_char_sport0_sd_hs_reg_52M_AAA	spec_clktCO_sdhs	echo_search	31	1	2	2	1	1	1	0	1	1
90004	next	quit	tSDIS_sdhs	9	90004	u30_char_sport0_sd_hs_reg_52M_AAA	tSDIS_sdhs	spec_search	31	1	4	2	1	1	1	0	1	1
90005	next	quit	tSDIH_sdhs	9	90005	u30_char_sport0_sd_hs_reg_52M_AAA	tSDIH_sdhs	spec_search	31	1	5	2	1	1	1	0	1	1
90006	next	quit	tSDOS_sdhs	9	90006	u30_char_sport0_sd_hs_reg_52M_AAA	tSDOS_sdhs	spec_search	31	1	6	2	1	1	1	0	1	1
90007	next	quit	tSDOH_sdhs	9	90007	u30_char_sport0_sd_hs_reg_52M_AAA	tSDOH_sdhs	spec_search	31	1	7	2	1	1	1	0	1	1
90525	next	quit	tSDCLKR_sdr50	9	90525	u30_char_sport1_mmc_hs_reg_52M_AAA_tSDCLKR	tSDCLKR_sdhs	rise_fall_time	31	6	12	2	1	1	1	0	1	1
90599	next	90502	looplss_end	15	999	dont_care	func_test	looplss	31	6	1	2	1	1	1	0	1	1
16005	next	quit	aca_adc_linearity_ramp	9	16005	u30_aca_x_Pall_Fall_pf1_read_1code	linearity	adc_linearity	81	1	1	2	1	1	1	0	1	1
16101	next	quit	bd_VDAT_LKG_DP	9	16101	u30_bd_x_Pall_Fall_pf1_cd_off	VDAT_LKG_DP	dvm	81	1	1	2	1	1	1	0	1	1
16201	next	quit	RPu_trim000	9	16201	u30_bd_x_Pall_Fall_pf1_rpu_000	RPu	resistance	81	1	1	2	1	1	1	0	1	1
21195	next	quit	PVT_enable_vnb_dac3_cp01	9	21195	u30_pvt_dac3_cp01_19_2M_AAA	vnb_enable_time	settling_time	91	1	1	2	1	1	1	0	1	1

TRD Components : Test Param

- Parameter Definitions
- Search Control
- Granularity Control (Pins, Resolution)

#param	spec_type	search_method	start	stop	reso	result_pin	ppOK	unit	source_pin	extra_params	$
continuity	TM::DC	TM::PPMU	120	1200	0	io	1	mV	uu	-100	$
vdd_short	TM::DC	TM::DPS	120	900	0	vpwr0_dps:vpwr13_dps:vpwr2_dps:vpwr_io1_dps	1	uA	uu	0	$
func_test	TM::FUNC	TM::Binary	0	293	0.01	allpins	1	P/F	pins	test	$
sdid_freq	TM::TIM	TM::Binary	cur-20	cur+20	0.1	@	1	kHz	uu	uu	$
sdop_freq	TM::TIM	TM::Binary	cur-2	cur+2	0.1	@	1	MHz	uu	uu	$
spec_clktCO_sdhs	TM::TIM	TM::Linear	0	cur	0.04	ac_sd_io_sXclk	1	nS	uu	uu	$
spec_clktOH_sdhs	TM::TIM	TM::Linear	cur	0	0.04	ac_sd_io_sXclk	1	nS	uu	uu	$
tSDIS_sdhs	TM::TIM	TM::Binary	cur-2	cur+2	0.01	ac_sd_io_s0D:ac_sd_io_s1D:ac_sd_io_s0cmd:ac_sd_io_s1cmd	1	nS	uu	uu	$
tSDIH_sdhs	TM::TIM	TM::Binary	cur-2	cur+2	0.01	ac_sd_io_s0D:ac_sd_io_s1D:ac_sd_io_s0cmd:ac_sd_io_s1cmd	1	nS	uu	uu	$
tSDOS_sdhs	TM::TIM	TM::Binary	cur-2	cur+2	0.01	ac_sd_io_s0D:ac_sd_io_s1D:ac_sd_io_s0cmd:ac_sd_io_s1cmd	1	nS	uu	uu	$
tSDOH_sdhs	TM::TIM	TM::Binary	cur-2	cur+2	0.01	ac_sd_io_s0D:ac_sd_io_s1D:ac_sd_io_s0cmd:ac_sd_io_s1cmd	1	nS	uu	uu	$
resistor_otg	TM::FUNC	TM::SPMU	0	3600	5	otg_id	1	mV	uu	clk_freq:1:15	$
RPu	TM::FUNC	TM::SPMU	150	300	50	otg_id	1	ohm	uu	uu	$
VDAT_LKG_DP	TM::FUNC	TM::PPMU	0	3.6	0.01	DP	1	mV	uu	uu	$
VDAT_LKG_DM	TM::FUNC	TM::PPMU	0	3.6	0.01	DM	1	mV	uu	uu	$
vnb_out	TM::FUNC	TM::PPMU	0	2.2	10	ac_pvt_op_vpb	1	mV	uu	0	$
vpb_out	TM::FUNC	TM::PPMU	0	2.2	10	ac_pvt_op_vnb	1	mV	uu	0	$
vnb_enable_time	TM::TIM	TM::Binary	120	900	0	ac_pvt_op_vpb	1	nS	vnb_out	vnb_out:95	$
vpb_enable_time	TM::TIM	TM::Binary	120	900	0	ac_pvt_op_vnb	1	nS	vpb_out	vpb_out:95	$

Test IP (tIP)

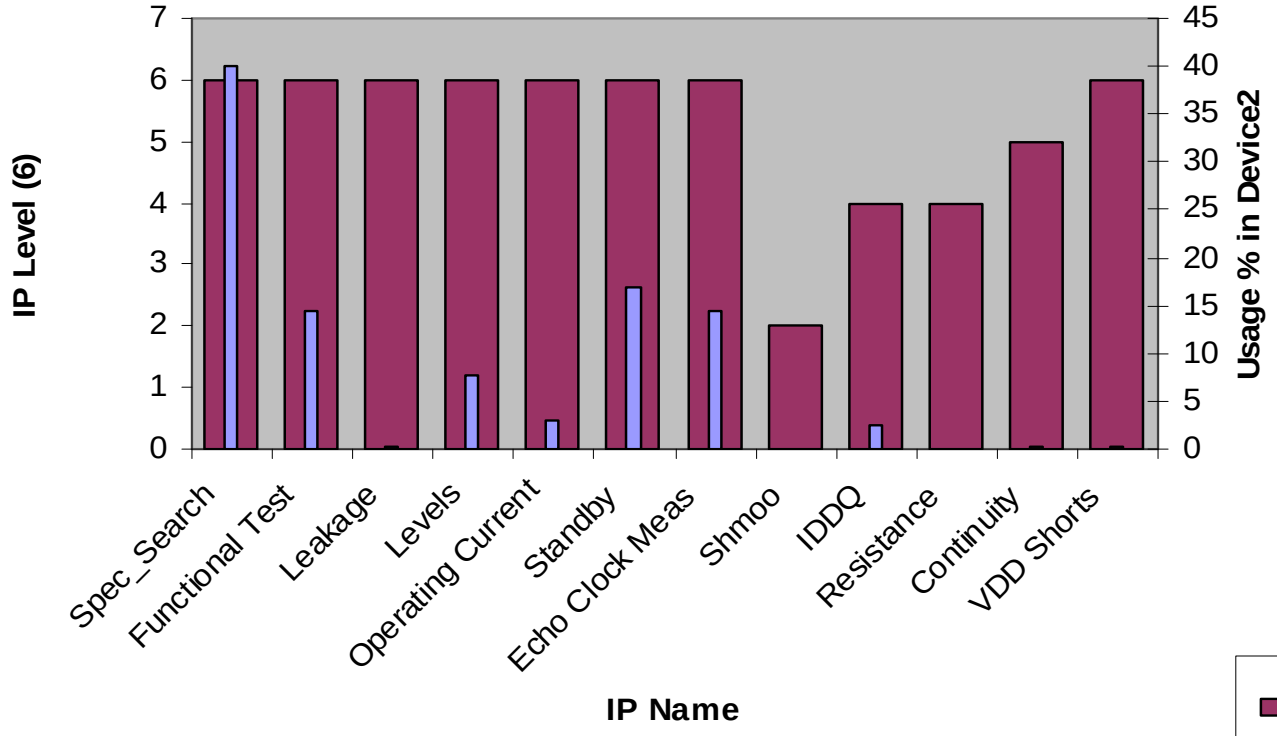
- Independent IP blocks
- Perform Standard Functions
- Standard Coding (Easy to Read)

DC	19
AC	9
Analog	8
Misc	9
Search	2
Functional	1
Total	48

tIP Level Definition

Number	Status	Definition	Deliverable
Level1	Identified	Identify a tIP that is required to test a Device or a Utility Function	None
Level2	Defined	Define the actual test procedure. This should include the definition of a generic test methodology (similar to bench setup) and 93k approach	Memo
Level3	Developed	Actual CPP Code developed and ready to be tested	None
Level4	Verified	Verify on a Real Silicon using the latest Iterator	Memo
Level5	Documented	Document using tIP doc template. Need to pass the review board.	tIP training module
Level6	Checked In	Check in tIP code, tIP documentation in Subversion	

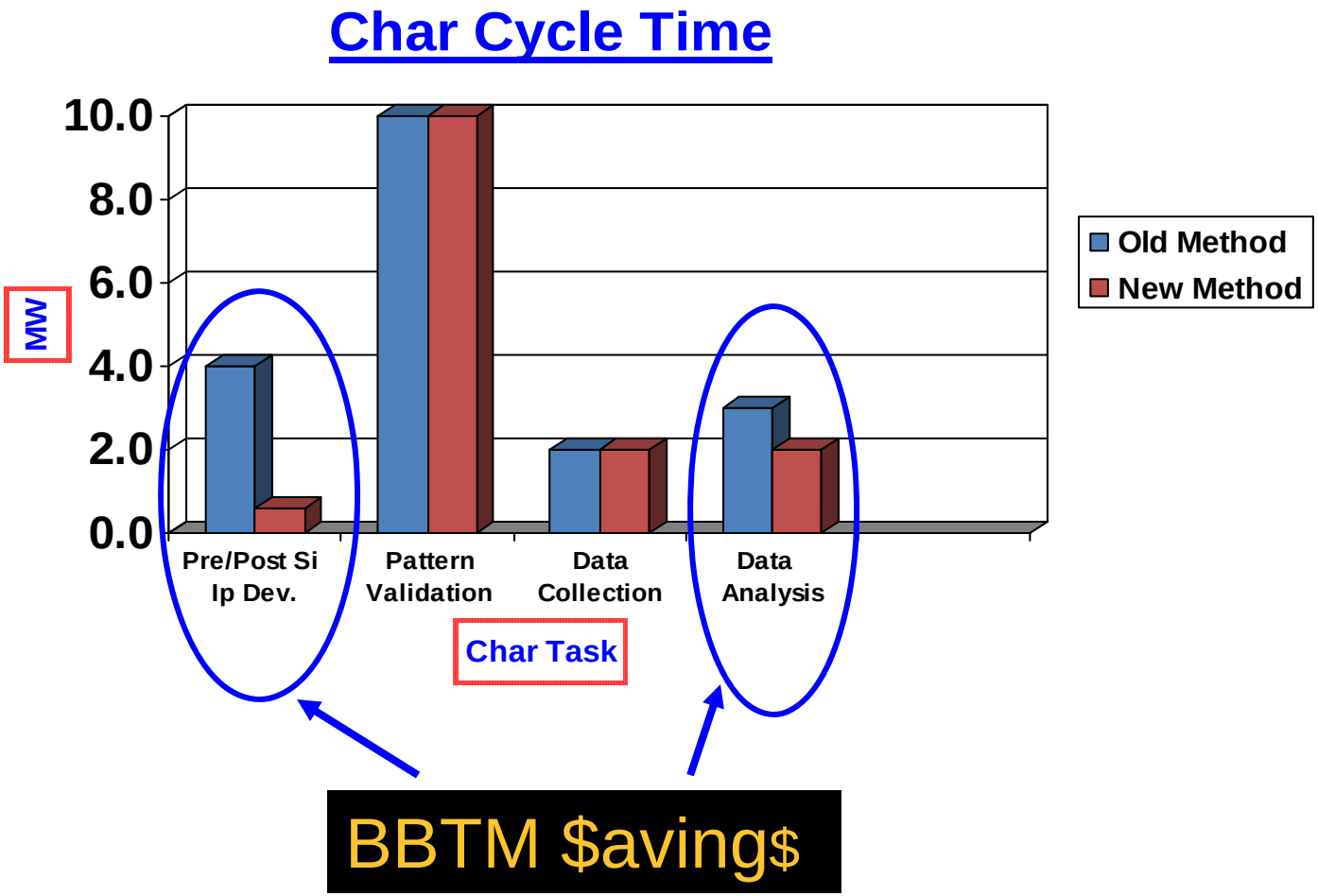
tIP Reuse Status



Level	IP Status
1	Identified
2	Defined
3	Developed
4	Verified
5	Documented
6	CheckedIn

- Total Tests : 325
- tIP Used : 12

ESTIMATED SAVINGS



ESTIMATED SAVINGS

Task	MW	COST ($K)
Old char development cycle time	6	24
BBTM development cycle time[1]	1	4
Savings per device	5	20
Total savings for 5 projects using BBTM	25	100

Note1 : Estimate for existing tIP. New tIP require more time.