Silicon Valley Test Workshop-2013

Program and Exhibitor Directory

www.svtest.com

Biltmore Hotel

Santa Clara, Ca

October 29, 2013

Thank you for attending our Workshop.

SV Test is known around the world for its robust technical dialog and discourse and the Technical Program is the focal point of our Workshops. Our Program includes outstanding presentations from IBM, Advantest, Agilent, Z-Tec, Cisco and other important groups who are meeting the diverse testing challenges in 3D SoC wafer probing, RF Cost of Test and many more challenges.

We are the only FREE workshop in the USA that targets the Silicon Valley Test Engineering community and we want to keep growing our attendance. This year we added the Silicon Valley PXI workshop to broaden our appeal to Test Engineers in the analog, mixed signal and RF world.

This year we have also added a Happy Hour at the end of the Technical Program. We want to encourage everyone to join us on the exhibit floor to talk to our vendors and view the demos.

Thanks to all who contributed to our workshops, attendees, authors, exhibitors, session chairs and especially our workshop Sponsors ***Advantest*** and ***Twin Solution***.

It is time to start thinking about submitting a paper or panel proposal for 2014.

Thank you and from all of us

Have a Happy Halloween!

Nick Langston Matthias Kamm Ira Feldman Anita Mastilock

Silicon Valley Test Workshop

Program

7:30 - 8:30AM Registration and Breakfast

8:30 - 8:45AM Chair Welcome and Agenda Review

8:45 - 9:45AM Keynote by Mark Roos

Mark is the founder and president of Roos Instruments. Roos Instruments develops RF ATE based on a modular architecture. He will present:

Adaptive Test and Big Data, the next step for Cost and Quality Improvement.

Seeking to drive down IC test costs, the industry is looking at new methods and standards for a promising technology called adaptive test. So what's adaptive test? For years, the IC industry used a simple formula on the IC test floor. It utilized conventional ATE and static test flows to determine whether a part passed or failed. In contrast, adaptive test makes use of software-based database and related technology, which can change the test flows and make decisions dynamically and on-the-fly based on manufacturing and statistical data

9:45 - 10:00 Break

10:00 - 10:45 Invited Presentation

Detecting Trojans, Counterfeits and IP Theft; Al Crouch,

Al Crouch, Chief Technologist – Core Instruments – ASSET InterTech. Senior Member of the IEEE. Formerly, chief scientist and director of R&D Inovys Corp. and Verigy Ltd. of Cupertino, Calif. He is the vice chairman of the IEEE P1687 IJTAG committee that is developing the IJTAG standard and has contributed significantly to the hardware architecture definition. Over the last 20 years, he's accumulated significant experience in chip design-for-test at both Freescale (formerly Motorola) and Texas Instruments. He has filed for more than 30 patents and been granted 15

Abstract: As the design and manufacturing process has continued to fracture and spread across multiple companies and continents, integrated circuits and systems have become increasingly susceptible to Trojan and counterfeit hardware and firmware. Numerous counterfeit parts have already entered the supply chain and may dangerously compromise government, military, medical, and communications systems. In addition, modern IC's today are made of many embedded IP Cores and may have functional configuration, test, debug, yield-analysis, and environmental monitoring instruments embedded within the silicon design that may aid in reverse-engineering of the IC or some of the IP Cores, so there is a need to hide the instruments and to obfuscate the instrument data (since it can be viewed at the pins of the IC). A security system is needed to both hide the embedded instruments and to hide material that can be used to verify the integrity and trust of the chip. This presentation will introduce Locking-SIB's and Trap-bits that utilizes the data flowing through the embedded instrument network as Keys to allow users to access hidden on-chip items such as instruments, codes, and possibly, trojan detection circuits. The security level of this method will also be evaluated in terms of "how long it would take an attacker to break."

10:45 - 11:15 **Strategies for Eliminating Counterfeit ICs**; Joe Holt. Joe Holt is currently Vice President, Business Development at Integra Technologies LLC and is one of the company founders. Joe has over 35 years experience in the semiconductor and related technology industries. In addition to his Integra experience, he has previously held senior management positions with Amkor Technology, Lucent Technologies, AT&T and NCR. Joe received a BSEE from the University of Florida in 1978.

Abstract: The worlds Counterfeit Integrated Circuit suppliers are getting more sophisticated and consequently detecting and eliminating them from the supply chain is becoming increasingly difficult. This paper will discuss the history of the counterfeit problem, the reasons it exists and the reasons that it will likely be with us for the foreseeable future. Real examples will be used to illustrate the growing sophistication of the counterfeiters and what detection methods are best used to catch them before they make it into end applications. The current legislative efforts to combat counterfeit ICs will also be discussed.

11:15 - 12:00P Cloud Based Testing Services; A. Sivaram, Advantest Corp.

Abstract :In the semiconductor industry millions of dollars are spent creating new components. These dollars represent retrospective costs that have already been incurred and cannot be recovered. Consequently, it is imperative that the new chip designs function in full and in perfect compliance to their specification, and be delivered to the market within tight consumer windows. Even a delay of a few weeks spent in re-spinning silicon can cost tens of millions of dollars. Post-silicon validation is therefore one of the most highly leveraged steps in successful design implementation. The best way to achieve high confidence is to leverage the pre-silicon verification work — which can comprise as much as 30% of the overall cost of the implementation — and use that knowledge in the post-silicon system. Today, much of this work is done on ATE and dedicated bench equipment, which partially explains the high costs associated with new silicon/system validation. However, a new tool introduced recently helps to reduce overall post-silicon validation costs.In this presentation we describe this new innovative service oriented test solution called Cloud Testing Service (CTS) whose main goal is to reduce debug and new silicon validation costs while providing leading edge test technology to satisfy the needs of design and verification engineers

12:00 - 1:30PM Lunch and Exhibits.

1:30PM – 2:00 **Strip Contactor: Design and Deployment Challenges; Jon Diller, Smiths Connectors, IDI**

Abstract : With the introduction of improved handler technology, the promise of greater throughput and lower cost of test that made strip test so attractive at the turn of the century has become much more practically realized. A growing customer base is implementing strip test for both analog and mixed-signal devices in Dual and Quad Flat No-Lead (DFN and QFN) applications.

The limited number of available handler platforms has allowed contactor manufacturers the luxury of a fairly fixed set of design constraints. This has permitted a significant amount of design standardization. The presentation will review an archetypical design for its features and limitations. The audience will gain an understanding of the rationale and benefits of this design. Mastery of alignment within the X, Y, and Z axes are the principal design challenge; the presentation will feature data from predesign analysis and post manufacturing quality assurance to validate these principles.

Manual test conversion of strip test contactors is a particularly challenging topic, and the presentation will discuss various available approaches in detail.

The presentation will conclude with the associated topic of film-frame testing of WLCSP devices, which is accomplished with the same handler technology and which presents many of the same challenges. This will broaden the usefulness of the presentation beyond high volume manufacturing to the rework and quality assurance disciplines.

2:00 - 2:30 A Fine Pitch MEMS Probe Card with Built in Active Device for 3D IC Test;

Florent Cros[1], Lakshmi Namburi[1], Ting Hu[1], Yong Hong[1], Robert Smith[1], Gary Maier[2], Luc Guerin[2], Van Thanh Truong[2], Katsuyuki Sakuma[2]
[1]Advantest America, Inc.
[2]International Business Machines

Abstract :Many challenges remain for the 3D Si (Silicon) Technology to make it viable and profitable. The entire 3D design verification, product qualification, and volume yield learning phase must be considered. In order to minimize costly 3D partial stack and final packaging yield losses, 3D die will have to pass stringent wafer, die, and KGS (Known Good Stack) testing. Due to limited 3D stack rework capability, some applications may also require a reasonable level of performance testing to guarantee the chip to chip interface before stacking. We attempt to solve all of the possible new test probe requirements for testing and measuring 3D wafers and individual die.

Our solution had several key goals. It must be capable of contacting both the external and internal chip to chip interconnects on current and next generation semiconductors manufactured at lithography scale on thin silicon and low-k dielectrics. The probing solution must also be capable of testing on smaller, thinner, and tighter pitch test contacts made of multiple pad and bump materials. There should be minimal disruption to product contact surfaces so as not to effect down stream processing during die and wafer scale stacking. The new probes must also be highly integrated and scalable for future technologies. Lastly, they must be processed in a low cost,

manufacturable, and serviceable solution for the HVM (High Volume Manufacturing) of 3D IC's.

In this paper, we discuss a probing solution capable of meeting the next generation product and technology test requirements. We present a compliant fine pitch MEMS (Micro electro-mechanical Systems) probe technology of up to 20,000 probes integrated onto an active 3D SiST (Silicon Space Transformer) with embedded test circuits. A ceramic substrate, silicon RDL layer, SiST, and MEMS probes were first manufactured in a wafer scale lithography process. We then show the probe assembly using an advanced 3D stacking and packaging method demonstrated in a series of die scale process steps. Finally, we show the mechanical and functional test results collected from a 3D eDRAM. The eDRAM was tested at wafer level with a mixed 150um and 50um pitch on multiple pad and bump materials across multiple temperatures.

2:30 - 3:00 **Trends, Challenges and Solutions in SoC Wafer Probing;** Mike Slessor, Jarek Kister, Ben Eldridge, Tin Nguyen, and Amy Leong FormFactor Inc, MicroProbe PBU, 617 River Oaks Parkway, San Jose CA 95134

With the once-relentless pace of front-end lithography-driven advances in semiconductor technology and economics now stalling, advanced packaging techniques are beginning to pick up the gauntlet and lead the next wave of "More than Moore" advances in our industry. This shift, manifest in novel assembly process flows like copper pillars and through-silicon vias, places a significant burden on assembly and test technology roadmaps; in this paper we focus on the direct impact on wafer probe and test.
Some trends are qualitatively similar to those the wafer probe community has successfully met for years: shrinking pitches and increased probe counts. On top of these familiar trends, however, there is also an emergence of challenging AC and DC electrical performance specifications for probe cards which demand a system-level approach to probe card design, validation, and test.Increasing probe counts are the result of two primary factors: increased parallelism (more DUTs per card); but perhaps more importantly, increased test coverage and electrical test performance for each of those DUTs, requiring more access points to accurately drive more test vectors through an increased number of diverse high-complexity circuits in the silicon.
At these sub-100um pitches, the Cobrastyle vertical technologies which are the workhorse of vertical probe at >130um face some significant cost and manufacturability challenges. These challenges are primarily inherent to the fundamental inaccuracies of the mechanical forming and drilling processes used in these technologies, and can be overcome with lithographically based MEMS processing technologies. These advances, when utilized to

fabricate sub-100um pitch full-grid-array cards with thousands of probes, result in robust and consistent manufacturing processes that provide inherently lower cost and higher performance than legacy technologies. Finally, although our collective historical focus has been biased towards the "probe" in "probe card", the increasing test coverage and reduced voltage/power margins of today's processors and SoCs have introduced a set of electrical signal integrity and power distribution performance requirements that were formerly the exclusive domain of final (package) test. As a result, many sophisticated tools and process technologies for the combined space transformer and printed circuit board are fast becoming requirements to successfully design and build a state of the art SoC probe card. A good indicator of this system-level complexity is evident in the board component counts, which are approaching, and even exceeding, the probe counts on a high-end card.
For both suppliers and users of production probe cards, meeting these challenges demands increasing supplier R&D investment to produce a set of robust production-worthy technologies with corresponding design, verification, and test tools/processes, all while continuing to meet the cost and leadtime trajectories demanded by the dynamic mobile-device market.

3:00 - 3:15 Refreshments, **Break and Exhibits**.

3:15 - 3:45 VRT – The Memory Test Escape that you can't Escape from. Craig Soldat, Cisco

Abstract : Variable Retention Time(VRT) is a behavior first documented in DRAMs in 1987. Though VRT is better understood today no strategies have come forward to eliminate the flaws in the silicon gate structures which cause the VRT behavior or reliably screen for the behavior in production. This presentation will introduce VRT and review it's repercussions. The presentation will share test considerations that rise from the desire to Escape from the Test Escape.

3:45 – 4:15 Configuration Dependent Test Socket Performance; Gert Hohenwater, Gatewave Northern, LLC

Abstract : While characterization of test sockets is typically performed for well controlled ground/signal pin arrangements, applications conform to such arrangements frequently only in cases of very high performance connections. Often applications require grouping of multiple signals near a few grounds, thus deviating from tested socket performance. Therefore the most accurate way to evaluate performance of a signal path in a given case is to simulate precisely this configuration.

This can, however, result in considerable expense of resources and potential delays of a design project. To aid in making the decision when to perform complete simulations vs. using existing data, simulation results for different configurations will be presented. These will show that frequency range and crosstalk requirements can become major drivers in the process. The impact of socket construction will also be illuminated. For example, two socket designs that both perform very well in 50 Ohm test environments may not do so in a general application in an equal manner. Beyond these differences test data, however, can lead the way to deciding which of the designs will be the proper choice and this will be demonstrated in this presentation

4:15 - 4:45 **PSoC Testing; A Case Study; Albert Alcorn, Cypress Semiconductor**. Albert is a Sr. Test Engineering Mgr and has more than 20 years of Test Engineering experience. Albert started his career at HP and was and instructor for the HP83000/F330 product. He is currently working on a high voltage LED lighting controller chip, a USB3.0 device and a wireless chip for keyboard applications, focusing on DFT/Test Modes and characterizing new silicon.

End of “Test“ Program

PXI Workshop Program

1:30 – 2:15 Advanced Characterization Techniques for RF Components, Chris Ziomek, President. ZTEC Instruments

Abstract : RF components such as power amplifiers (PA), front-end modules (FEM), and switches are integral to a system-level wireless design. The performance of an RF component can dominate the system-level performance, including key wireless device specifications such as wireless coverage area, data rate capacity, and battery life. For example, the transmitter PA or FEM must generate sufficient linear RF output power while using as little DC power as possible. In order to optimize the linearity and power usage of RF components, modern digital wireless devices use advanced digital signal processing techniques such as: (a) dynamic enable pulsing, (b) digital pre-distortion, and (c) envelope tracking. This signal-processing adds significant complexity to the selection and qualification of RF components for use in a wireless device. In order to truly know the operational characteristics for a RF component in circuit, the RF component performance must be characterized for

these signal processing techniques. This presentation describes test methods using PXIe compatible, FPGA based, modular instruments to characterize RF components for wireless device designs that use dynamic enable pulsing, digital pre-distortion, and envelope tracking

2:15 – 3:00 PA/FEM manufacturing Test – Maximizing Speed and Accuracy, Gennady Farber, RF Solutions Architect, Agilent Technologies.

Abstract : Testing Power Amplifiers (PA) and Front-End Modules (FEM) received new attention recently because of a number of market driven and technological reasons. On the market side explosive growth of handheld devices with variety of wireless connectivity features demanded from PA and FEM vendors increased volumes and therefore from test industry – improved throughput of test solutions. On the technology side development of new ways of optimization of PA performance with focus on efficiency and linearity, resulted in development of new test approached satisfying those needs. In our review we cover traditional PA characterization like Pout vs. Pin and ACPR from prospective of speed of test and stability or variance of test results. But mostly we go over new needs of the industry like Dynamic EVM and Envelope Tracking. Dynamic EVM describes performance of the PA / FEM when bias is provided ONLY when RF signal is present. ET is a way to optimize usage of power supply when signal envelope is changing over time. Both needs are addressed by appropriate test solutions that we are going to review and analyze from the same merit of speed and accuracy. We close our review by addressing PA / FEM characterization at the R&D stage, where Digital Pre-distortion, especially for wide bandwidth, is taking priority

3:00 - 3:15 Refreshment Break & Exhibits

3:15 - 3:45 Adopting the PXI Architecture for Semiconductor Test Applications, Mike Dewey, Marvin Test Solutions

Abstract : The PXI platform is a well-established standard and has been widely deployed for a range of functional test applications. More recently, PXI-centric, semiconductor test systems are now entering the market place. This paper will discuss some of the requirements and features that have been incorporated into PXI-based, semiconductor test systems.
Specific topics discussed will inlcude:

- System power requirements
- Instrument / UUT interface requirements
- Software requirements
- Digital subsystem requirements / capabilities

3:45 – 4:15 High Speed Data Streaming using PXIe Test Systems, Monica Lanctot, Adlink Technology

Abstract : High-speed data streaming applications requiring high accuracy and long sampling times include LIDAR testing, optical fiber testing, and radar and satellite signal acquisition. These applications present unique engineering challenges to meet demands for high throughput. This presentation will focus on specific requirements for optimizing the configuration of systems supporting high-bandwidth applications, by:

- Enabling high-speed real-time data streaming
- Designing applications optimizing system streaming performance
- Furnishing benchmarks that can be achieved in stream-to-disk and stream-to-memory applications

4:15 - 4:45PM Is PXI the Best Switching Platform for my Application, Paul Shanahan, Sr. Apps Engineer, Pickering Test

Abstract: There are many choices to make when designing a test station – the test platform is one of them. While PXI is an excellent choice for most applications, sometimes a hybrid solution is more accurate, reliable, and potentially even lower cost. This presentation will cover the advantages and limitations of choosing PXI as a switch platform. A variety of applications will be discussed and why PXI is or is not well suited for those applications. Other platforms will be mentioned for their advantages over PXI and when you might want to choose those instead of PXI

4:45 Concluding Remarks and Awards

Exhibitor Directory

1 TwinSolution Technology
Room 214, Building 20, No. 498, GuoShouJing Road Pudong New Area, Shanghai, PRC. 86-21-502-72817
www.TwinSolution.com
TwinSolution Technology is global supplier of Test Interface Solutions with headquarters in Shanghai. We are focused on supplying high performance Test Interface products, including ATE Test Sockets, Spring Probes, Thermal Control System and Connector products. We think locally and act globally with our worldwide sales and application network. Please contact us for your next test interface project.

2. Advantest America, Inc
3201 Scott Boulevard, Santa Clara, CA 95054 408-988-7700 www.advantest.com
Advantest has earned a worldwide reputation for blazing new trails in technology innovation. Having established, over its 50-year history, a track record of helping customers turn innovations into practical, market-ready products, in 2003, Advantest became the first ATE supplier to introduce a system-on-chip (SoC) tester platform based on the Open Semiconductor Test Architecture, or OPENSTAR®, specification. OPENSTAR is an open test architecture that that provides a modular, open platform for accommodating future applications and solutions. This extends the lifetime of the test system and significantly lowers the cost of ownership.

3. Adlink Technologies
5215 Hellyer Ave, San Jose, CA 408-360-4337
www.adlinktech.com

ADLINK Technology provides embedded computing solutions to the industrial automation, test & measurement, communications, medical, defense, and transportation industries. ADLINK products include data acquisition and I/O, vision and motion control, modules, boards, blades, chassis, and systems in a variety of standard form factors. ADLINK is a Sponsor Member of the PXI Systems Alliance.

4. Agilent Technologies

5301 Stevens Creek Blvd, Santa Clara, CA 95051 www.agilent.com
Agilent Technologies is the world's premier measurement company. Our singular focus on measurement helps scientists and engineers address their toughest challenges with precision and confidence. Agilent provides solutions to a variety of industries through a large number of product families. These include network analyzers, spectrum or signal analyzers, general-purpose electronic instruments, one-box testers, radio frequency and microwave signal generators, oscilloscopes, electronic design automation software, and in-circuit/parametric testers.

5. Aehr Test

400 Kato Terrace, Fremont, CA 510-623-9400 www.aehr.com
Aehr Test Systems is a worldwide provider of systems for burn-in and testing DRAMs, flash and other memory and logic integrated circuits and has an installed base of more than 2,500 systems worldwide. The FOX system is a full wafer contact test and burn-in system. The DiePak carrier is a reusable, temporary package that enables IC manufacturers to perform cost-effective final test and burn-in of bare die.

6. Ardent Concepts

130 Ledge Road, Seabrook, NH 03874 603-474-1760
www.ardentconcepts.com
Ardent designs high performance signal integrity connectors with patented technologies, including the smallest, fastest, all metal compression mount connector technology on the planet. Ardent connectors enable our customers, the world's leading integrated circuit manufacturers and systems integrators, to bring the fastest supercomputers, servers and next generation electronics to market.

7. Chroma ATE

7 Chrysler Rd, Irvine, CA 92618 949-421-0355 www.chromaus.com
Founded in 1984, Chroma is a global leading manufacturer specializing in integrated and fully automated turnkey electronic test & measurement solutions for the semiconductor, automotive, military, government, and the emerging green industries. Leveraging this in-house expertise in offering ATE, MES, and other T&M solutions, Chroma now also has a significant foot print in the PXI sector, with 6 and growing models of "Source Measure Units", number of other "Power Supply" options, as well as having one of the more advanced Pin Electronics Modules for PXI. We also offer various size Chassis, other functional cards, as well as various software drivers to complete a fully configured PXI system.

8. CMR Summit Technologies

473 Sapena Ct. Santa Clara, CA 408-844-9550
www.cmrsummit.com
Computer aided engineering design and manufacturing of specialty circuit boards specializes in providing its Customers the Ideas, Products and Services they need to sustain a valuable competitive advantage

9. Dynamic Test Solutions(DTS)/MC Test Products

21 Science Park Road #03-28 Singapore www.dynamic-test.com
+65-68734610
DTS has recently merged with MC Test Products of San Jose and offers custom designed PCB's for all ATE applications, including loadboards, DUT boards, PIB, DIB, HIB and Probe Card circuit boards. Specializing in complete turn-key test hardware, DTS drives the test hardware schedules and integration to provide a single point of contact. All major tester and handler platforms are supported

10. Evans Analytical Group (EAG)

2710 Walsh Ave, Santa Clara, CA 95051 **www.eag.com**
Evans Analytical Group's Microelectronics Test and Engineering (MTE) team provides comprehensive services and support from first silicon debug to high volume production. Our services include: ATE test hardware and software development, production testing, tester rental, Burn-in and Reliability qualification, ESD & latch-up, PCB design, FIB circuit edit/debug, and Failure Analysis.

11. E-Tech Solutions
Bud Kundich, PO Box 4078, Mt. View, CA **info-us@e-tec.com**
www.e-tec.com
E-tec Interconnect specializes in the design and manufacture of high quality elastomer and probe-pin test sockets. We support virtually any package footprint and mounting requirement with a variety of closure options. Engineered and manufactured by Swiss craftsmen; they are economically priced and can be shipped in as little as 10 days.

12. Feinmetall
2151 O'Toole Ave, Ste 10, San Jose, CA 95131 408-432-7500
www.feinmetall.com
Good contacts are important due to demand in the interpersonal communication and technical fields. FEINMETALL is a leading provider of contact solutions, particularly for testing electrical and electronic components. Our product portfolio includes test probes, test fixtures and probe cards with the finest structures for semiconductor test. In addition to our standard program, we also develop customized solutions for our customers' specific requirements.

13. Finley Design Services
910 Bern Ct. #130 San Jose, CA 95131 408-437-4080
www.finleydesign.com
Finley Design Services, Inc. located in Silicon Valley is a leading designer and supplier of quality Load Boards, Probe Cards, and D.U.T. Boards for the I.C. Test Industry. We provide superior engineering, layout, fabrication, and assembly of Load Boards specializing in high performance solutions. Let us optimize your test performance!

14. Interconnect Devices Inc.
5101 Richland Ave, Kansas City, KS 66106 913-342-5544
www.idinet.com
IDI is the originator of the spring contact probe test socket and continues to be the leader of innovations in the semiconductor test industry with our Antares and Synergetix brand test sockets

15. Marvin Test Solutions, Inc
1770 Kettering Ave, Irvine, CA 92614 949-263-2222
www.marvintest.com
Marvin Test Systems, Inc. is a global producer of PXI and PC-Based test equipment, software and automated test solutions for electronics manufacturers including the semiconductor industry. Marvin Test's products and services include PXI chassis and instruments, test executive and development software (ATEasy), integration services and semiconductor test systems.

16. MJC Electronics Products
Austin, Tx 408-264-8880 www.mctest.com
Our services include printed circuit board design, simulation, a full mechanical engineering department, in house assembly including repair as well as consulting services. 3150 Almaden Expressway #250

17. Pickering Test Interfaces
67 So Bedford Rd, Suite 400, Burlington, MA 01803
www.pickeringtest.com
Pickering Interfaces offers signal switching and conditioning for a broad range of applications and architectures; our portfolio contains the largest range of switching cards in the industry. Pickering's products are specified in PXI, commercial and military test systems throughout the world with a reputation for providing excellent reliability and value.

18. . R&D Circuits
3601 So. Clinton Ave, So Plainfield, NJ 07080 732-549-4554
www.rdcircuits.com
In business since 1969, R&D Circuits has been manufacturing the most cutting edge technology in the printed circuit board and engineering community *for over 30 years*. As a world-class PCB Manufacturer and Electronic Assembler we offer advanced technology printed circuit board fabrication and circuit assemblies. Our leading edge equipment, on-demand engineering support, personalized service and outstanding quality make us an ideal choice for your prototype PCB supplier.

19. Rika Denshi USA, Solution Technology Center
46750 Fremont Blvd, Ste 110, Fremont, CA 94538 510-445-1136
www.testprobe.com
Rika Denshi America has been a leader in Test Probe (Spring Probe) development, design and manufacture for 50 years. RDA has extensive experience and provides Test Sockets, Standard Probes, Custom Probes, and Test Interfaces. RDA's Solution Technology Center (STC) in Fremont designs sockets, spring probes and provides technical support.

20. Spire Manufacturing Inc
62 Bonaventura Dr, San Jose, CA 95134 408-456-0234
www.spiremfg.com
Spire Manufacturing offers test sockets with the highest electrical and mechanical performance on the market, ensuring global semiconductor manufactures and test houses the most stable and reliable contactors that deliver the most accurate tests for a wide range of applications

21. Test Spectrum Inc
9701 Brodie Lane Ste 101, Austin, Tx 78748 512-472-6750
www.testspectrum.com
Test Spectrum is a recognized leader in semiconductor test solutions. We deliver the best possible test development solutions, whether you need to outsource an entire project or simply augment your team. We specialize in Test Hardware, Test Software and Soft Tools for Pattern Generation, Pattern Conversion and Data Analysis.

22. Titan Semiconductor Tool, LLC
17 Bramford St, Ladera Ranch, CA 92694 949-429-5423
www.titansemitool.comTitan Semiconductor Tool provides the Semiconductor Assembly and Test Industry with sockets, fixtures and mechanical spares to Original Equipment Manufacturers (OEM) and End-Users. We can custom engineer and/or manufacture your solution to meet your bench and ATE needs. Titan specializes in providing three dimensional modeling and visualization to our customers.

23. ZTEC Instruments

Tiburon St. NE, Albuquerque, NM 87109 T: 505-715-0245 7715
www.ztecinstruments.com
ZTEC Instruments is a New Mexico-based corporation that designs and develops leading-edge modular wireless test equipment, oscilloscopes, and waveform generators. ZTEC's modular instrument products offer functionality that is optimized for markets such as wireless communication and defense/aerospace test, and are available in PXI/PXIe, LXI, VXI, and PCI modular form factors.

24. Oak-Mitsui Technologies

80 First St. Hoosick Falls, NY 12090 408-483-5413
www.faradflex.com
FaradFlex is an ultra-thin embedded capacitance material fit for ATE and evaluation boards which provides ultra low impedance for the best high speed power delivery, minimum noise, and optimum PDN. By using FaradFlex you can eliminate decoupling capacitors, reduce layer count, and reduce board thickness.

25. Robson Technology Inc

Morgan Hill, CA 408-779-8008 www.testfixtures.com

Established in 1989, Robson Technologies, Inc. (RTI) is a solutions based provider of customizable hardware interfaces that bridge the gap between your device under test and your test/measurement system. RTI offers a variety of high performance interconnect technologies such as Pogo Pins and Low Profile Elastomers in their test sockets, test fixtures, and test system interfaces. Located 20 minutes south of silicon valley, RTI designs and produces product in house for semiconductor and electronic development companies world wide. Discuss your upcoming test project with RTI's team