“25GBps Socket and Loadboard Test Issues”

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Abstract

This paper discusses testing for 25GB/s multi-lane devices based on performance, measurement repeatability, ease-of-implementation (reproducibility), and cost. A modified form of loopback testing will be used to study the impact of socket and loadboard concerns.

Introduction

Advances in semiconductor technology will soon allow consumer-oriented (that is, low cost and high volume) multi-lane serial communication devices in excess of 20GB/s. High volume production electrical test at these speeds create some interface challenges not yet encountered within the ATE test industry. For example, via-to-trace right angle interfaces may resonate within the much higher required bandwidth [1]. Such resonant points have not been a concern for lower data rate devices.

This paper identifies some of these new challenges and then identifies the potential impact on a form of external loopback testing.

Device Assumptions

For discussion purposes, the authors make the following assumptions about a 25GB/s electrical interface:

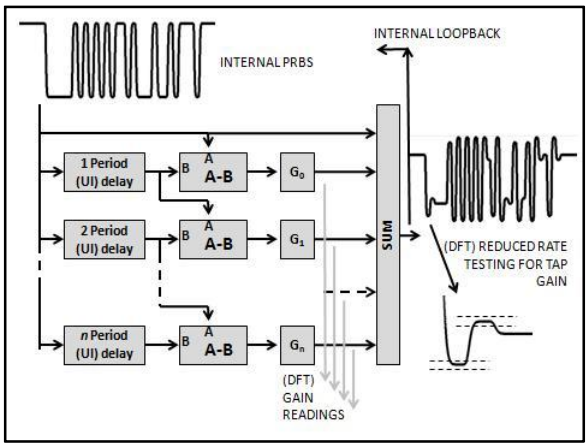

Figure 1: 25 GB/s Device Assumptions

1. The device will support an emerging configurations of four transmit (Tx) and four receive (Rx) differential lanes (16 total high speed signals.)
2. The device will connect to an optical interface within 12ò through one connector. Therefore any Tx to Rx correction scheme must correct 24ò of electrical loss, two interconnects, the optical transceivers, and optical cable.
3. The device may or may not support more than one optical port, and each port requires 16 total high speed lanes.
4. The device will use a FIR tap-style and/or DFE form of pre-emphasis and equalization that conform to a standard [2].
5. The device will support a variety of useful BIST and DFT features. These include internal loopback, an internal PRBS source, and the ability to read training settings, such as tap gain coefficients [2].

Assuming that structural, device defect, tap gain, and internal loopback tests pass, the main concern for testing is the ability of the device to correct for the highest specified losses ï or a range of losses -- at its rated operating speed.

Today loadboard and socket technologies exist that allow 25GBps testing. Therefore, reproducibility of test results from test to test, site to site and loadboard to loadboard becomes the concern of the test engineer.

Generic Concerns @ 25Gb/s

Relative to lower speed lanes, five critical areas of concern develop for 25Gb/s serial lanes. For the corrective methods discussed above, the transmission loss should be as monotonic as possible over the bandwidth of the signal. The bandwidth relates directly to the rise (fall) time of the signal (t_r), and the authors use $1.05/t_r$ [3]. (This is somewhat more accurate than use of the 5th harmonic [3].) An 18ps t_r therefore translates to a 58GHz bandwidth.

The first of these is the package pitch and pin-out. Current PCIE devices operating at 6.5GB/s, for example, operate cleanly in a 1 mm package. However, the spacing of a 1 mm package limits itself to 20-25 GHzï less than ½ of the required bandwidth. Above these frequencies, the spacing between pins is larger than ə/4 (quarter wavelength), and the wave no longer propagates in a single mode fashion. A large diameter cable demonstrates a similar effect [1]. For this reason, the most suitable pitch for 25GB/s devices is 0.4mm and below. Further, the differential signal must be surrounded by ground to maintain impedance and to isolate the differential pair from adjacent (aggressor) pairs. Figure #2 shows appropriate pitch patterns.

Pitch, of course, is a much bigger issue than just test. However, test aggravates crosstalk (e.g. bounded uncorrelated jitter) and loss by typically requiring thicker test boards and a test socket. A completely ground-surrounded differential pair as shown in Figure #2 results in much lower crosstalk. (See Figure #3.)

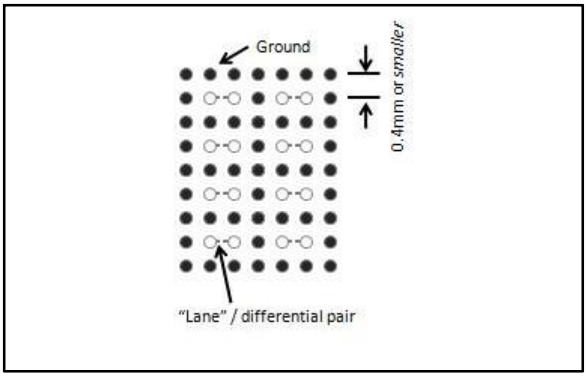

Figure 2: Most Desirable Pin and Pitch Configuration

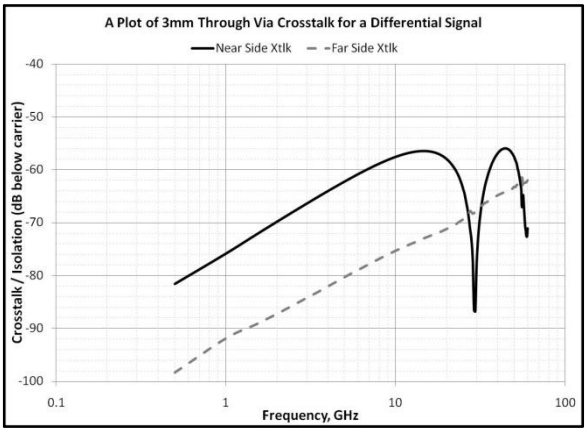

Figure 3: Through Via Crosstalk with Desirable Configuration

The second generic concern relates to the transition of the via to the trace. In nearly all cases, this requires a right angle bend and associated drill pad for transitioning the via to the trace. Further, nearly all vias, except for through vias and shallow laser-drilled vias, result in a small stub extending beyond the drill pad. At lower frequencies, back-drilling adequately reduced this stub. However, for 25GB/s signals, even a 5 mil stub will be noticed. This right angle and associated stub tend to create a resonating structure. Figure #4 shows such an example back-drilled via structure. Figure #9 shows the accumulated losses of the vias and traces in a data path.

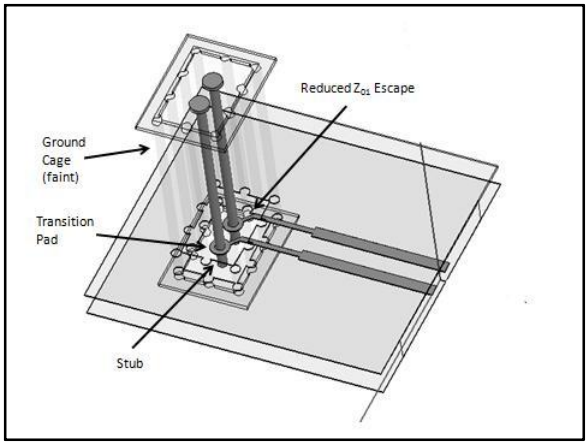

Figure 4: 3D Model of A Common Differential Via and Trace Pair

The third concern for 25GB/s transmission again relates to propagation modes fore-mentioned in the device pitch discussion. Many test engineers tend to use very wide traces for lanes on load-boards. Wide lines drive taller heights between ground planes, which limit the TEM mode propagation. For common high speed materials, any ñwideò line should not exceed 0.4mm in width. The author notes, however, that losses tend to track dielectric loss more than skin effect loss at higher frequencies. For example, a 150% increase in line width may only result in a 10% improvement in loss @ 60GHz.

The fourth concern is printed circuit board tolerances. For lower data rate applicationsð but not RF applications [5]-- losses and variations are not as major of a concern. However, as the data rate increases, so do the negative effects of variations within the loadboard. The critical loadboard tolerance issues are [6]:

(1) Etch Tolerance
(2) Average Material Thickness Tolerance
(3) Within-sheet Thickness Variation
(4) Material Weave and Dielectric Variation
(5) Metal Plate Variation
(6) Regional Variation Within a Board
(7) Copper roughness
(8) Use of Nickel

Printed circuit board tolerances result in loss variations with a board from lane to lane and from test site to test site (+/- 3 ohms) and, more significantly, higher variations from board to board (+ / - 6 ohms) [6]. That trace must be narrower to support 25GB/s bandwidths increases the overall error tolerance.

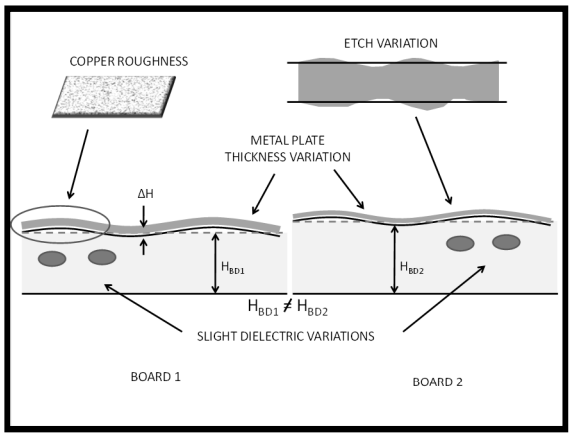

Figure 5: Non-ideal Loss Contributions [6]

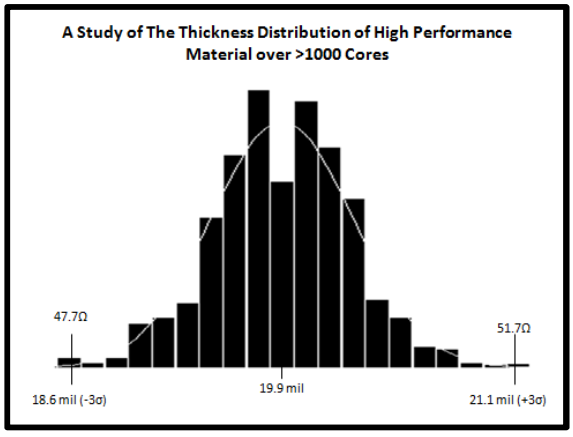

Figure 6: Material Thickness Distribution

Figure #6 shows core thickness variation for approximately 1200 cores of a common high performance material. This data, however, is for a 20 mil core, which corresponds to ~21.7 mil trace. Such a wide line is relatively insensitive to etch concerns and even micro-reflections discussed below. However, it cannot be used for 25GBps transmission. The dielectric height exceeds ∂/4 @ 39GHz. This results in a change

in propagation mode within the bandwidth of interest.

A growing tolerance concern can best be described as ñmicro-reflectionsò, as shown in Figure #7. The authorsô concern is that the variation from lane to lane, site to site, and board to board results in test repeatability issues when a device trains. In the worst-case scenario, the test pc board repeatability issues will result in failures for high loss tests.

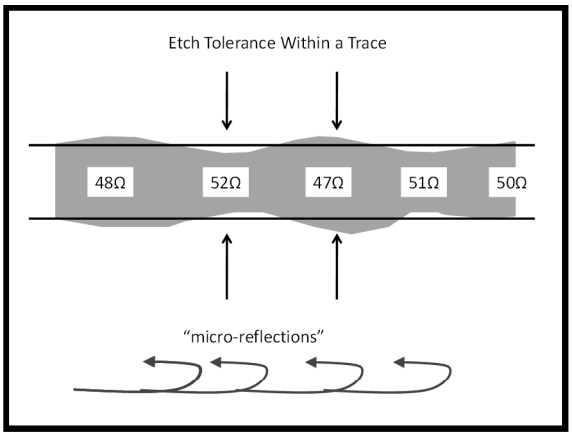

Figure 7: Micro-reflection Concept [6]

Figures #8 and #9 show reasonably monotonic losses for a device escape, 3ò differential stripline trace, and interface via using the perturbation correction method described above.

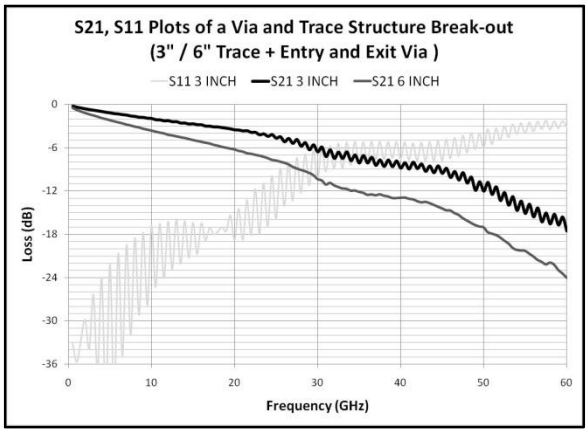

Figure 8: Typical Loss for a 25GB/s test Structure

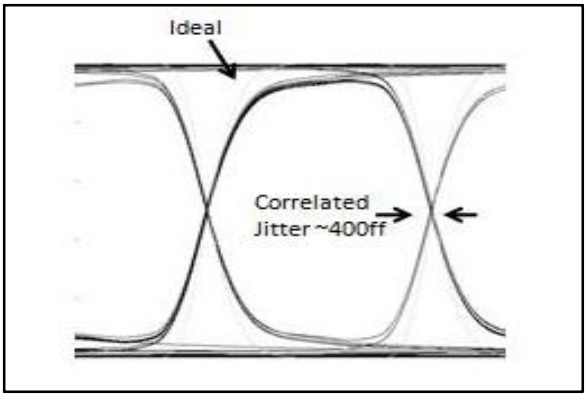

Figure 9: Data Eye of the Loadboard Structure (3" trace)

Unfortunately, a single lane on a single board does not allow one to evaluate lane to lane, site to site and board to board deviations. Figure #10 shows the data eye effects of the best/worst loss variation over four different pc boards (6ò trace + 2 vias).

Such loss variation will directly result in deviations in the data eye from test setup to test setup. Correction, training, and tap settings will consequently vary, as well.

The final critical concern is the socket. At the writing of this paper, commercially available spring probe / mechanical sockets did not yet have the required bandwidth and band flatness desired. However, elastomeric sockets do, and usually add less than 0.5db of loss at 40GHz. In From figure 11, the loss of the spring contact probe socket adds ~ 1ps of correlated jitter.

In summary, the five critical concerns of pitch, via to stripline transition, narrower line widths, pc board process tolerances, and sockets can be reasonably managed to enable a successful 25GB/s test environment. Only test site to test site repeatability remains a concern and potential yield issue.

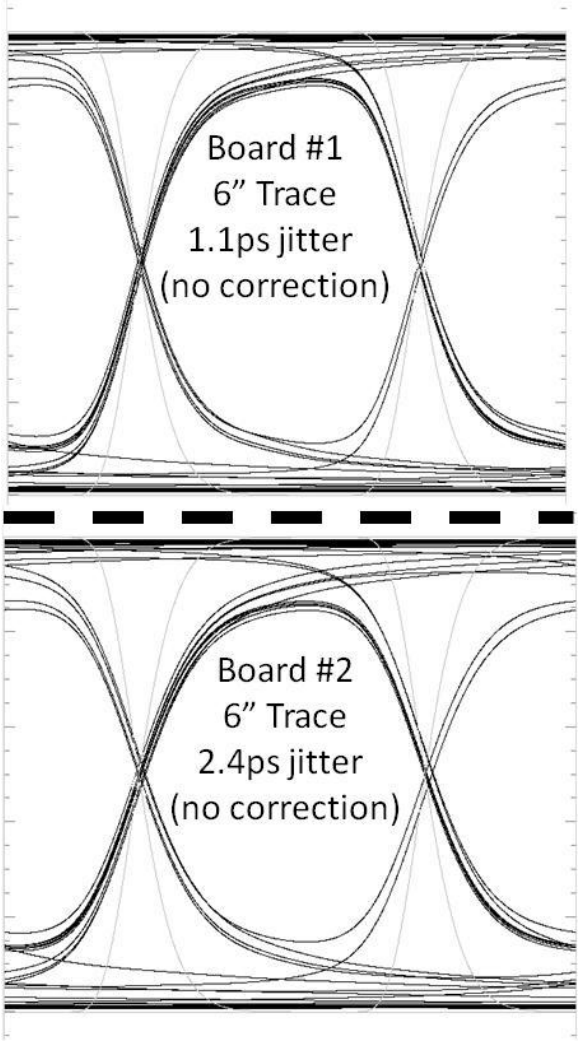

Figure 10: Loss Variation Affect on the Data Eye

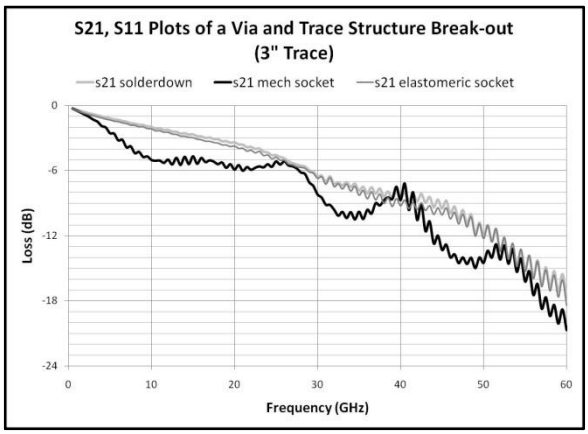

Figure 11: Loss Compared to Loss with 2 Socket Styles

Application of Errors to the Assumed Test Strategy: High Fidelity External Loopback

Figure #12 shows the assumed test strategy for this paper. The approach relies on developing a highly reproducible interconnect from the device under test to an interface for a daughter card. Allowing a high density, high fidelity daughter card interface for loads adds two benefits. First lossy loads or optical loads may be changed without re-spinning the loadboard. Second, instrumentation may also be connected to the device, when required. Therefore such an interface promises to be the very flexible.

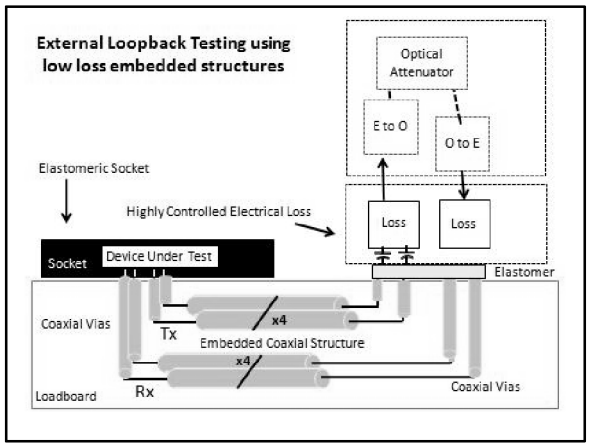

Figure 12: High Fidelity Loop-Back Testing

However, all of the issues remain for creating the highly reproducible loadboard. Now, in fact, an additional connector interface exists. Based on standard technologies, this approach will have the following differences from board to board:

1. Dielectric Thickness Variation, bd to bd.
2. Dielectric Thickness Variation, within a board (e.g. trace to trace)
3. Etch Variation

Emerging Solutions

Specific processes in the pc board industry do have highly reproducible properties. The first of

these is an embedded coaxial via or twin-axial via. (Vertical coax: See Figures 13 and 14.) The coaxial via depends primarily on mechanical drills for tolerances.

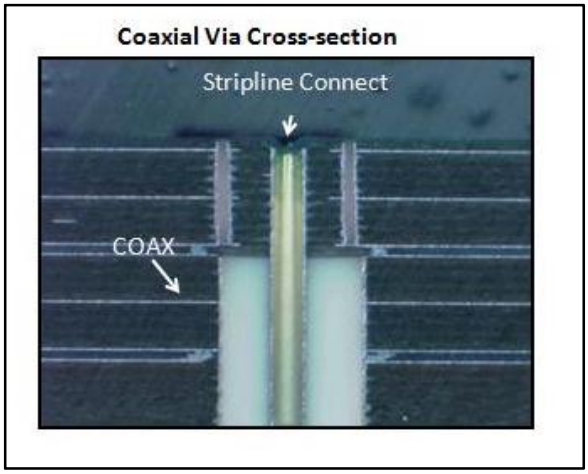

Figure 13: Cross-section of an Embedded Coaxial Via

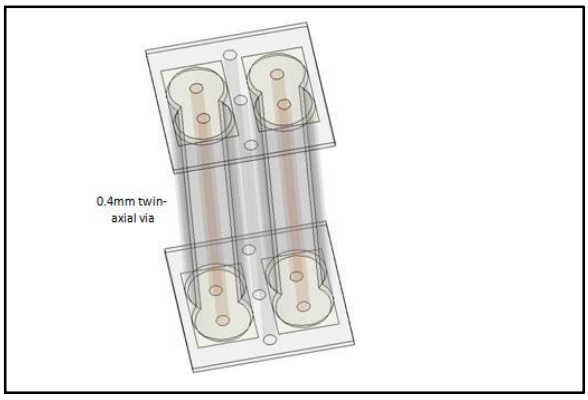

Figure 14: 3D Model of a Twin-axial Via

The second process is the ability to embed low-loss structures in the pc board. (air-core stripline: See Figures #17 and #18.) Two such processes exist. Air-core structures rely on mechanical routing. This reduces thickness variation issues within materials [3]. Because the lines are naturally wider, etch tolerances also reduce.

A critical cost benefit of the air-core line is that it does not require exotic materials to process. Therefore, materials known to work well for fine pitch may still be used. That stated, this approach still needs matured.

The remaining challenge is the right angle bend from the vertical to horizontal coax. The bend can easily create a resonant point. *The authors cannot over-emphasize how problematic the via transition can be.* Research for this paper shows that when the stub and pad can be modeled as a capacitive parasitic, it can be corrected by reducing the line width of the trace leaving the via pad for a short distance. Figure #15 uses TDR and thus shows how the effective discontinuity can be mitigated.

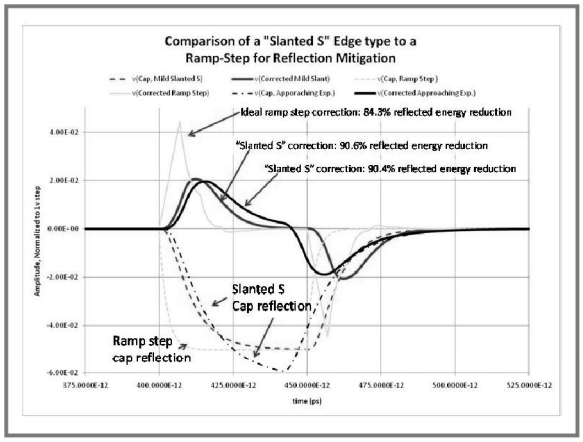

Figure 15: Mitigation of Via Pad, Stub and Bend Issues

The exact length of the corrective stub depends on the effective characteristic impedance of the narrowed section, the propagation delay of the section, the rise time of the signal, and the shape of the signal, as depicted in Figure #16.

The following equation represents both a derivation of the perturbation cancellation and a curve fit to a variety of different wave shapes:

$$T_{PD} = 0.87 \times \frac{T_C}{[2 \times (\rho + \rho^3 + \rho^5 + \rho^7)]}$$

Where:

T_{PD} = The electrical length of the correcting Z_{01} section

T_C = The time constant formed between the parasitic capacitor and Z_0

ρ = $(Z_{01}$ ï $Z_0) / (Z_{01} + Z_0)$

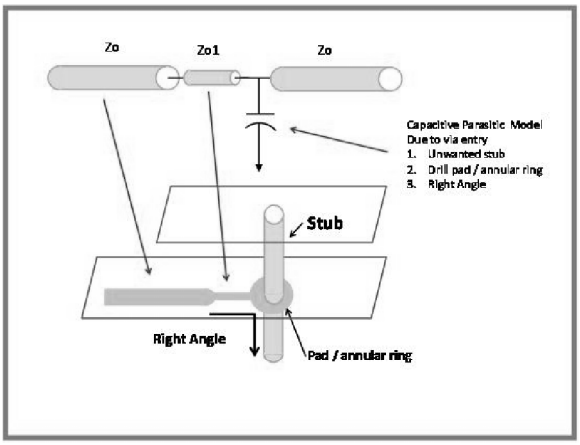

Figure 16: Correcting Via to trace Transitions

For a 0.4mm pitch device and a short via stub, the parasitic capacitance will range between 50 and 100 ff. This method, although bandwidth limited, will mitigate the perturbation effectively down to 10ps rise times. This approach is not limited to test applications; however, it is more effective in test because most test engineers tend to use wider, more pristine traces.

Performance Comparison

Figure #17 shows the authorsô first pass effort at creating an ultra-high fidelity loadboard, including a resonant structure around 48GHz. Even with this resonant point, the improved loss of the approach reduces correlated jitter (270fs) to levels below a comparable 3ò trace. (See Figure #18 and #19.)

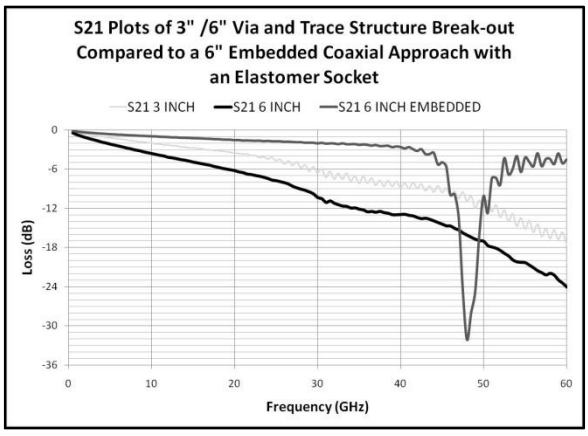

Figure 18: Comparison Results

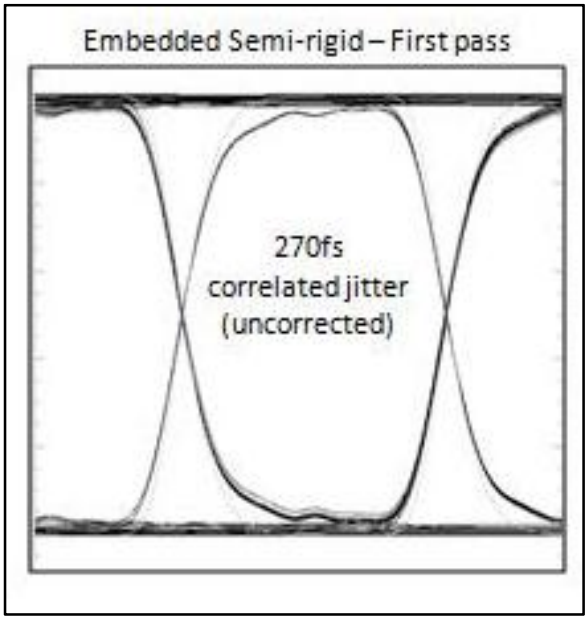

Figure19: Embedded Semi-rigid Results

Repeatability and Reproducibility

Because the high fidelity approach using emerging technologies is new, exact repeatability for 25GB/s links is not fully studied at the creation of this paper. Preliminary work in on high frequency RF circuits using embedded technologies suggests that repeatability improves approximately one order of magnitude.

Cost of Emerging Technologies

Adding the embedded coaxial via and air-core structures increases the cost of the load board approximately 50% over a board using standard methods and materials. Relative to premium materials, such as a Teflon™ material, the cost is significantly less. However, the cost must be considered in terms of the total cost of ownership. If the overall loss and board to board variation have been reduced, then so have yield-impact considerations for 25GBps devices.

Concluding Comments

This paper first presented the unique challenges for testing at 25GB/s relative to current serial data testing. In summary:

1. Device Pitch and via structure through the loadboard.
2. Transition of the via to the stripline (or microstrip).
3. Requirement for narrower lines.
4. Printed circuit board material, press and etch tolerances.
5. Socket Interfaces.

All of these challenges may be overcome through various techniques, which apply generically to any test method approach. Most note worthy were the Z_{01} correction length for the via transition and the use of a high performance, low profile socket (i.e. elastomeric socket).

When applied to a desired high fidelity test philosophy, these issues result in disastrous repeatability issues from board to board. Therefore methods must change for the implementation of the loadboard and socket:

1. An elastomeric socket
2. Embedded coaxial vias
3. Embedded coaxial horizontal structures
4. An elastomeric interface to the instrumentation or the external loopback scheme.

The first pass prototype work for this type of a high fidelity board outperformed the existing technology significantly. It also promises a much higher level of site to site repeatability. However, the process has room to improve and mature.

Even though the initial loadboard cost is higher, the emerging approaches can ultimately save an implementing test engineer significant time and money in developing 25GB/s test interfaces.

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