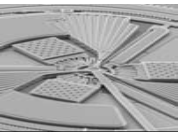
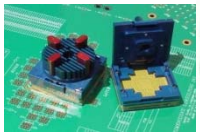
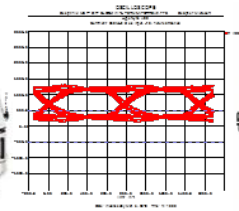
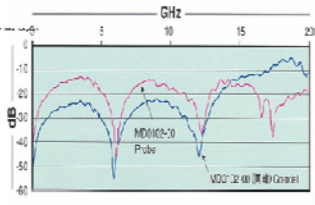





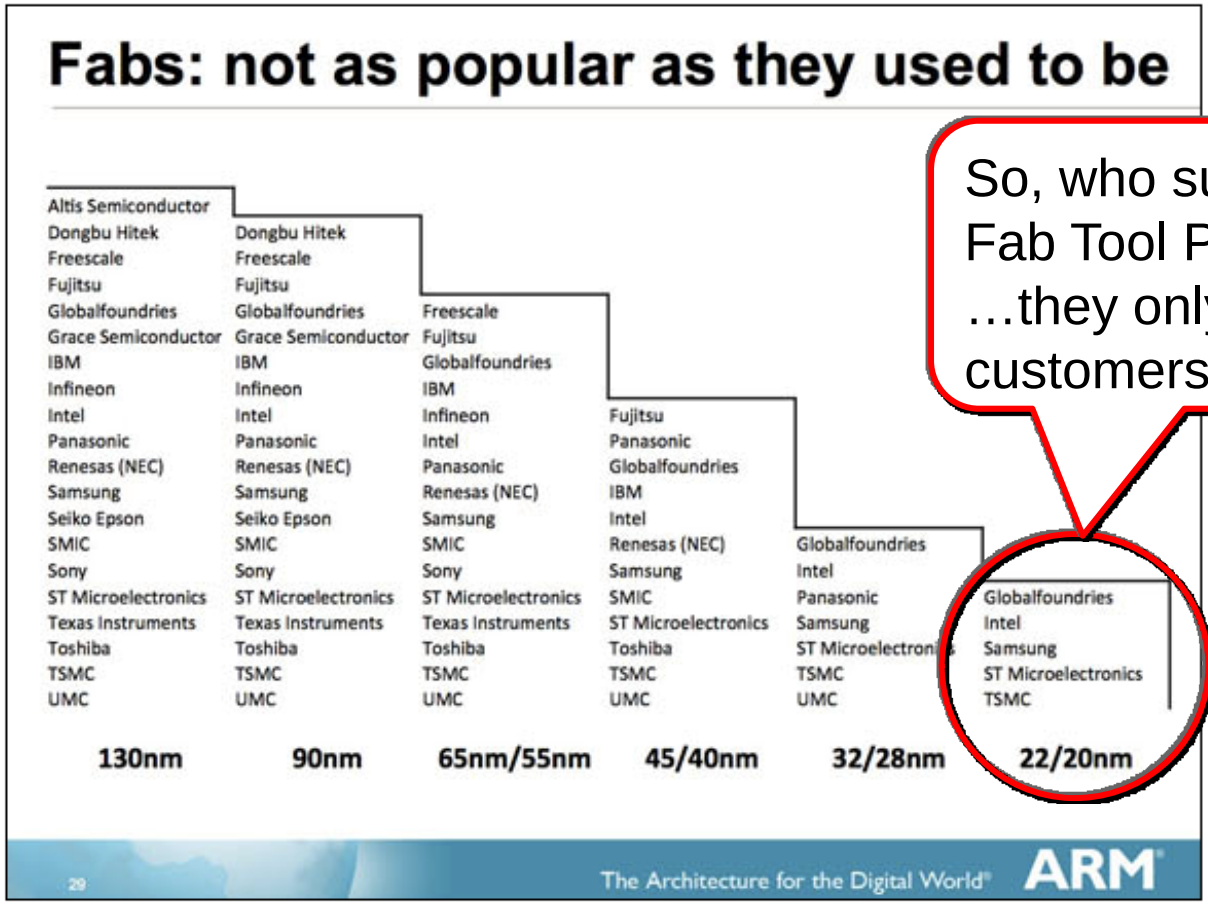



# IJTAG Test Strategy for 3D IC Integration

Al Crouch
ASSET InterTech
acrouch@ASSET-InterTech.com

# Why 3D?

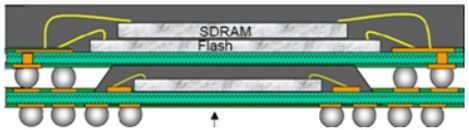


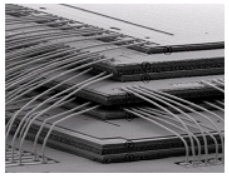

As process size shrinks, so do the number of fabs able to produce chips at those geometries (click to enlarge)

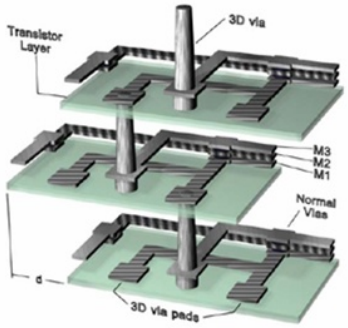
# 3D Packaging vs 3D ICs



## 3-D Packaging to 3-D IC Integration



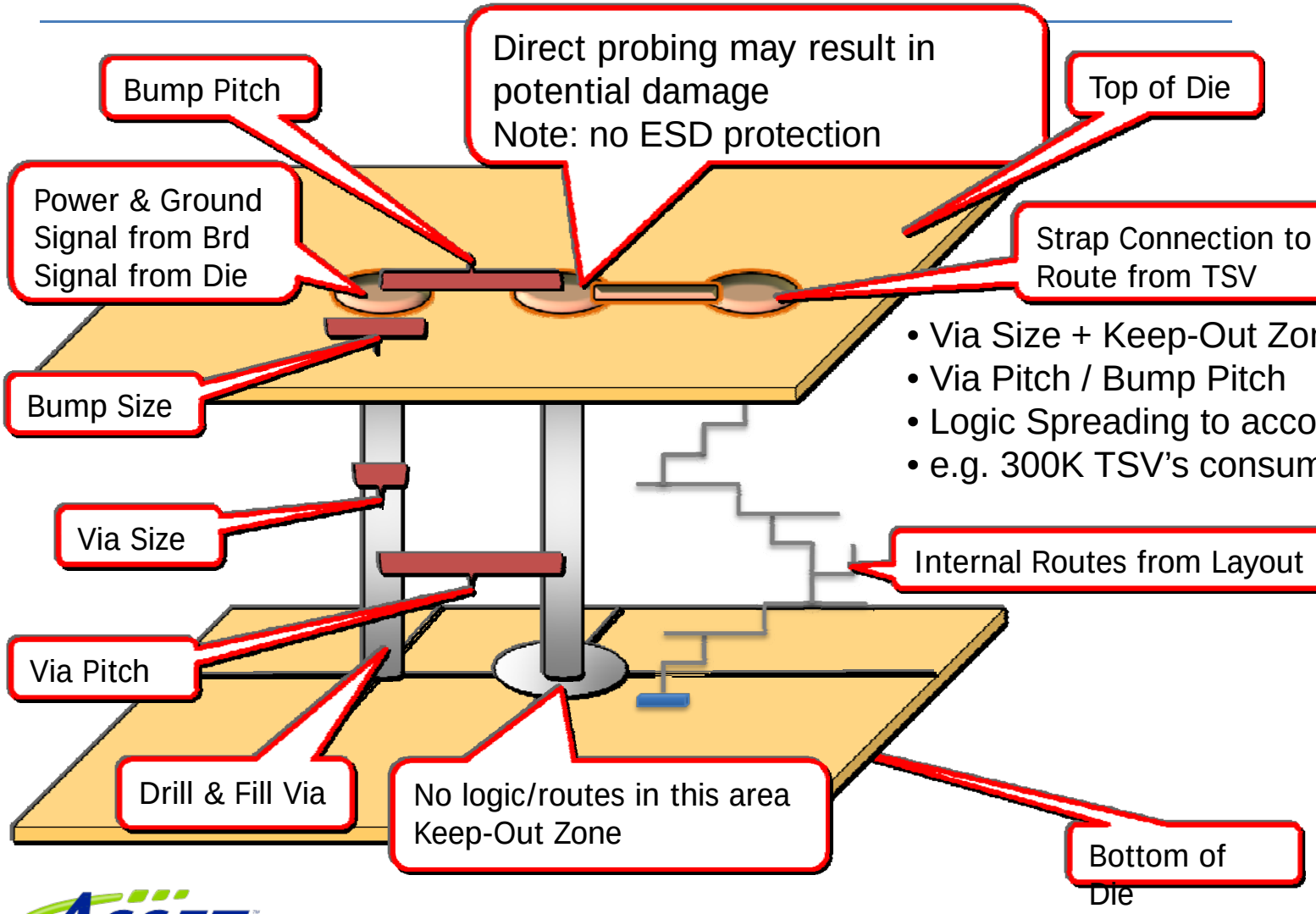






- Through-silicon (wafer) vias (TSVs)
- Wafer thinning
- Wafer (die) bonding

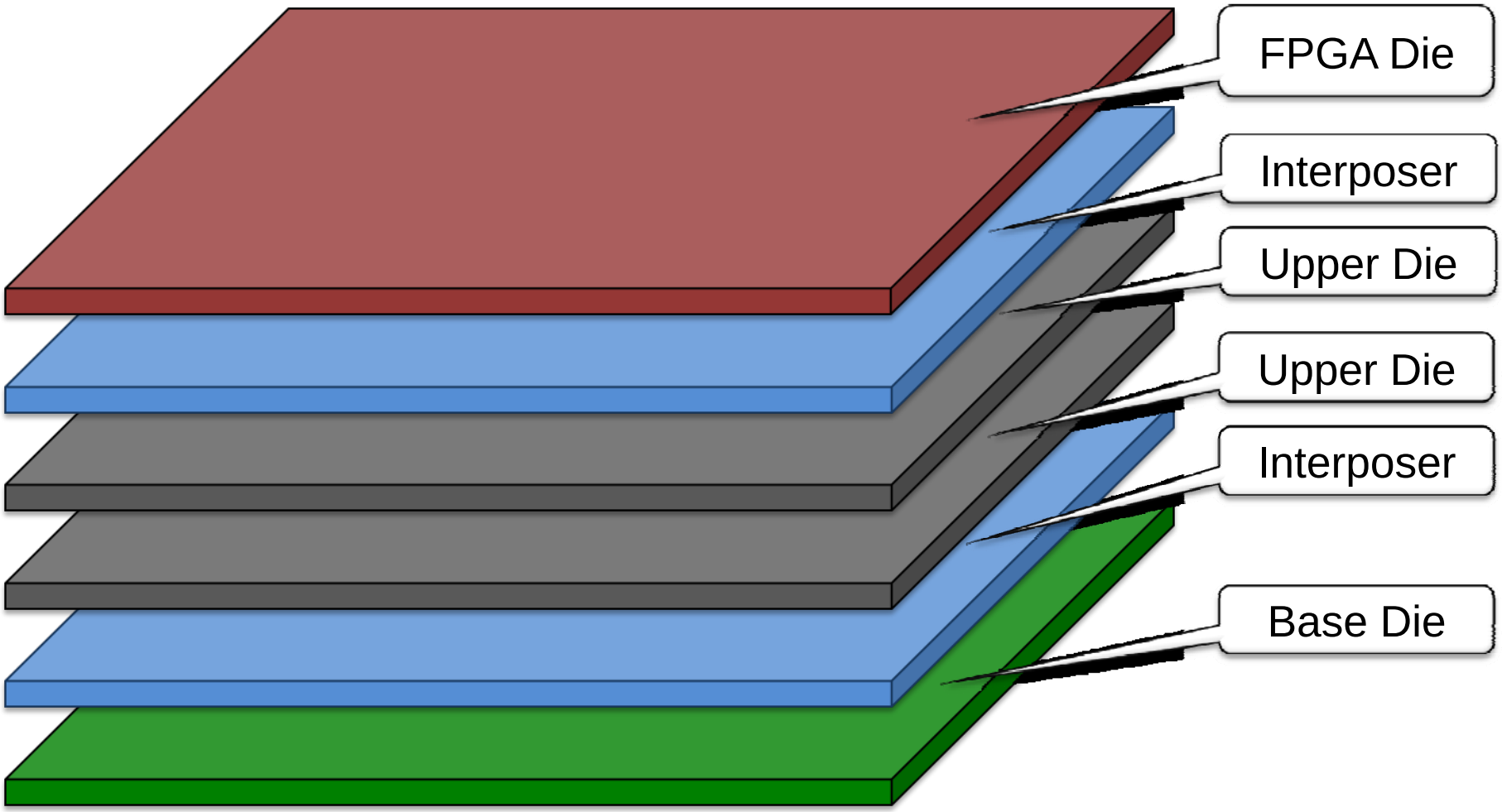
Webcast: Through-Silicon Vias: Ready for Prime Time?, *Semiconductor International*, 3/25/2008

# 3D TSV's

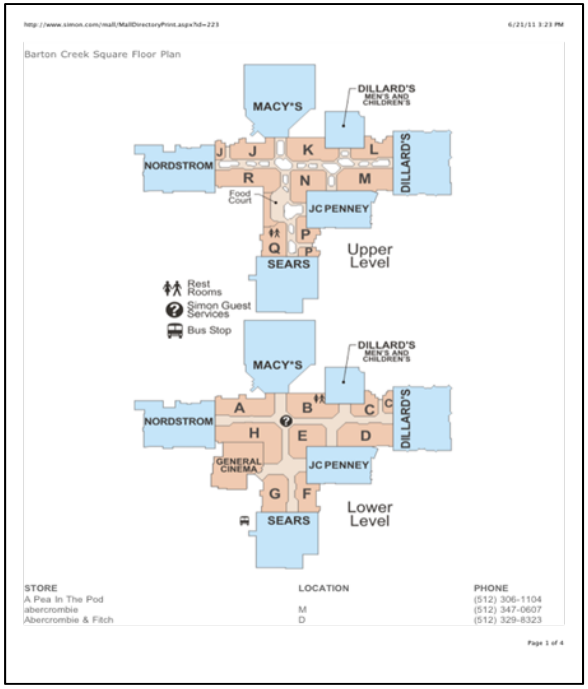



- Via Size + Keep-Out Zone
- Via Pitch / Bump Pitch
- Logic Spreading to accommodate TSVs
- e.g. 300K TSV's consume 1mm$^2$

# The 3D Stack


FPGA Die
Interposer
Upper Die
Upper Die
Interposer
Base Die

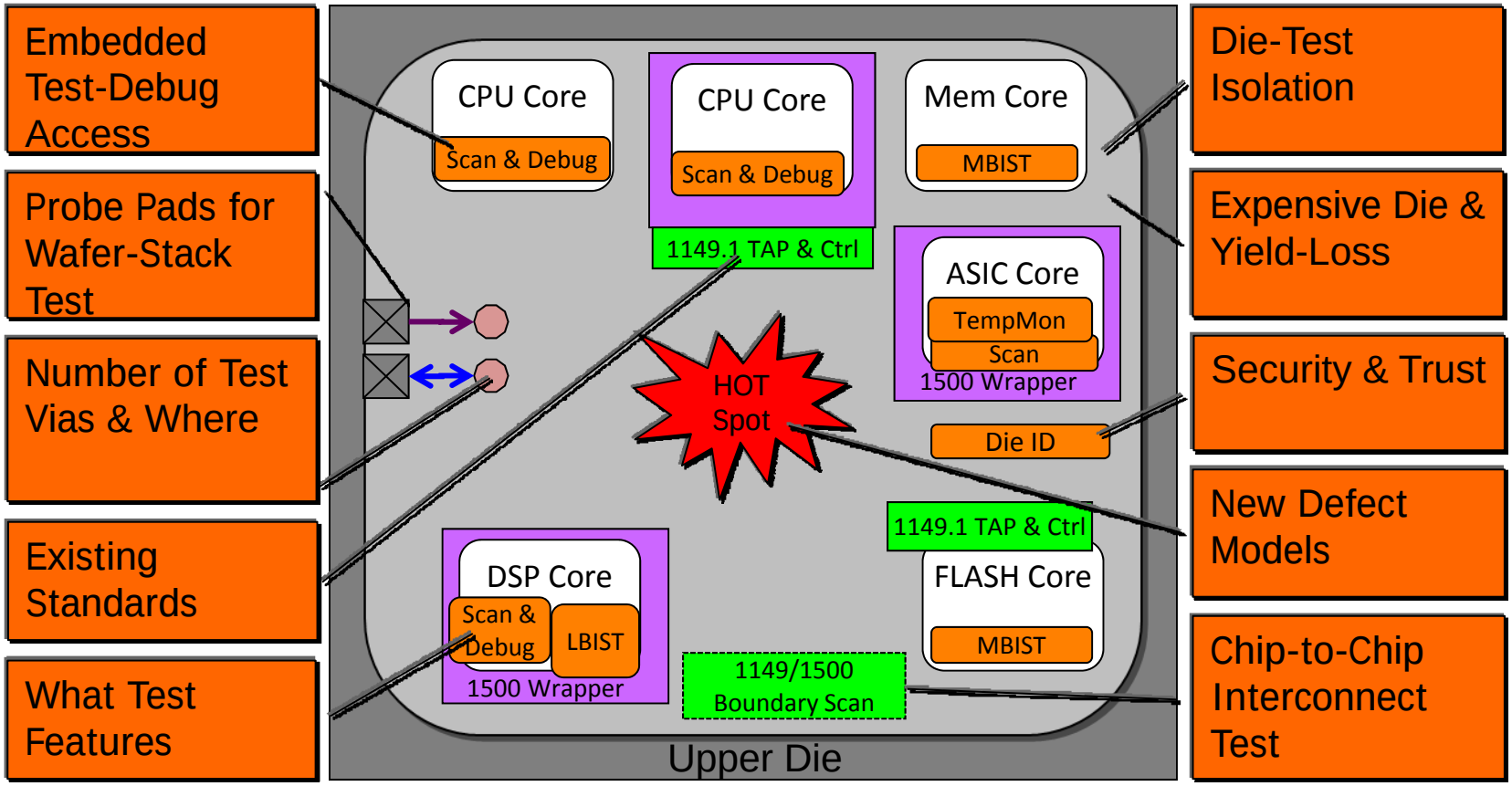
# 3D Now vs 3D Future



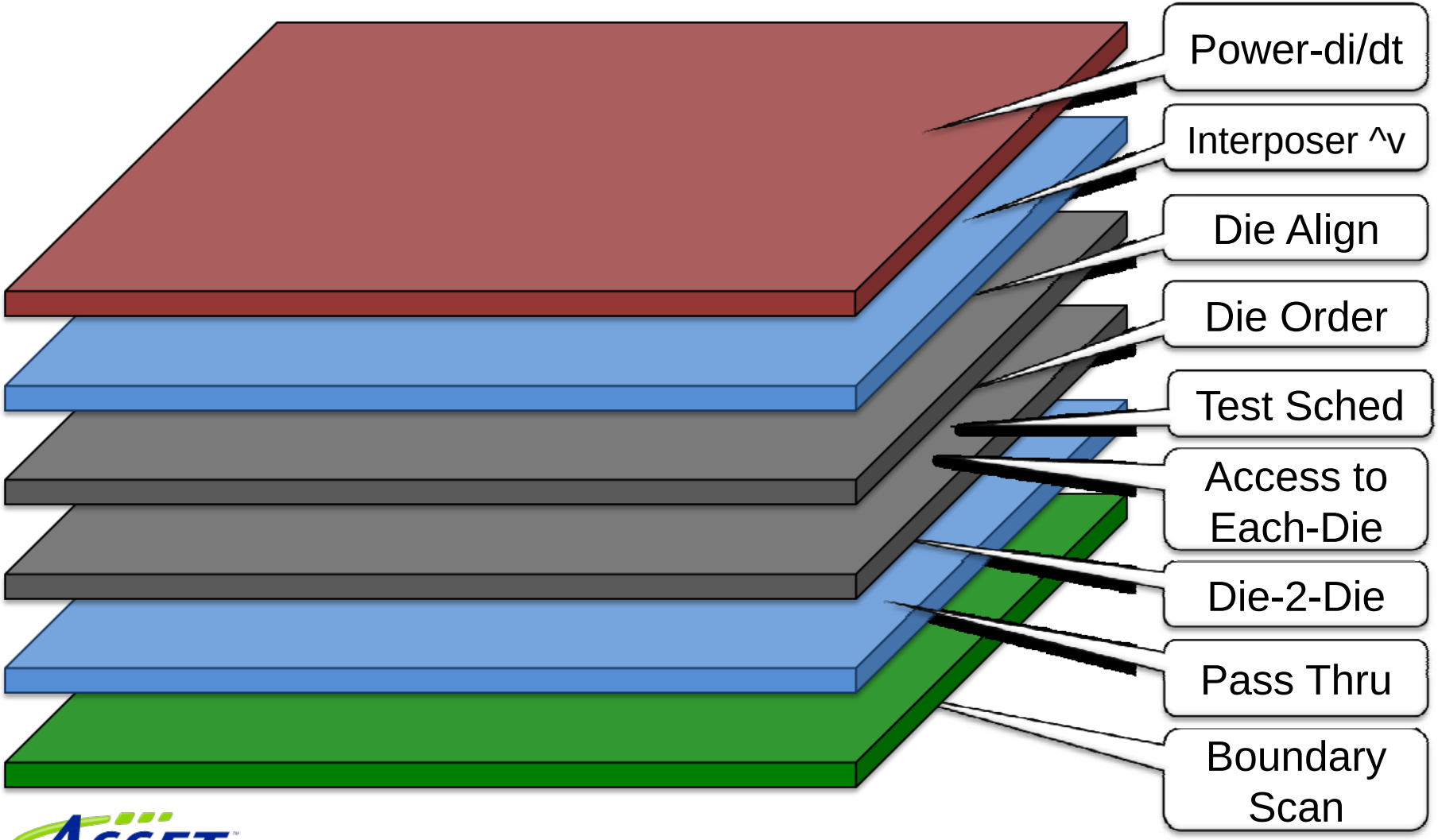

- Flat Layout & N-S/E-W space
- Routing N-S/E-W lengths
- Stacking TSV displacement
- Today's CAD/CAE Tools

- Vertical Layout from the start
- Core/Elevators at heart of design
- Routing distance is X, Y, or Z
- Stack Engineering New CAD/CAE

# The 3D Die Concerns



# 3D Stack Concerns



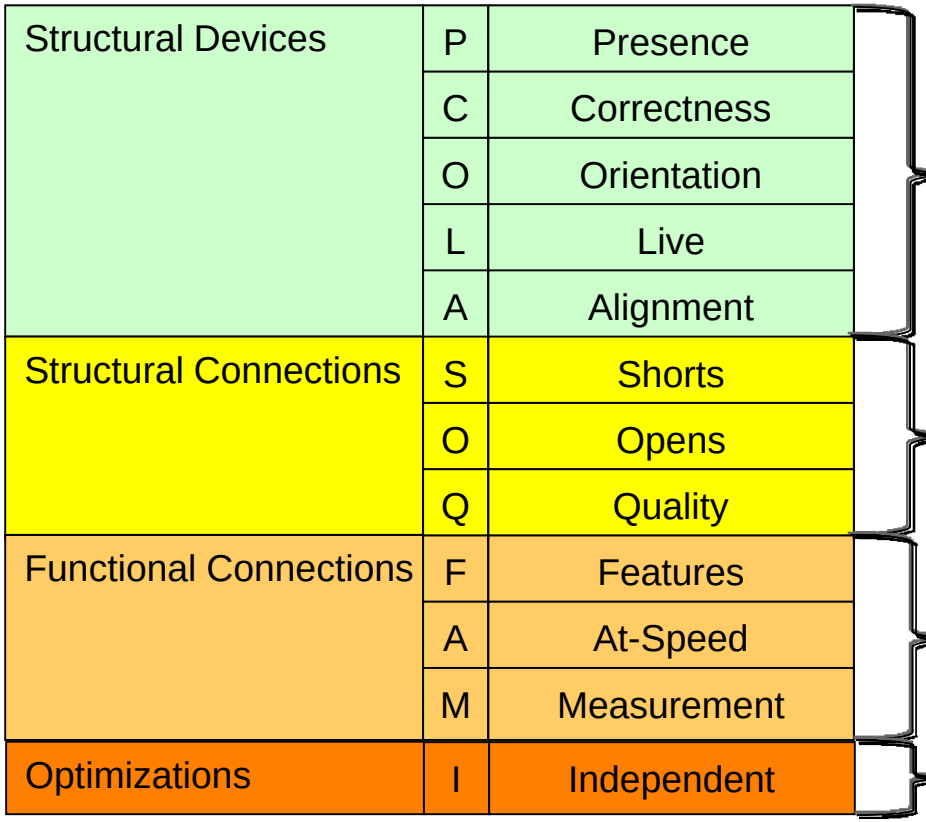
# What is being tested?

- There are Chip (IC) Tests
  - Fault Coverage (e.g. Stuck-At, Path Delay, Transition Delay, n-Detect)
  - Defect Coverage (shorts, opens, bridges, GOS)
  - Parametrics (Max FRQ, Leakage – iDDQ, IOH,IIL, VOH, VIL)
  - Functional (Read, Write, Bus Transactions, etc.)
  - Embedded BIST (Logic, Memory, HSIO)

- There are Board Tests
  - PCOLA
  - SOQ
  - FAMI

3D Test is a combination of Both

# Board Test Concerns




**PCOLA** tests are tests that verify the **P**resence of a chip in a socket or at a board location; that it is the **C**orrect chip; and is **O**riented correctly; receives power and is **L**ive; and is **A**ligned correctly

Boundary Scan Tests and External Equipment (ICT, X-Ray) and Visual Inspection

**SOQ** tests are tests that verify the connections/signals to the chip to be free of **S**horts and **O**pens; and can assess the **Q**uality of the connection's solder joints

Boundary Scan Interconnect Test and X-Ray

**FAM** tests are tests that can operate or verify a **F**eature of the chip; can be applied **A**t-speed; and that allow a **M**easurement to be taken

Functional Tests

**I** tests are tests that can be operated **I**ndependently so they can be scheduled in parallel to reduce test time

Simultaneous and Concurrent Tests

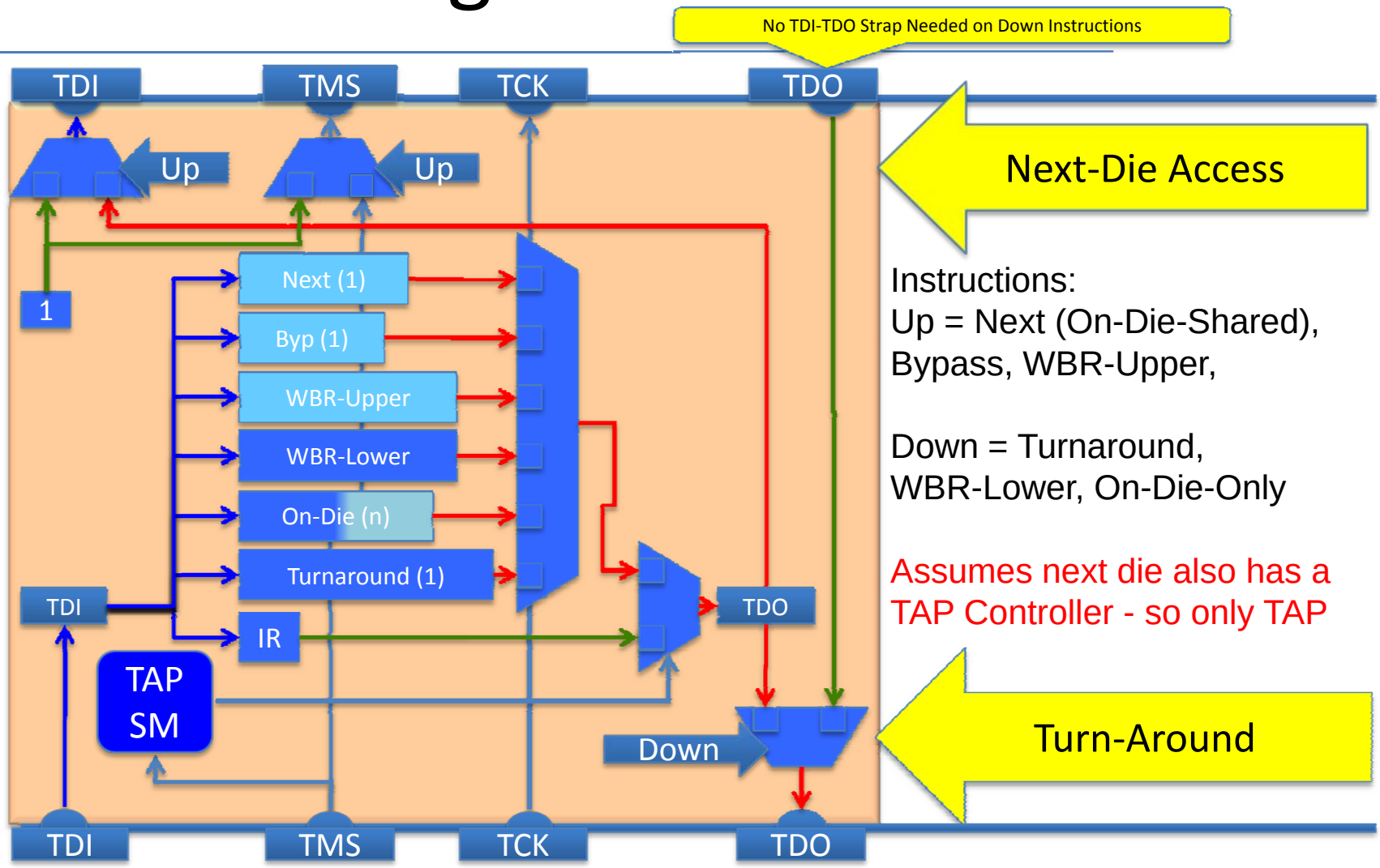
# Use of IEEE Standards?

- 1149.1 is the Base Standard that provides the “protocol”
  - Instruction-Based, Register-Based, Defines the “State-Machine”
  - Defined to assist with Board Test, Described with BSDL/SVF
- 1500 is a derivation used for Core Test
  - Instruction-Based, Register-Based
  - Defined to assist with Cores (Virtual Chips), Described with CTL/STIL
- 1687 is a departure to address certain weaknesses in 1149.1/1500
  - Vectors are defined at the Instrument
  - Mixes Instruction and Data, Defined to assist with Instruments
  - Network-Based (variable length scan paths), Described with ICL/PDL
- 1149.7 can reduce 1149.1’s TAP to just 2 Pins
  - Defines a TDMA packet protocol

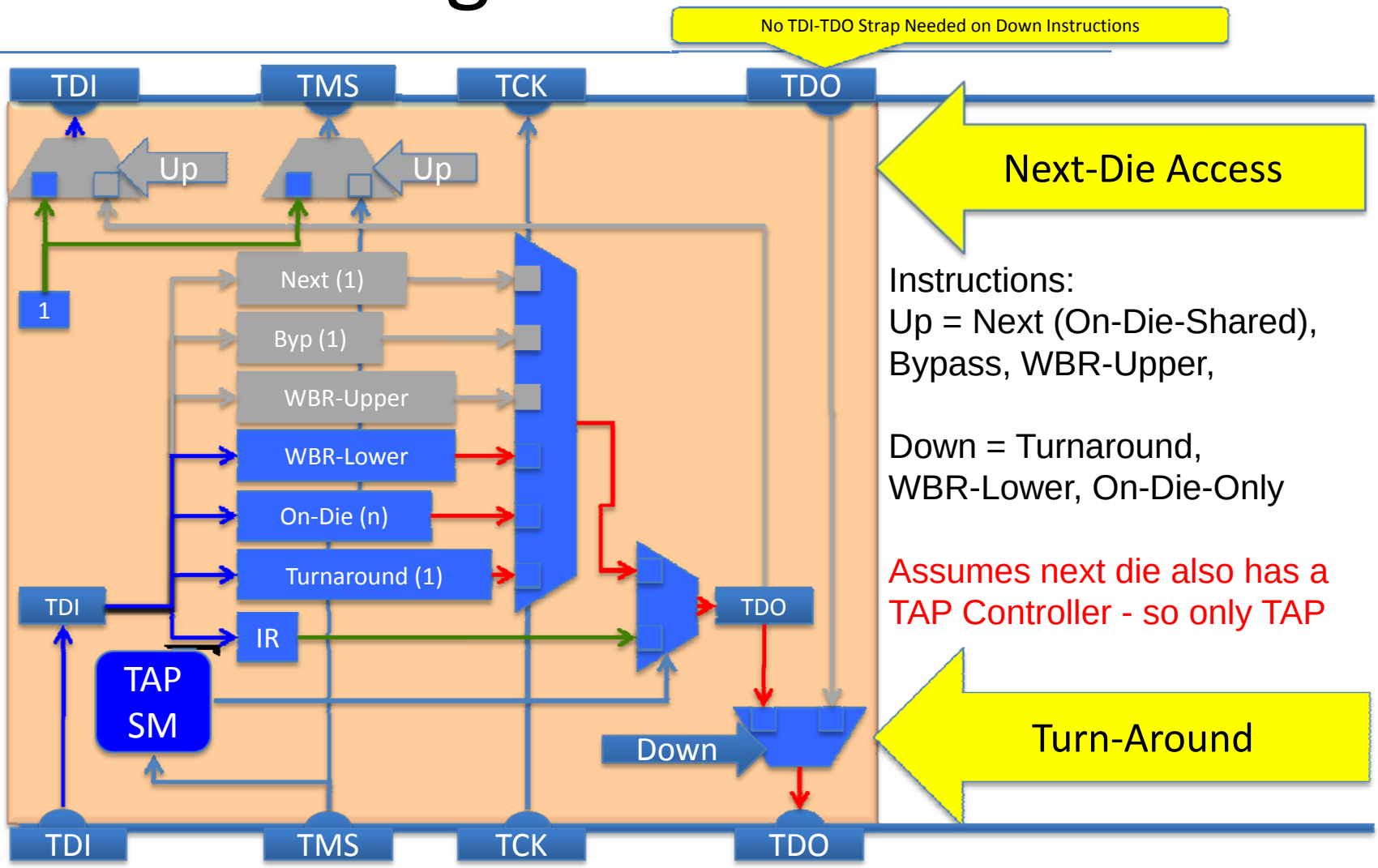
# Die Access Functions

- Any individual die must provide access functions if applicable
  1. There must be an Access Turn-Around
     (terminate access at this die)
  2. If there is to be an Upper die (above this die), then there must be an Access Bypass or Access Pass-Through
     (skip this die without on-die access)
  3. If there is on-chip test/debug logic, then there must be the ability to have On-Die Access
  4. If there is on-chip test/debug logic and an Upper die (above this die), then there must be a combined On-Die Access and a Next-Die Access

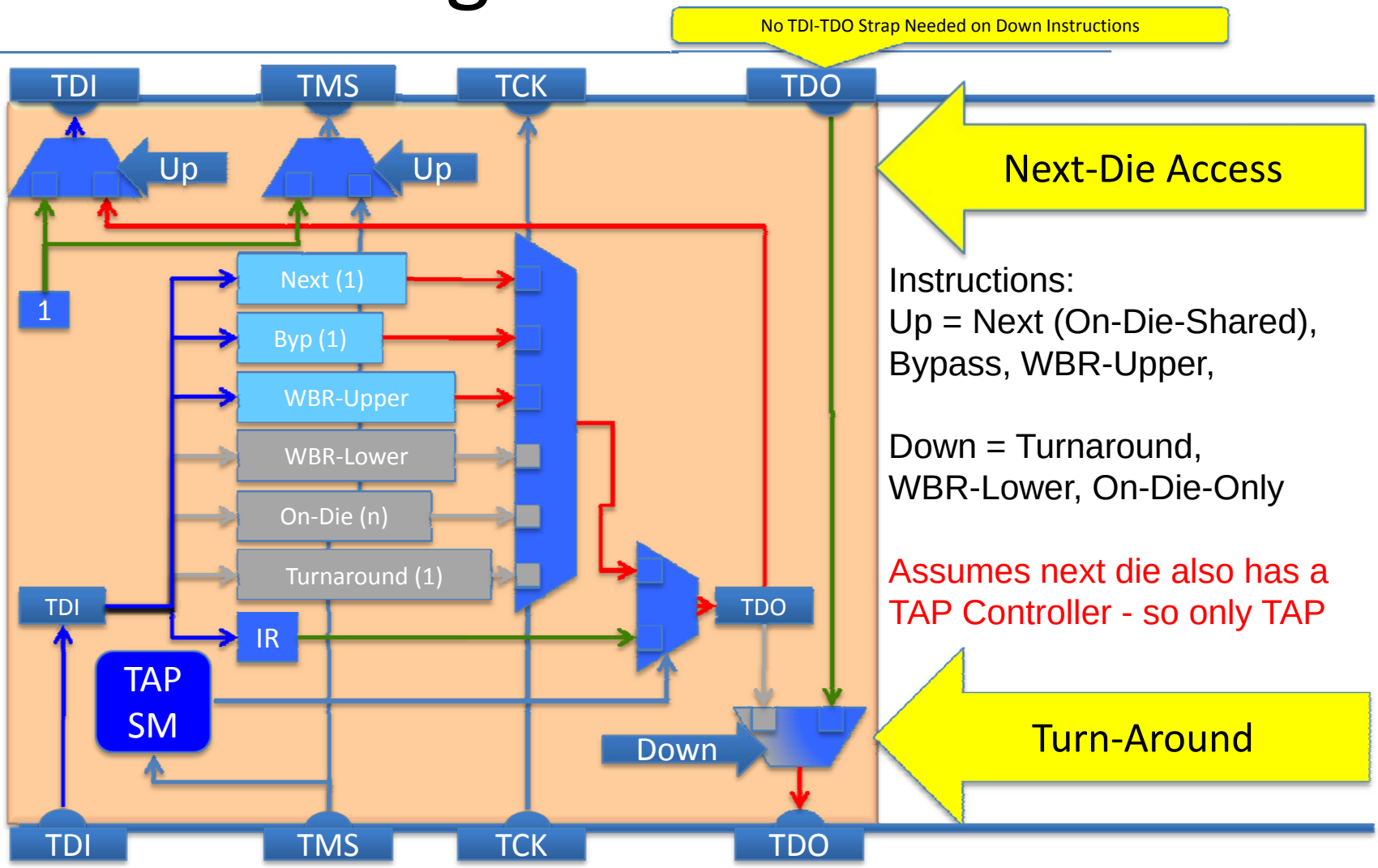
# Using 1149.1


No TDI-TDO Strap Needed on Down Instructions
TDI
TMS
TCK
TDO
Up
Up
1
Next (1)
Byp (1)
WBR-Upper
WBR-Lower
On-Die (n)
Turnaround (1)
IR
TDI
TDO
TAP
SM
Down
TDI
TMS
TCK
TDO
Next-Die Access
Instructions:
Up = Next (On-Die-Shared), Bypass, WBR-Upper,
Down = Turnaround, WBR-Lower, On-Die-Only
Assumes next die also has a TAP Controller - so only TAP
Turn-Around

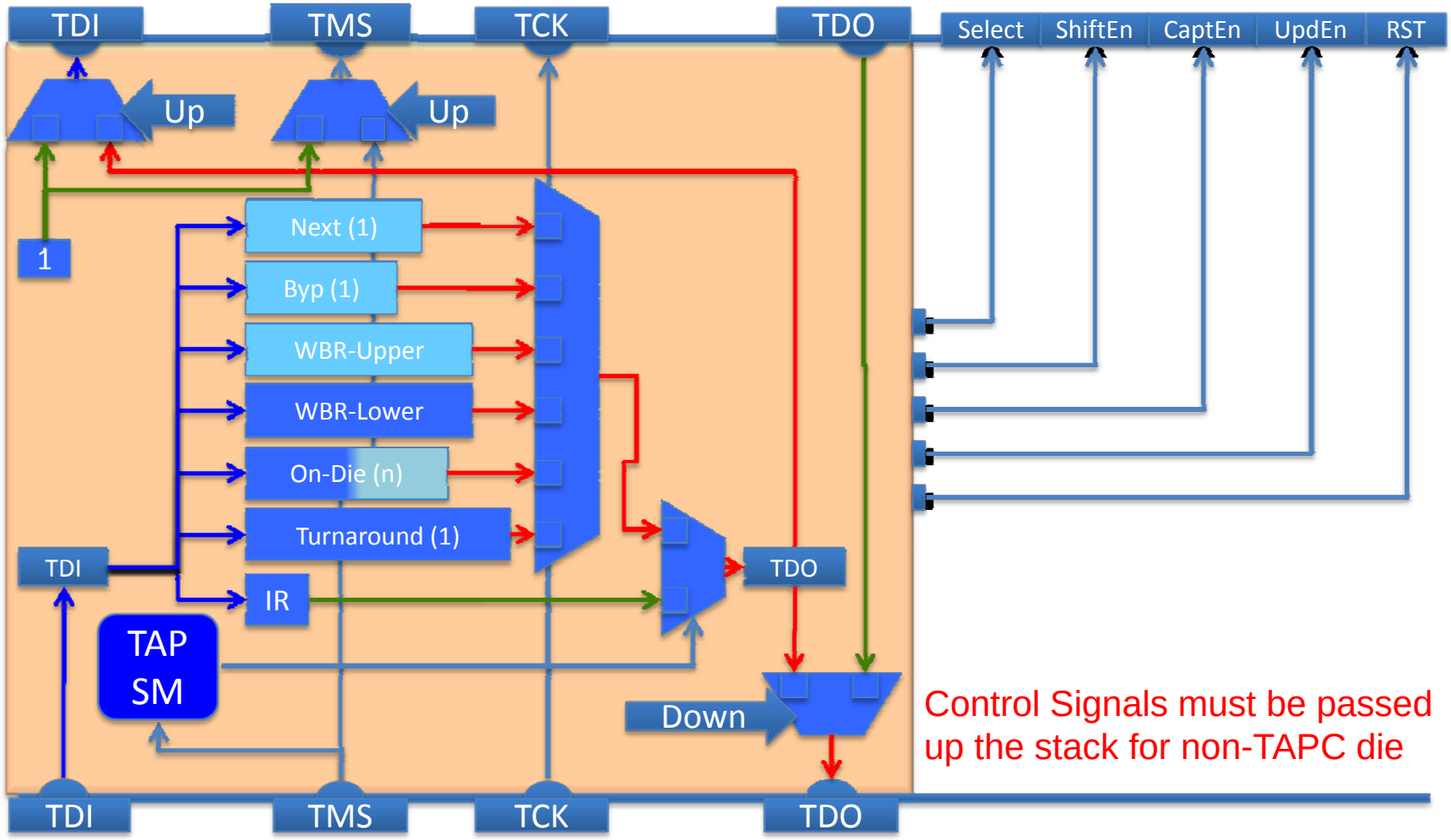
# Using 1149.1


No TDI-TDO Strap Needed on Down Instructions
TDI
TMS
TCK
TDO
Up
Up
1
Next (1)
Byp (1)
WBR-Upper
WBR-Lower
On-Die (n)
Turnaround (1)
IR
TDI
TAP SM
TDO
Down
TDI
TMS
TCK
TDO
Next-Die Access
Instructions:
Up = Next (On-Die-Shared), Bypass, WBR-Upper,
Down = Turnaround, WBR-Lower, On-Die-Only
Assumes next die also has a TAP Controller - so only TAP
Turn-Around

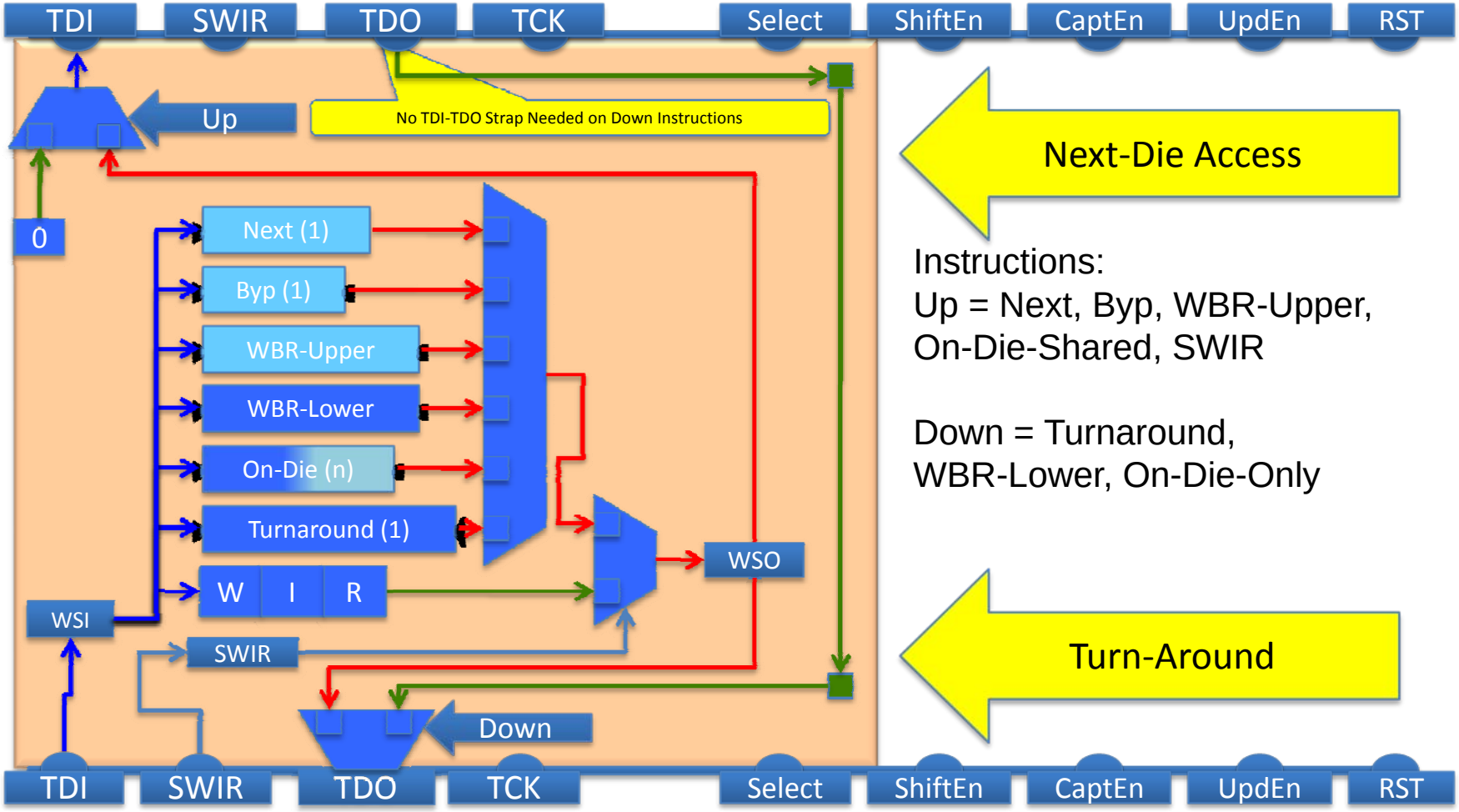
# Using 1149.1


No TDI-TDO Strap Needed on Down Instructions
TDI
TMS
TCK
TDO
Up
Up
1
Next (1)
Byp (1)
WBR-Upper
WBR-Lower
On-Die (n)
Turnaround (1)
IR
TAP SM
TDI
TDO
Down
TDI
TMS
TCK
TDO
Next-Die Access
Instructions:
Up = Next (On-Die-Shared), Bypass, WBR-Upper,
Down = Turnaround, WBR-Lower, On-Die-Only
Assumes next die also has a TAP Controller - so only TAP
Turn-Around

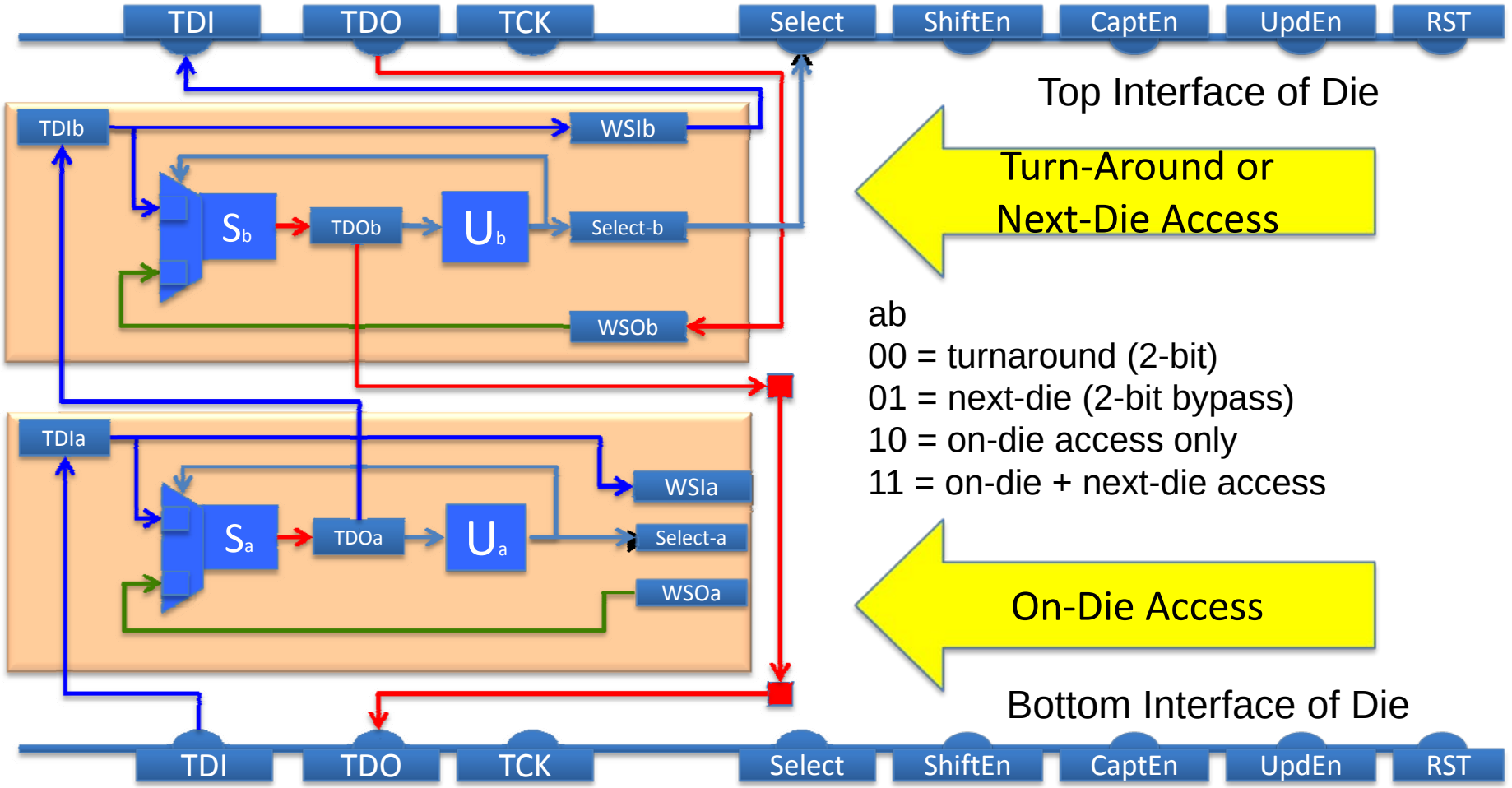
# Using 1149.1


TDI
TMS
TCK
TDO
Select
ShiftEn
CaptEn
UpdEn
RST
Up
Up
1
Next (1)
Byp (1)
WBR-Upper
WBR-Lower
On-Die (n)
Turnaround (1)
IR
TDI
TDO
TAP
SM
Down
TDI
TMS
TCK
TDO
Control Signals must be passed up the stack for non-TAPC die

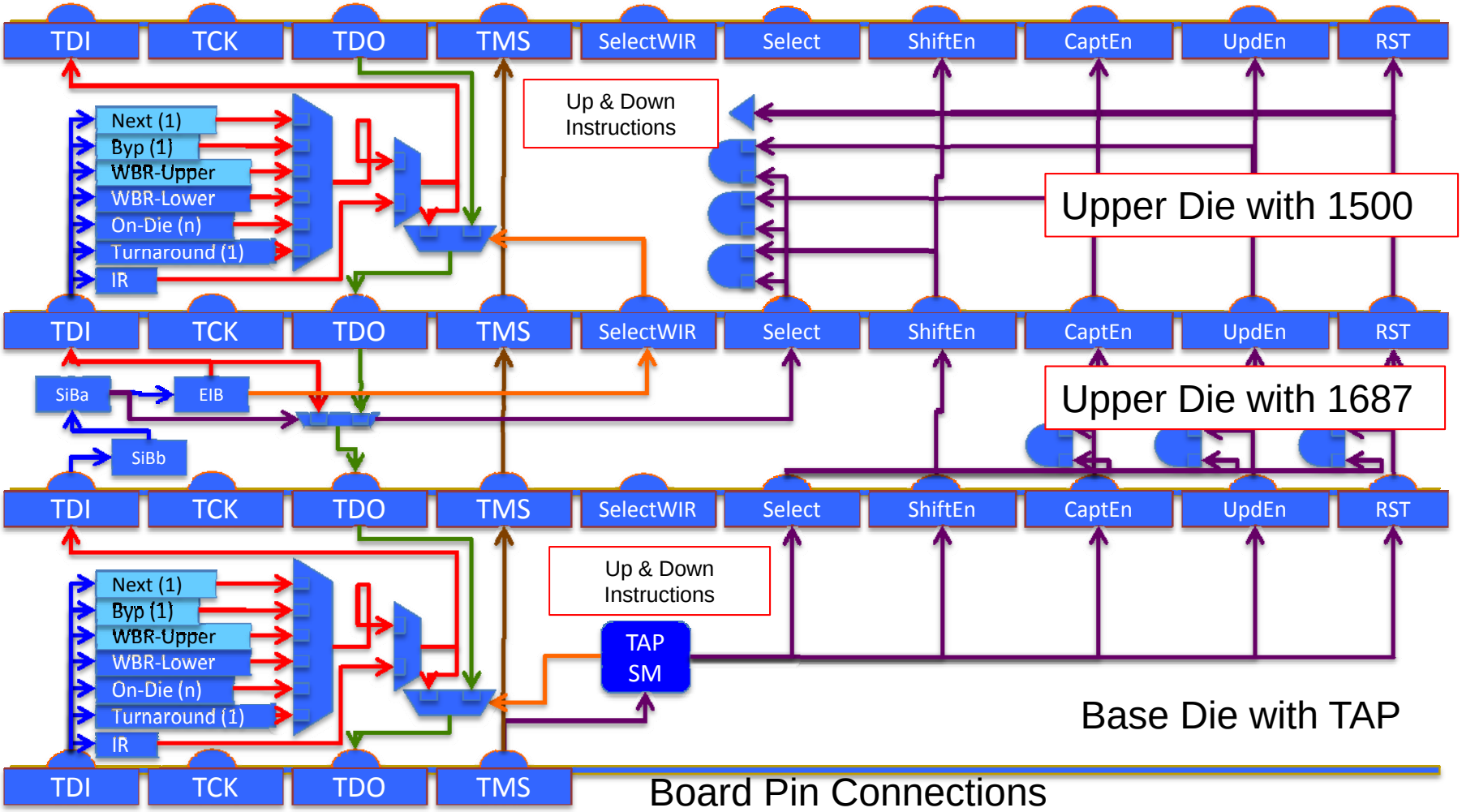
# Using 1500


TDI
SWIR
TDO
TCK
Select
ShiftEn
CaptEn
UpdEn
RST
Up
No TDI-TDO Strap Needed on Down Instructions
0
Next (1)
Byp (1)
WBR-Upper
WBR-Lower
On-Die (n)
Turnaround (1)
W
I
R
WSO
WSI
SWIR
Down
Next-Die Access
Instructions:
Up = Next, Byp, WBR-Upper, On-Die-Shared, SWIR
Down = Turnaround, WBR-Lower, On-Die-Only
Turn-Around

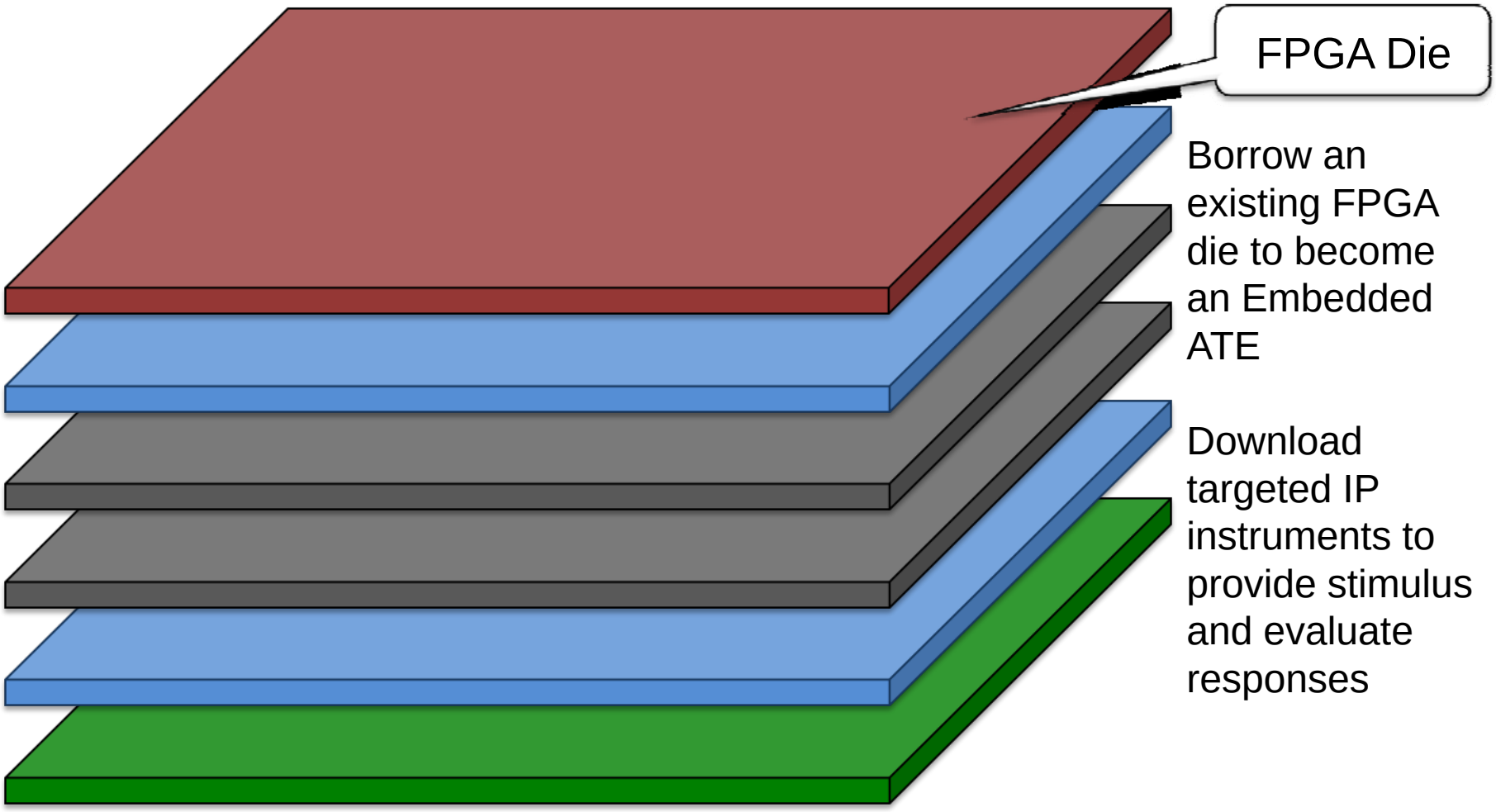
# Using P1687


TDI
TDO
TCK
Select
ShiftEn
CaptEn
UpdEn
RST
Top Interface of Die
TDIb
WSIb
Sb
TDOb
Ub
Select-b
WSOb
Turn-Around or
Next-Die Access
ab
00 = turnaround (2-bit)
01 = next-die (2-bit bypass)
10 = on-die access only
11 = on-die + next-die access
TDIa
WSIa
Sa
TDOa
Ua
Select-a
WSOa
On-Die Access
Bottom Interface of Die
TDI
TDO
TCK
Select
ShiftEn
CaptEn
UpdEn
RST

# Mixing Standards



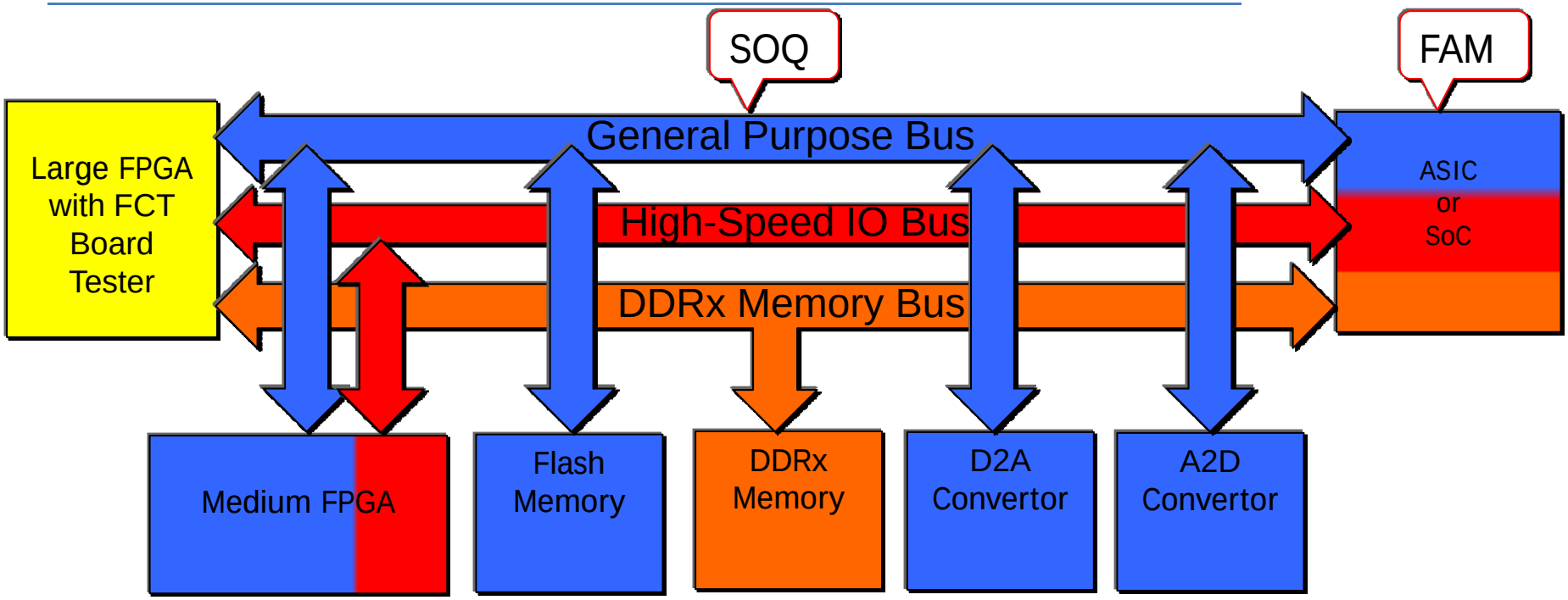
# The Embedded Tester




Borrow an existing FPGA die to become an Embedded ATE

Download targeted IP instruments to provide stimulus and evaluate responses

# FPGA Controlled Test




**FCT Tester Coverage:**

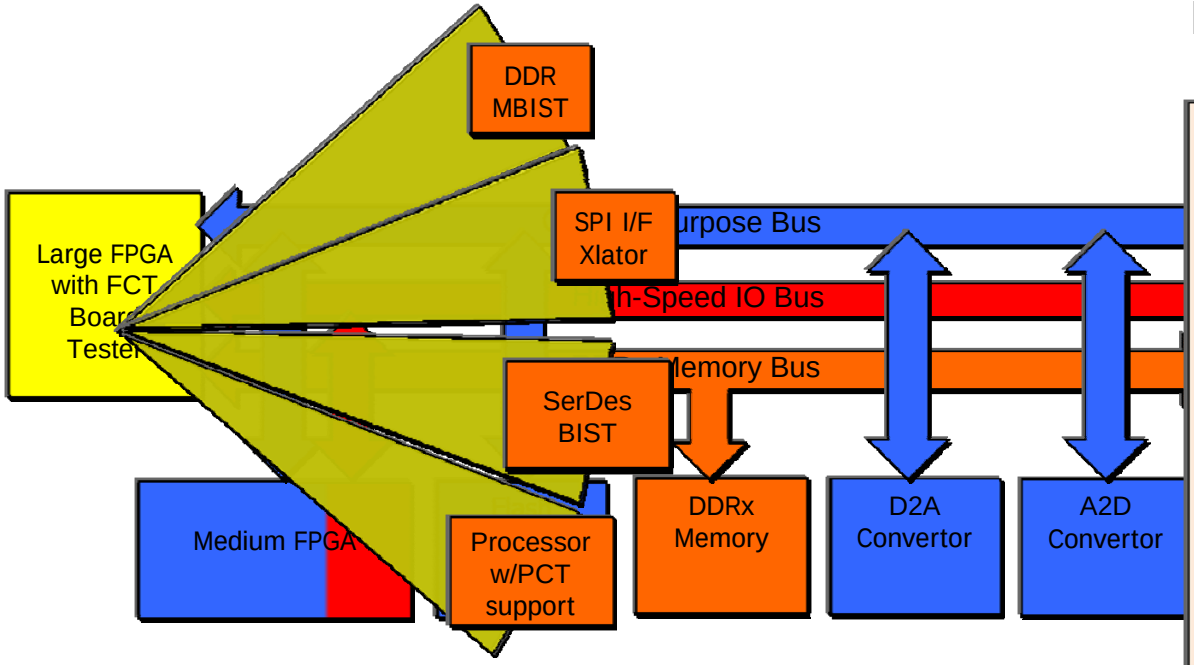
GPB coverage

HSIO coverage

DDRx coverage

# FCT Test Instruments

1. Identify board with FPGA as an opportunity for Embedded ATE
2. Identify Test Goals of Peripheral (PCOLA, SOQ, FAM)
3. Identify needed instruments to meet Test Goals and usage environment (MFG Test, Debug, NPI Test Development, etc.)

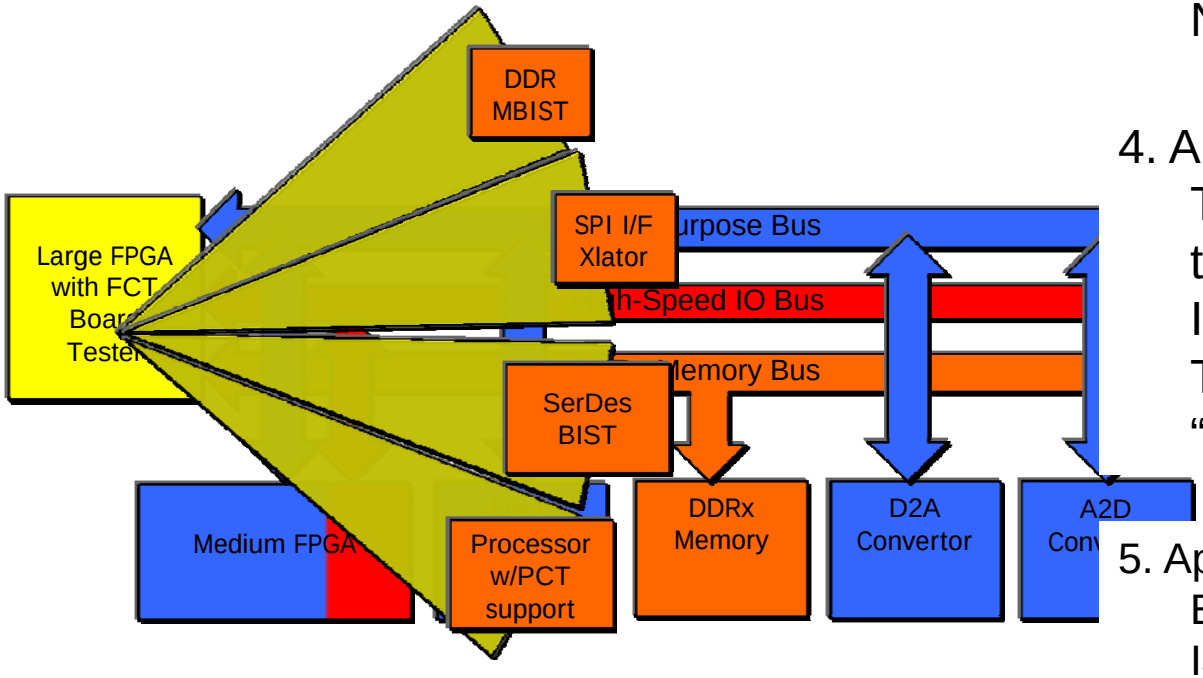



Common List of Instruments

1. Pattern Generator
2. Capture Buffer
3. Memory BIST/Test
4. SerDes BERT
5. HSIO Protocols (e.g. PCIe, XAUI, DDRx)
6. SPI/I2C Interfaces
7. D2A Waveform Gen
8. A2D/DSP Sampler
9. Clock Counters
10. Flash Programmer

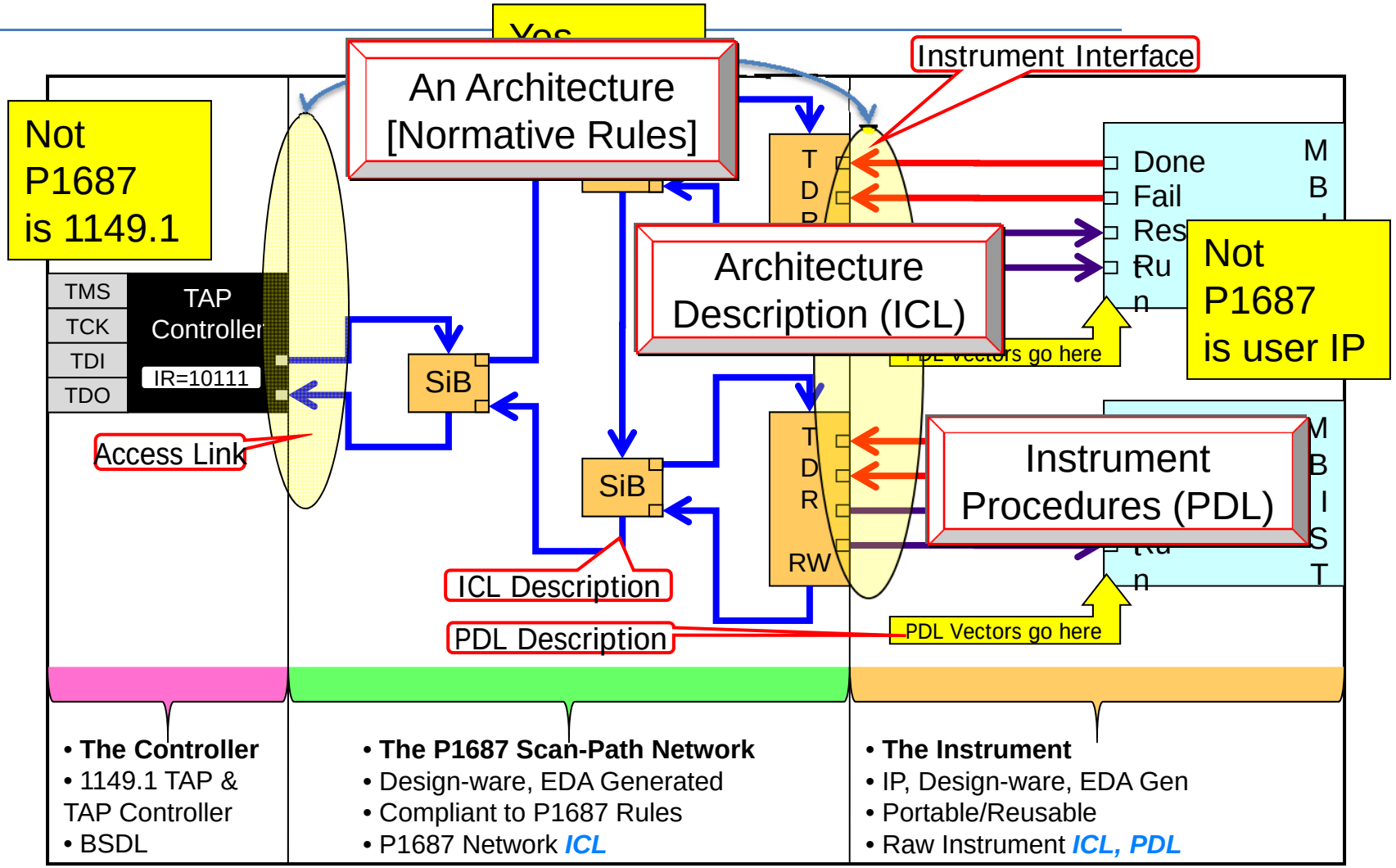
# FCT Methodology

1. Identify board with FPGA as an opportunity for Embedded ATE
2. Identify Test Goals of Peripheral (PCOLA, SOQ, FAM)
3. Identify needed instruments to meet Test Goals and usage environment (MFG Test, Debug, NPI Test Development, etc.)

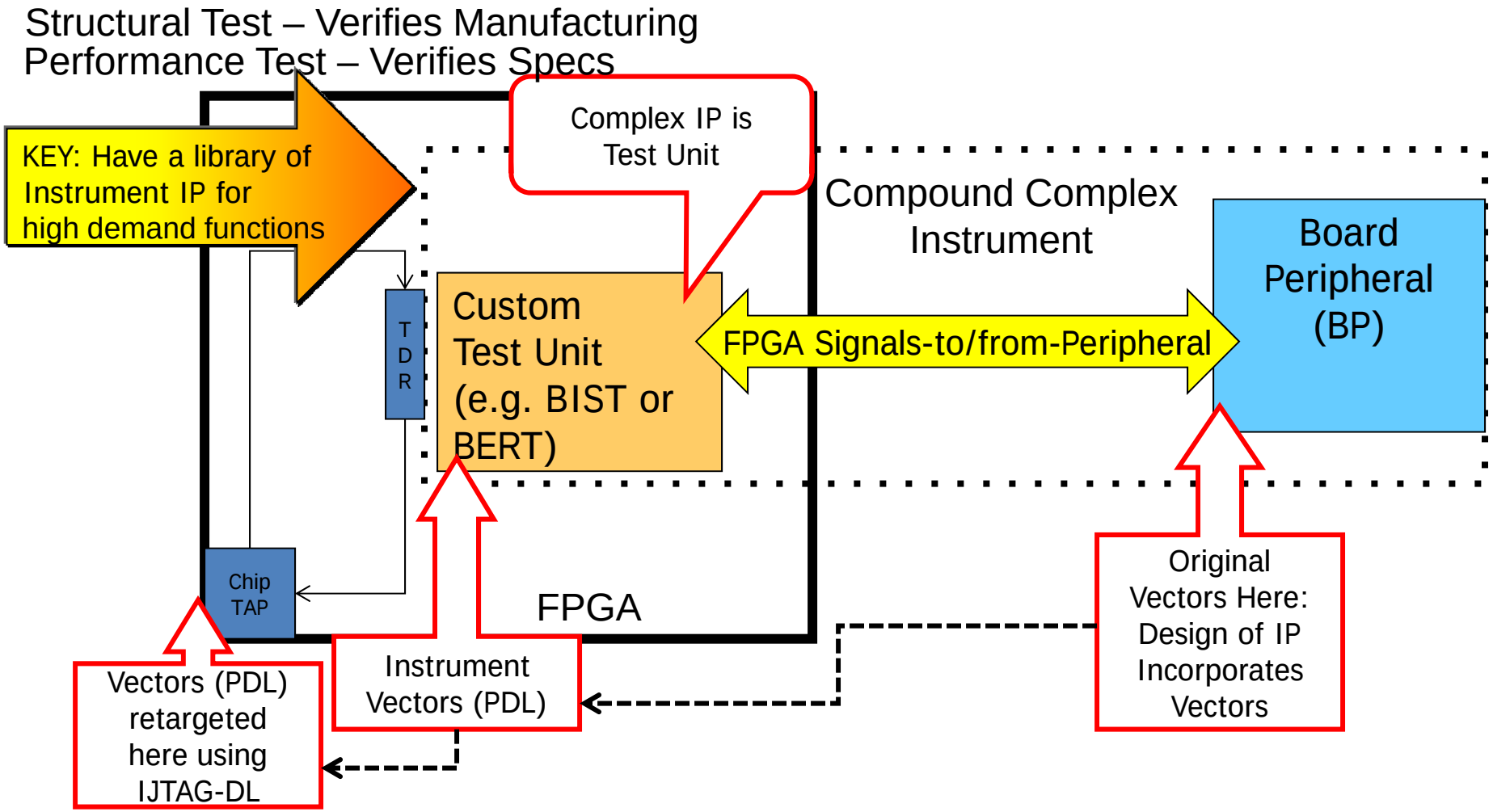



4. Apply the Embedded Tester Generator:
   to Create instruments plus IJTAG Network Bit File
   The tester may support many "Instruments" simultaneously
5. Apply the appropriate tools:
   Boundary Scan for Interconnect,
   IJTAG for Instruments,
   Emulation for Processor

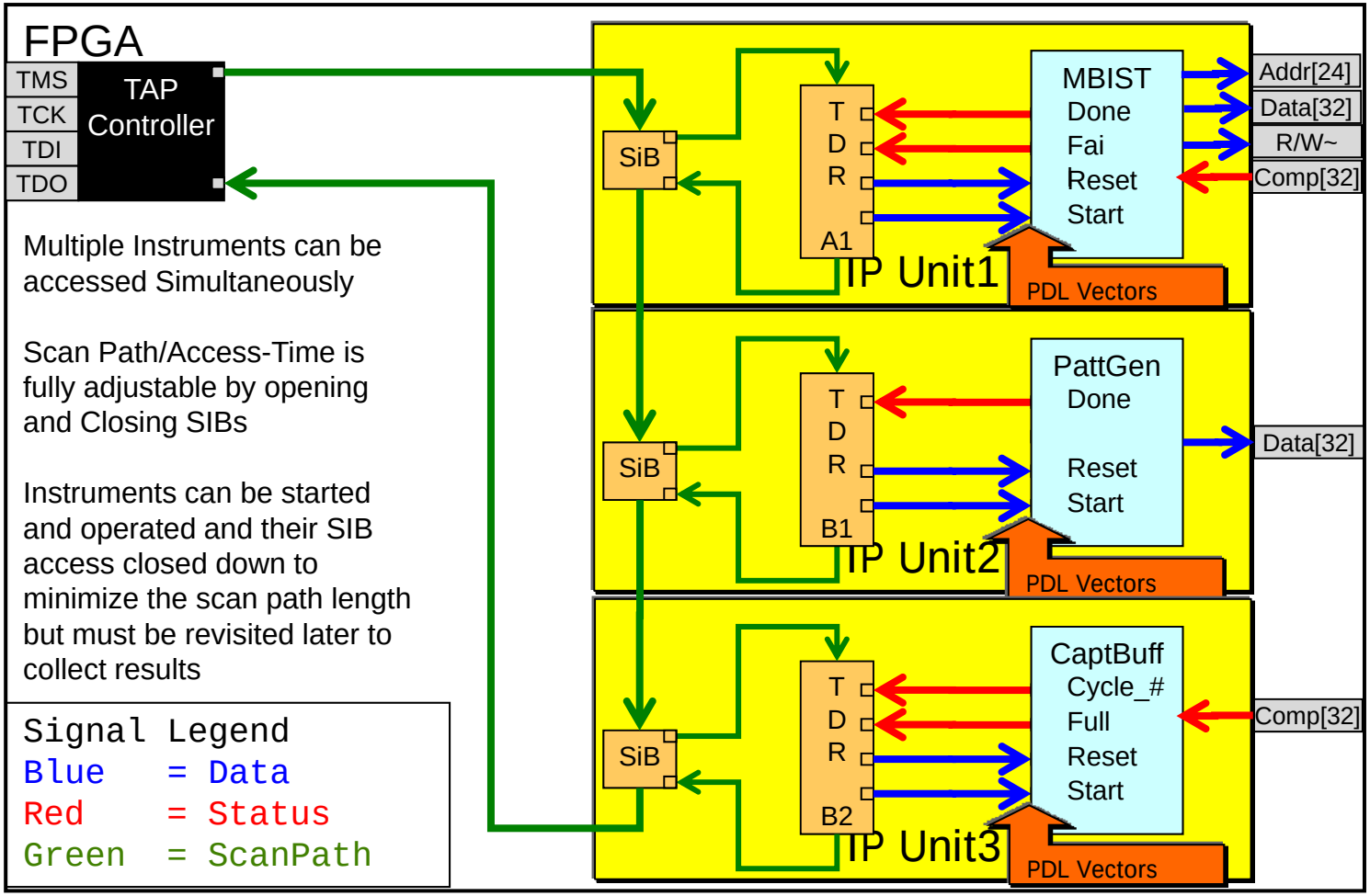
# Defining P1687



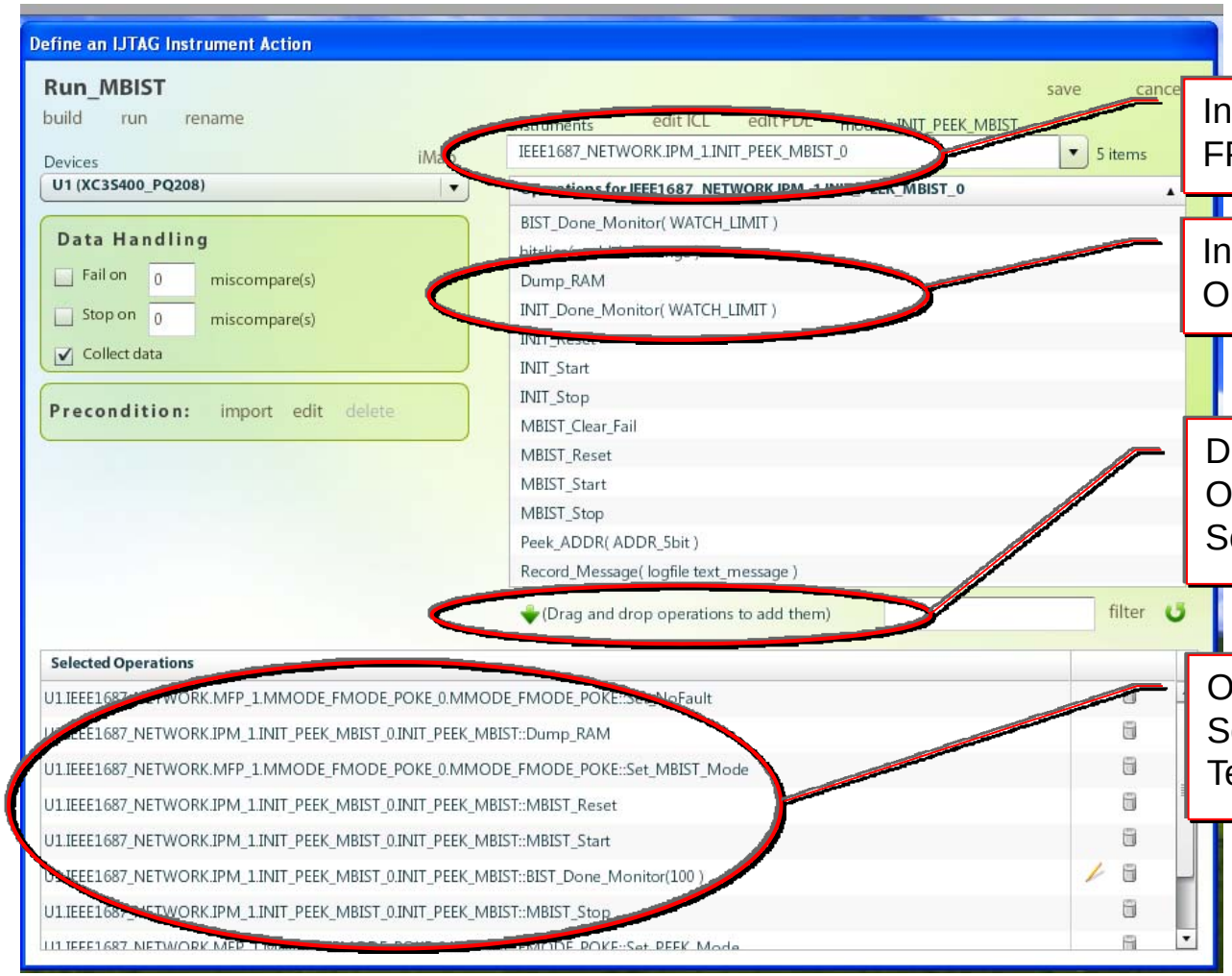
# Embedding a Tester



# P1687 Access to Tester



# Using P1687 as the OS



# Summary-Conclusions

- 3D is one way to extend Moore's Law
  - We are Stacking Shopping Malls today (not real 3D)
  - 3D comes with many test & debug concerns
  - Solutions must solve both IC Test and Board Test type issues
  - Access is the first item that must be solved
  - The density of functions will be so great that embedding the ATE may be the best solution
  - Similarly, including redundancy and fault-tolerance may be required
  - An ATE can be programmed into any FPGA type logic
  - P1687 enables both the Access and the FPGA Tester OS issues