Assessing CRES Performance for On-line Cleaning Optimization

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Overview

- Background
- Problem – Wafer Yield Fallout
  - Probe cleaning is needed
  - Effects of aggressive cleaning (technical and commercial)
- Challenge – Choosing a Cleaning Process
  - On-line process development is becoming difficult
  - Methodology for cleaning recipe development
- Implementation – Customer Benefits
- Summary

International Test Solutions – Who are we?

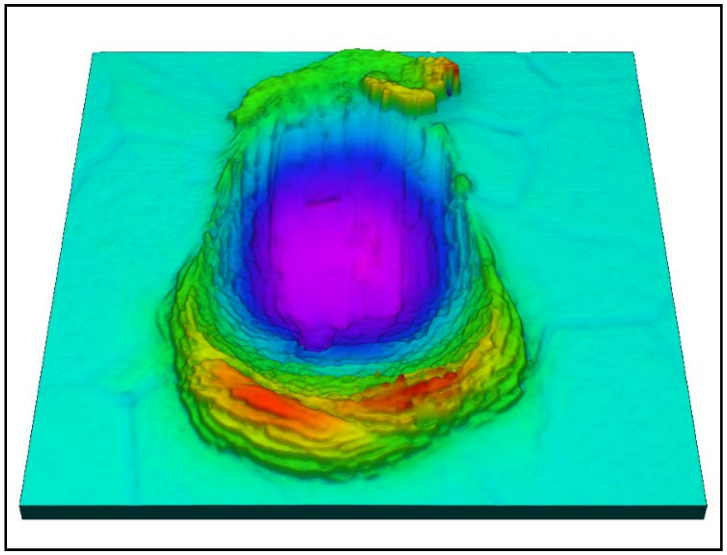
- Global supplier of highly engineered on-line and off-line cleaning materials for wafer sort and package test industries.
  - Cost-effective cleaning solutions and related technical support services focused on improvement solutions.
  - Patented processes and materials (UPTO 6,777,966 and 7,202,683)
  - Pending US and International IP applications for front-end, wafer-sort, and back-end testing.
- "Manufacturing Center" for advanced polymer materials
  - Controlled Compliance Technology (CCT) manufacturing methods.
  - Materials characterization, development, and testing laboratories.
- "Test Analysis Center" for performance characterization.
  - Analytical laboratory focused on CRES performance testing.
  - Probe technology and cleaning recipe assessment with optimization.

International Test Solutions – Where are we?

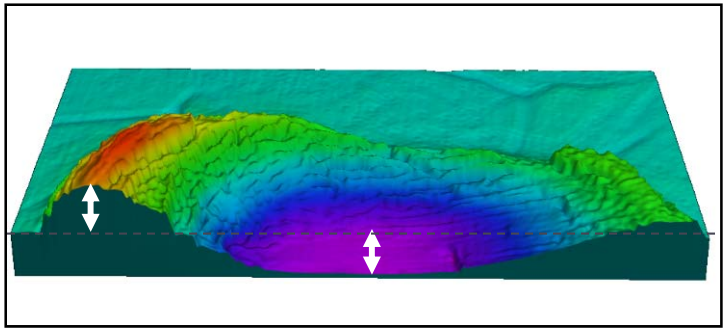
Background

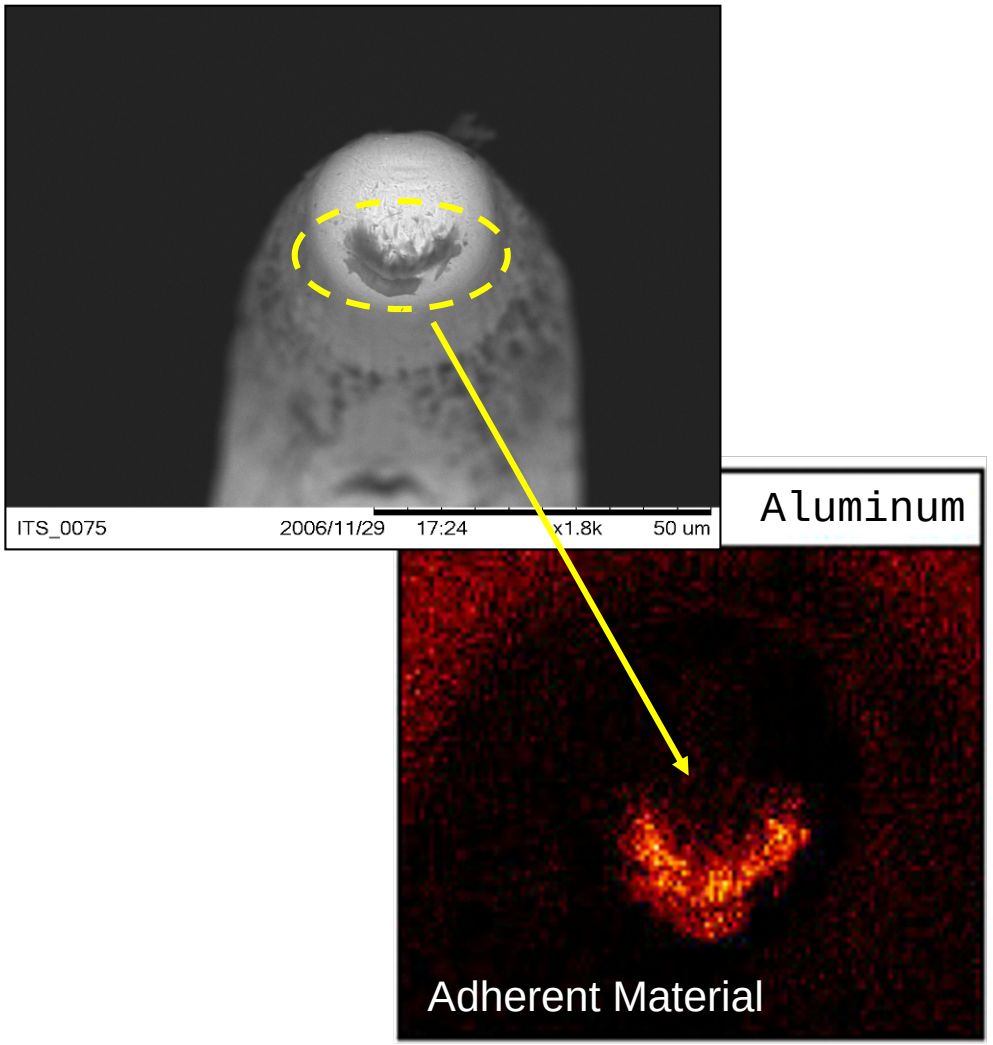
- Contact technologies have become advanced; however, the basics of wafer sort and package test have not really changed.
- ALL contactor technologies have a type of "tip" which makes physical contact with the various I/O's of the DUT.
- "Contact and slide" is CRITICAL to break surface oxide(s), but creates some level of localized plastic deformation
  - Physical damage, a.k.a., "probe mark" affects bondability, packaging, assembly, long term reliability, etc.
  - Amount of material displaced or transferred is a complex function of operational settings, metallic interaction, and tribological properties.

Adherent Materials Accumulation



Probe Mark 3D Profile of Displaced Pad Material

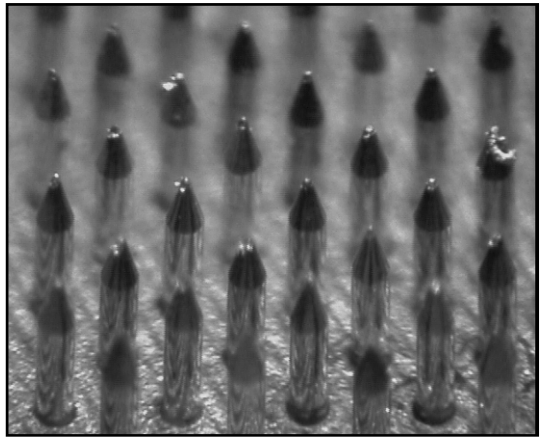




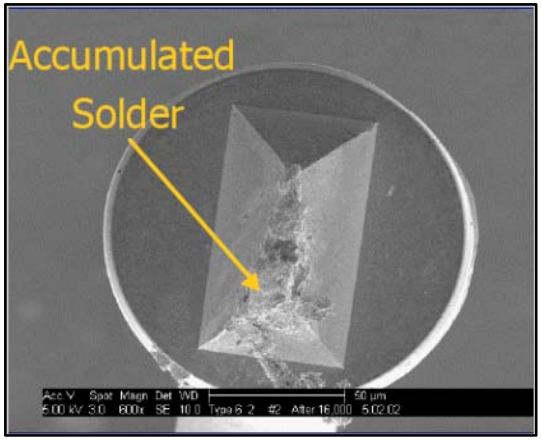
Broz et al., SW Test 2006

Wafer Sort / Test is a "Dirty Business"

- ALL types of probes generate, accumulate, and pick up debris to some extent

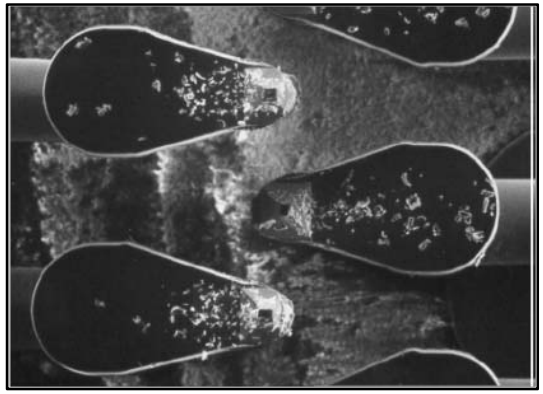


Courtesy of WWL

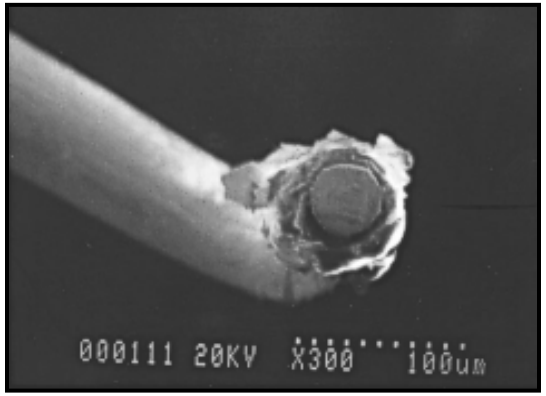


Martens, R., et al., SWTW-2002

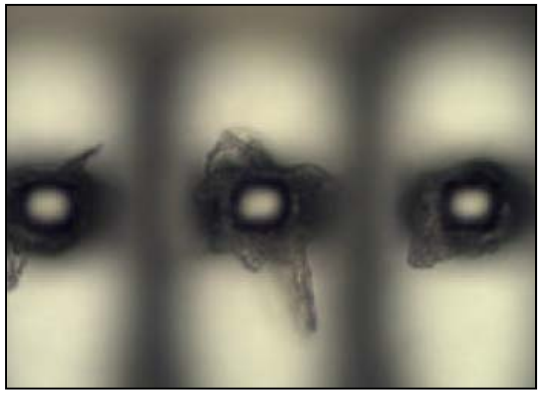
Forestal, J., et al., SWTW-2005



Brandemuehl, et al., SWTW-1999



International Test Solutions Technical Bulletin



Cascade MicroTech 121-710-APP-0805

Contamination Affects Contact Resistance (CRES)

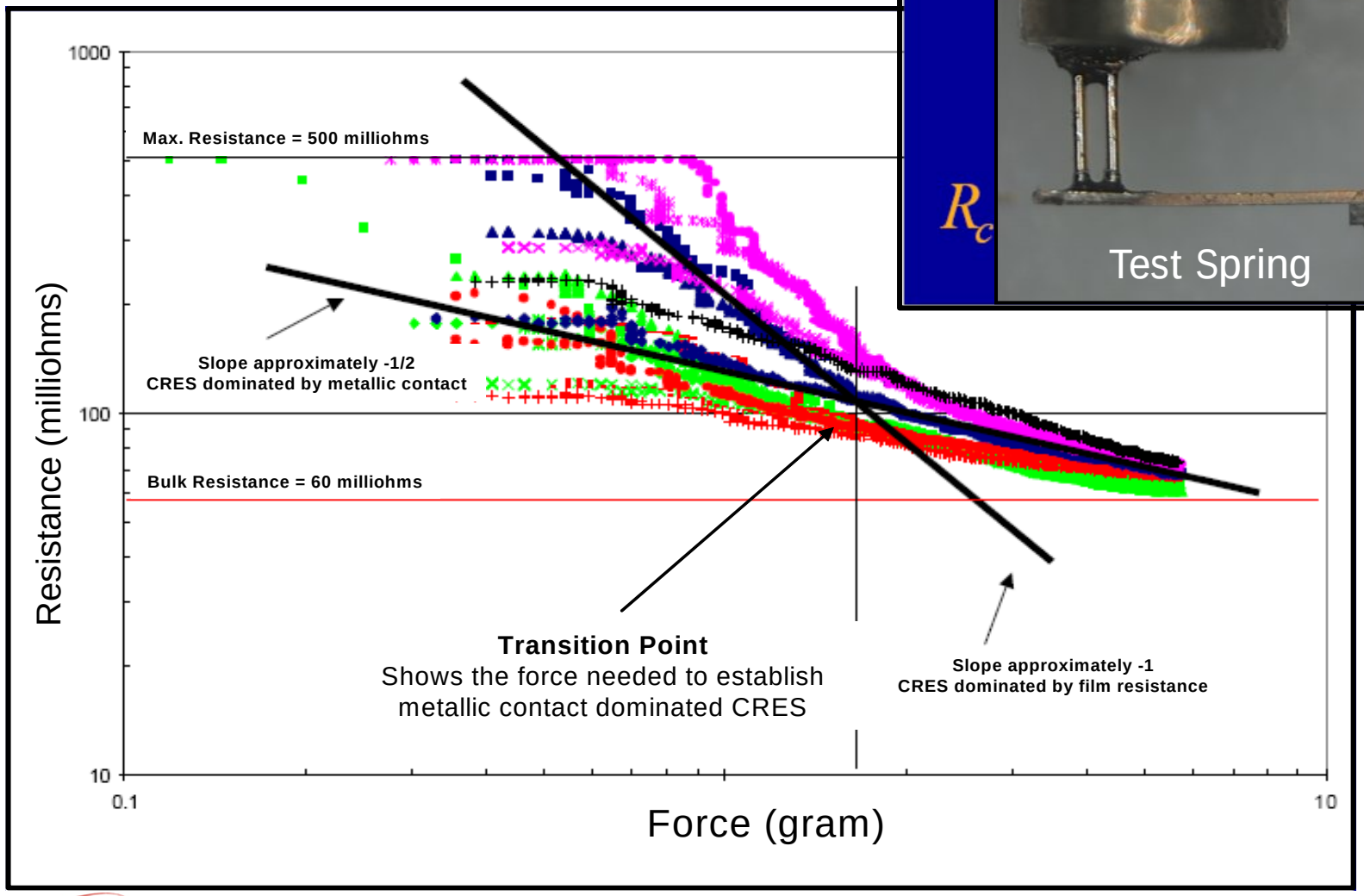
- Contact Resistance (CRES) a CRITICAL parameter in wafer sort
- CRES affected by two primary parameters
  - "Metal on Metal Contact" between a probe tip and the pads, bumps, pillars, etc.
  - Non-conductive film resistance that interferes with the "Metal on Metal Contact"

$$C_{RES} = \frac{(\rho_{probe} + \rho_{pad})}{4}\sqrt{\frac{\pi H}{P}} + \frac{\sigma_{film} H}{P}$$

METALLIC CONTACT **FILM RESISTANCE**

  - ρ_{pad}, ρ_{probe}, σ_{film} = resistivity values
  - H = hardness of the pads, bumps, pillars, etc.
  - P = contact pressure applied by probe
- Unstable CRES and first pass yield stability is affected film resistance (σ_{film}) due to build-up of non-conductive materials on the probe tip contact .

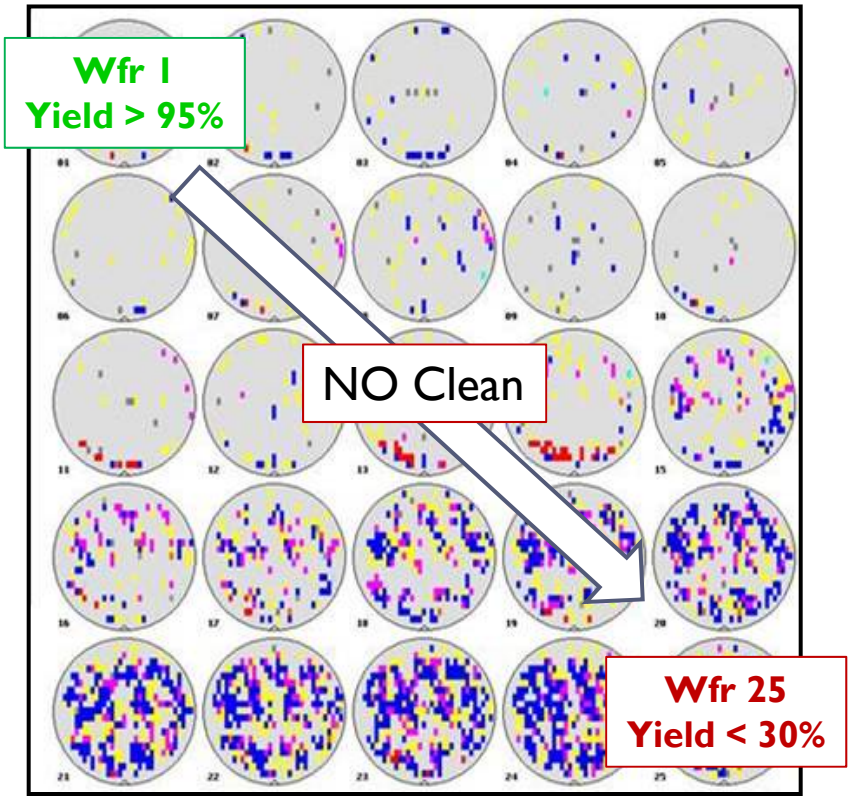
Film Resistance Dominates CRES



Martens, et al., SW Test 2002

Problem – Wafer Yield Fallout due to CRES

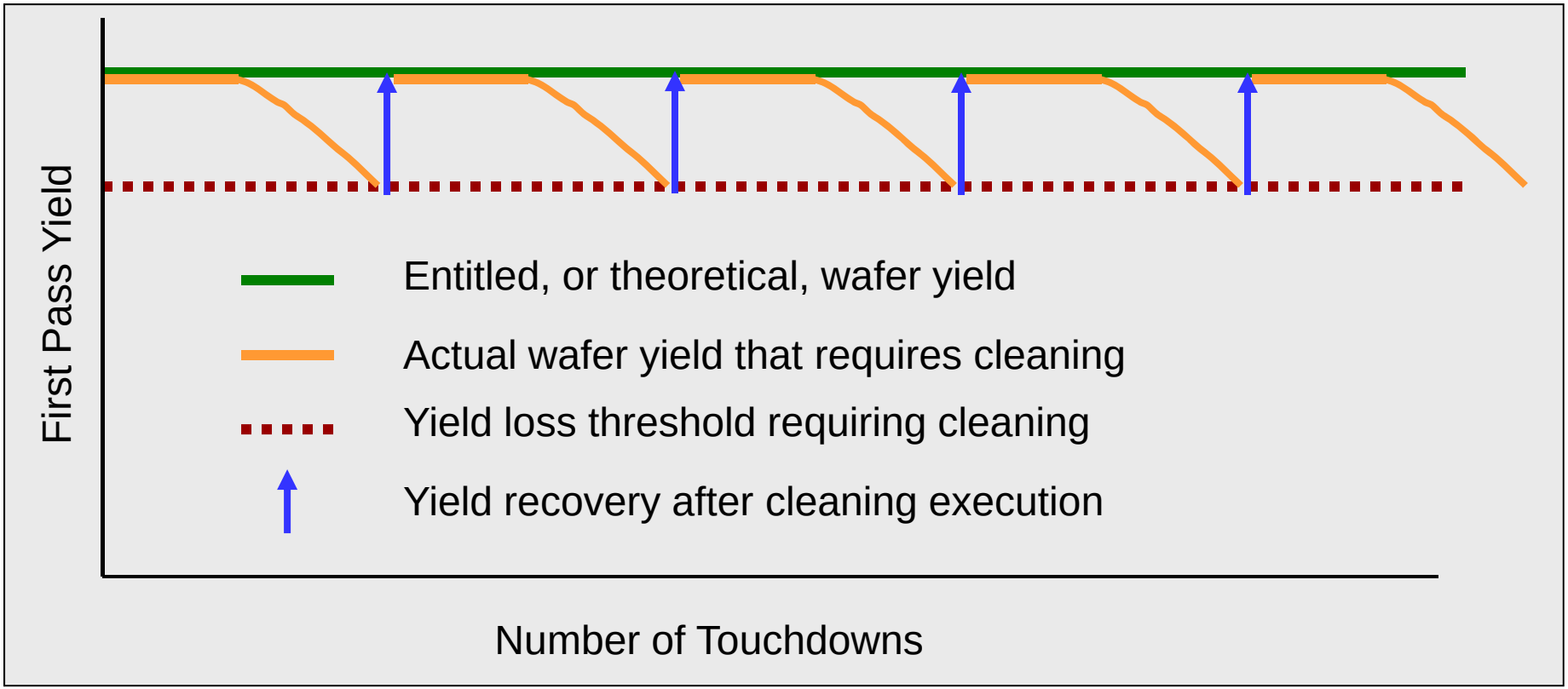
- Increased first pass yield fallout occurs with continuous probing.



- Re-sort is used to maintain production requirements and "recover" good devices that failed during first pass.
- Logic testing costs can be 15% (or greater) of device cost.
- Memory testing costs can be 18% (or greater) of device cost.

Probe Cleaning Is Needed for CRES Control

- Excessive cleaning reduces test throughput without yield benefits.
- Too little cleaning adversely affects test yields and affects uptime.

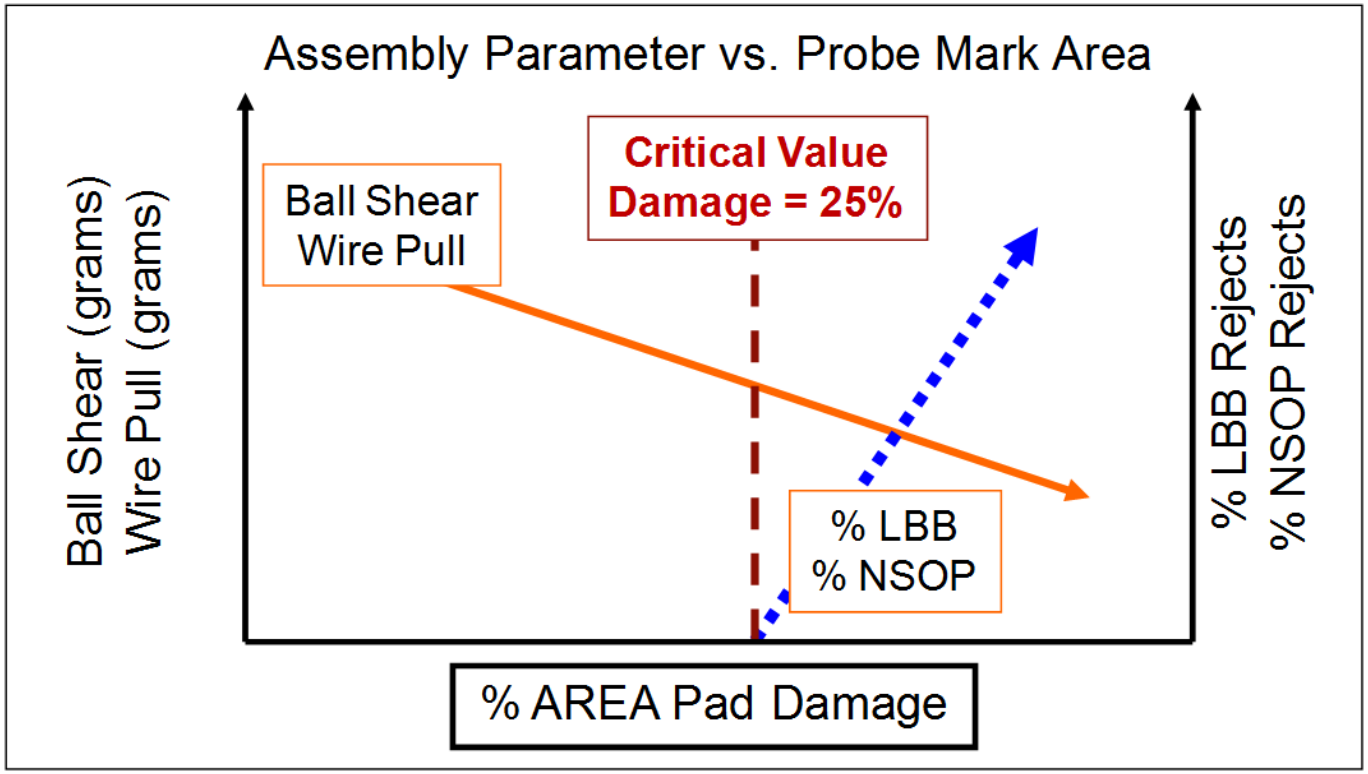


Effects of Aggressive Cleaning

- Controlled probing is critical for high dollar devices
  - Excess pad damage due to probe has been positively correlated to bondability and long term reliability defects
  - Excessively deep probe marks damage and crack low-k dielectrics, circuitry under bond pads, and aluminum caps
- Probe tip geometry changes from aggressive cleaning can have detrimental affects for the device
  - Increased tip diameter due to abrasive cleaning materials
    - Reduced contact stresses for CRES instability
    - Higher area damage with each probe event across the bondable area
  - Sharpened tip diameter due to shaping materials
    - Substantially increased contact pressure at the probe tip
    - Deeper probe marks and barrier metal cracking
    - Probe to pad alignment issues

Large Probe Marks Affect Assembly

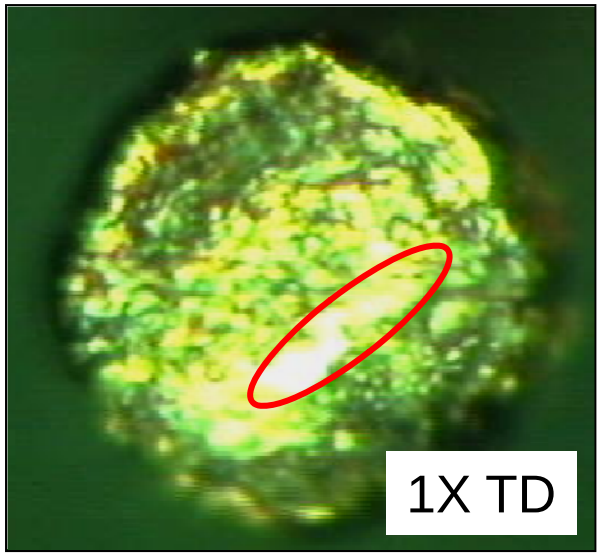
- High pad damage correlates to bondability issues.
  - Reduced ball shear strength and wire pull strength
  - Increased NSOP (no stick on pad) and LBB (lifted ball bond)

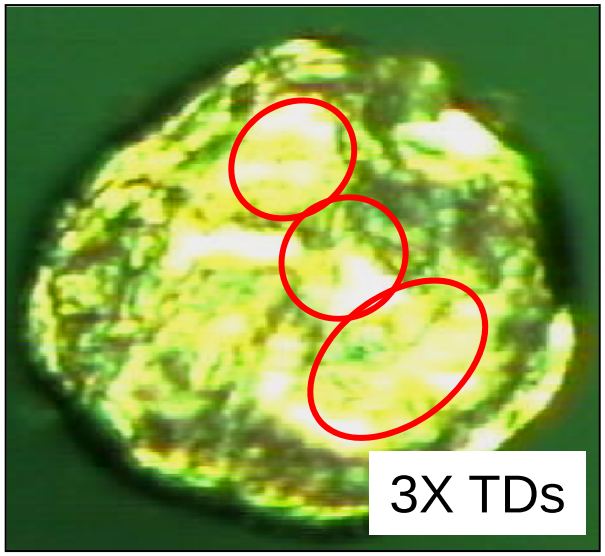


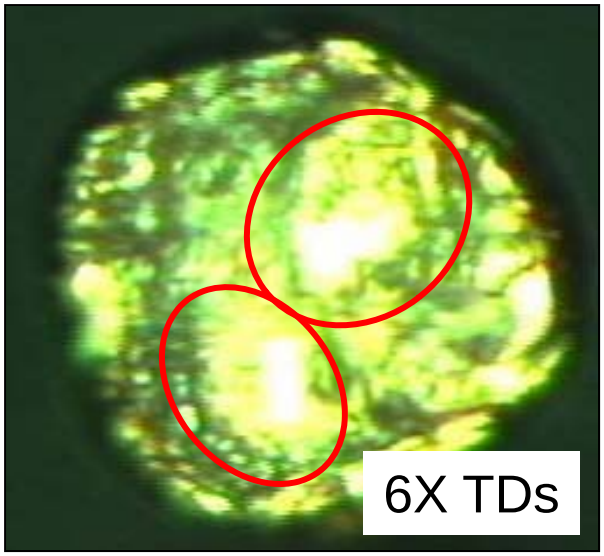
Reduced Inter-metallics Formation

- Insufficient aluminum-gold inter-metallics form at the deepest portion of the probe mark.

Regions of poor intermetallic formation and voids match the locations of the probe marks



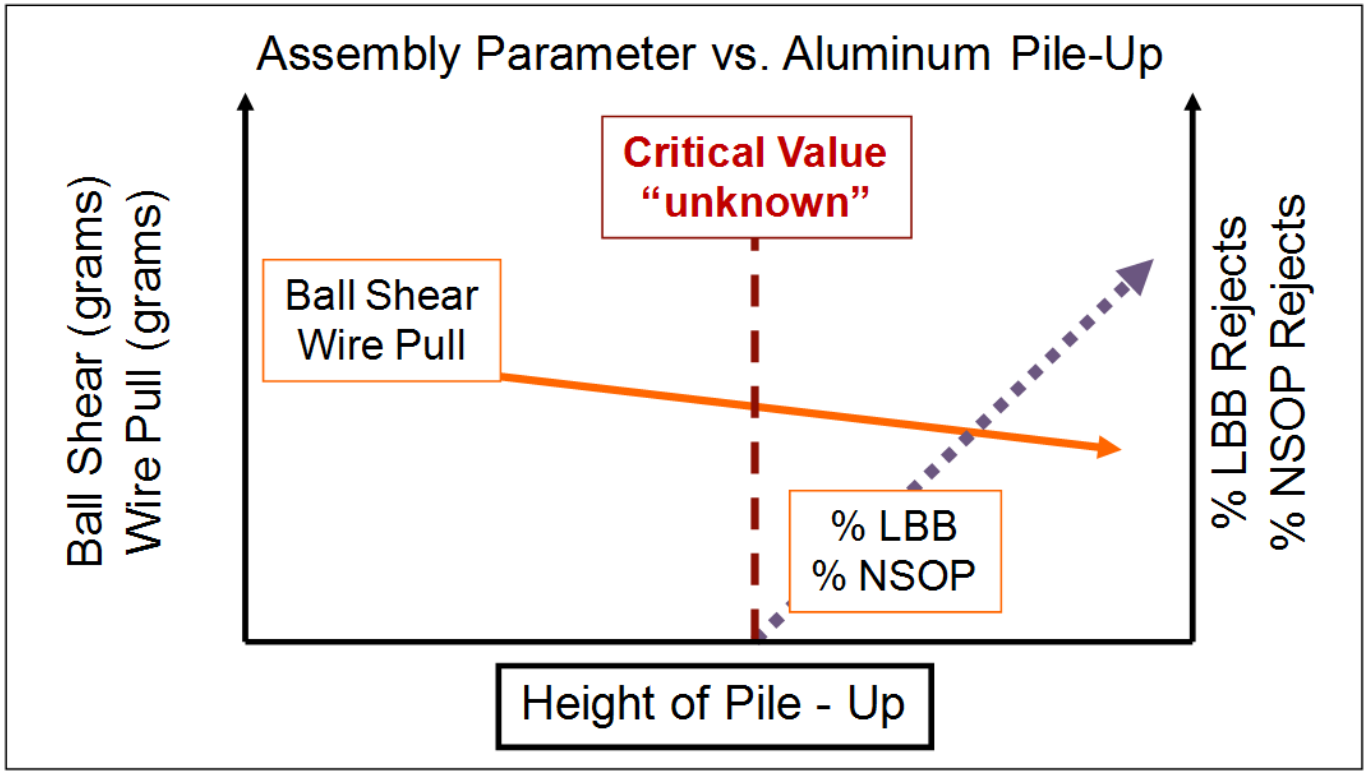




Hotchkiss and Broz, ECTC - 2000

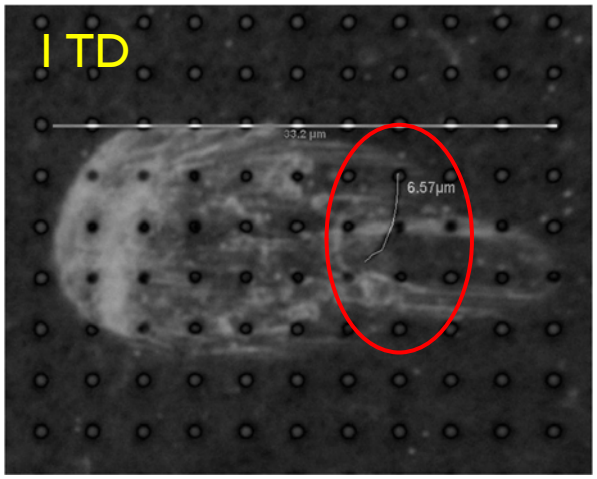
Deep Marks Affect Assembly

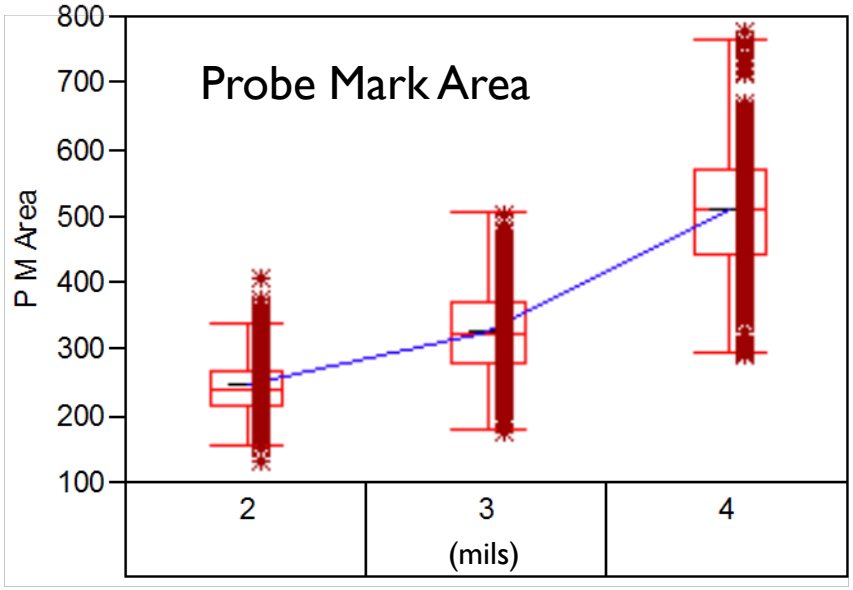
- Pad pile-up is correlated to bondability issues.
  - Reduced ball shear strength and wire pull strength
  - Increased NSOP (no stick on pad) and LBB (lifted ball bond)

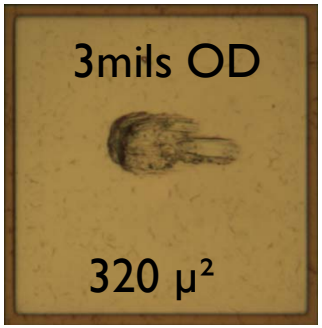


Pad Cracking Affects Reliability

- Harsh Wafer Probing
  - Probe mark size increases
  - Probe mark depth increases
  - % of pads cracked increases
  - Number and length of cracks increases

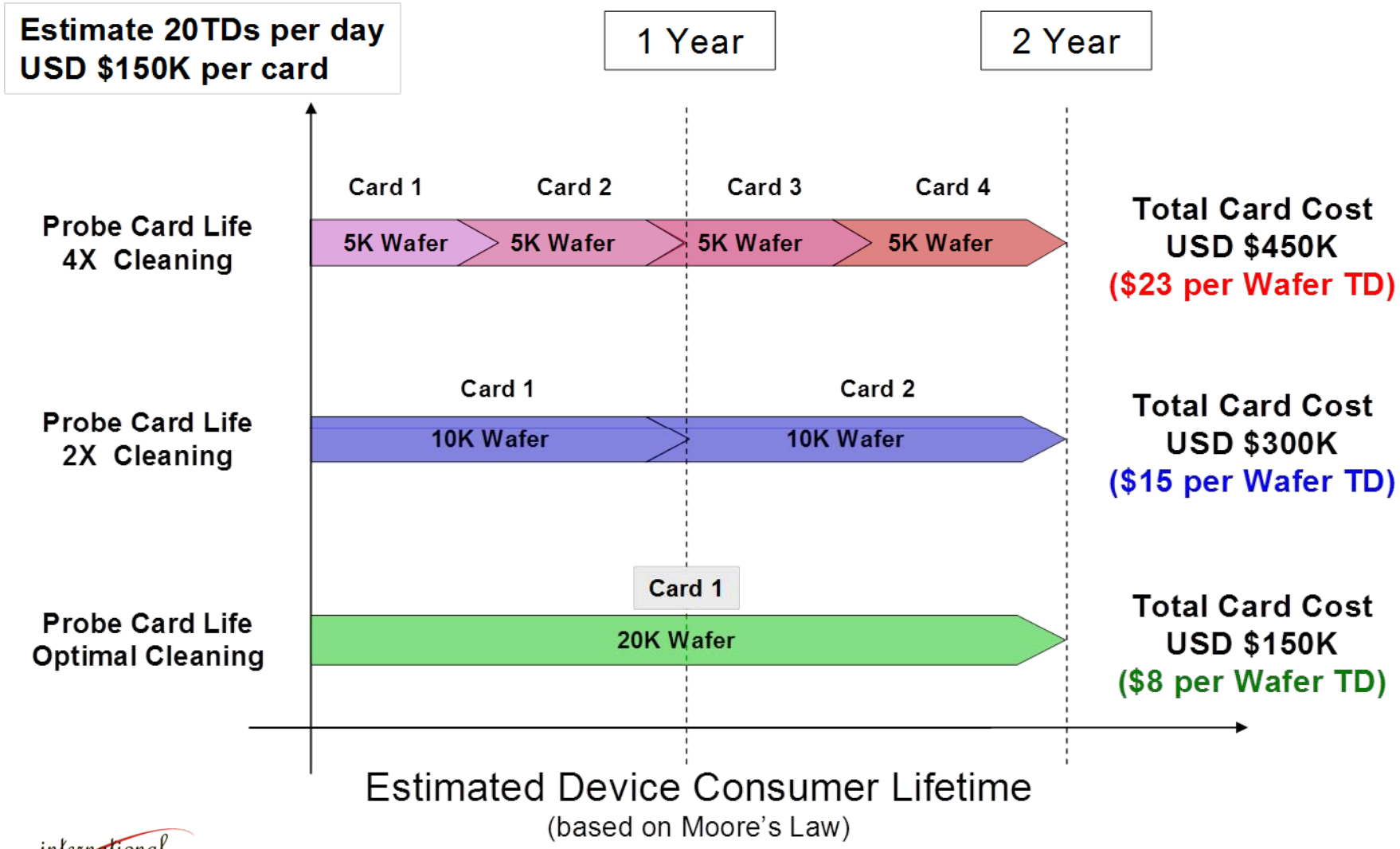




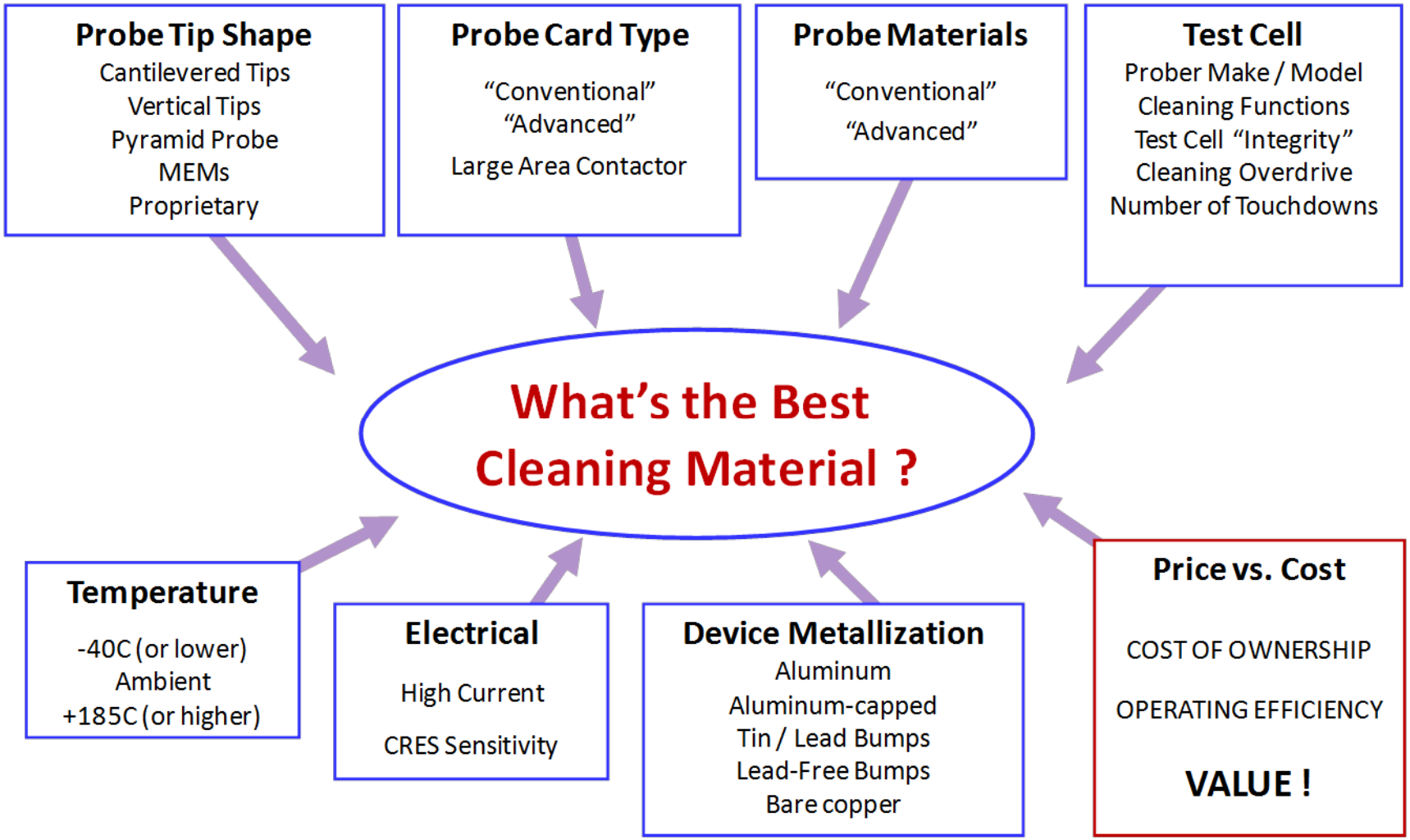


Hunter, et al., SW Test 2011

Poor Cleaning Has Commercial Implications



Challenge – Choosing a Cleaning Process



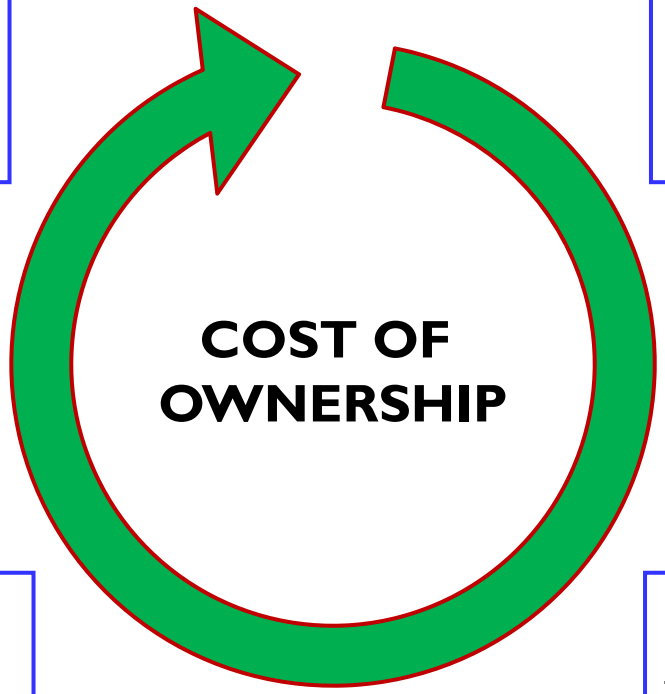
Cleaning Material and Process Considerations

Cleaning Material Selection

Retest / 2nd Pass Yield
Added Pad Damage
Added Test Time
Extra Equipment Utilization

Uptime
Ease of Prober Setup
Operator Assist / Intervention
Consistent Cleaning Efficiency

1st Pass Yield Fallout
CRES Related Issues
Additional Wafers
Additional Test Time



Capacity
Probe Wear out
Retest Requirements
Lead time for Spares / Extras
Test Time Requirements

Online Cleaning
CRES Sensitivity
Contamination / Debris
Pad and ILD Damage
Frequency / Duration

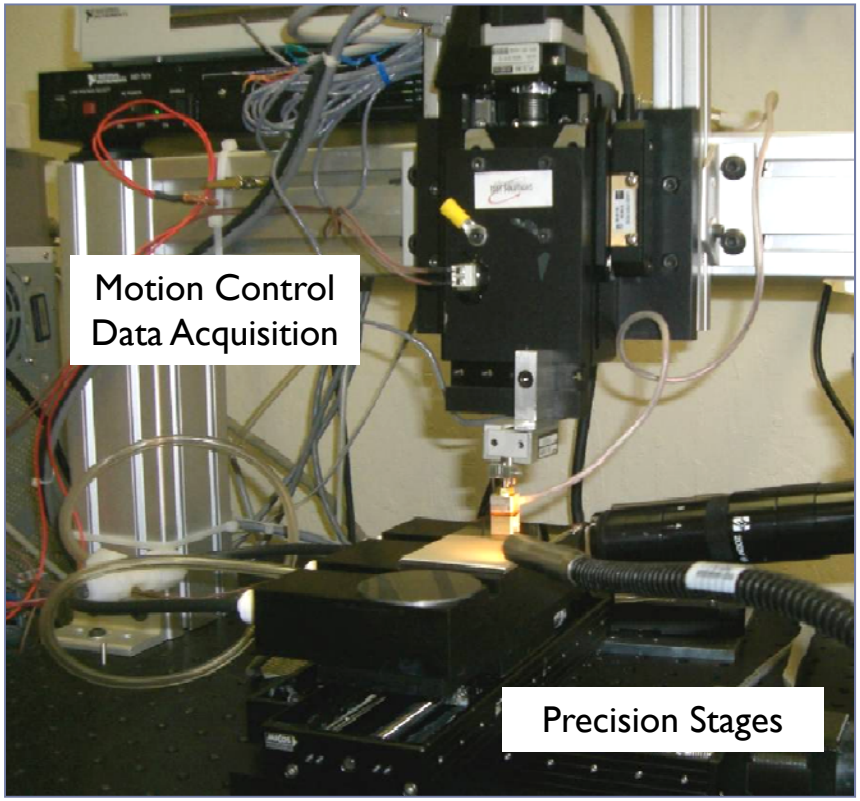
Offline Repair
Unscheduled Downtime
Tip shape / Tip Lifetime
Frequency / Duration
Off-site Repairs

Cleaning Process / Recipe Development

- Production sort floors are often manpower, materials, and financially limited for detailed characterization studies.
- Testing with "full-build" probe cards is expensive and often not feasible, particularly with large array probe cards.
- Assessing combinations of key probe process parameters requires substantial resource allocation.
- Gaining key insights with a representative test vehicles can be performed quickly under known and controlled conditions.
- Probe engineers need "a reasonable starting point" from which to develop on-line cleaning processes.

Test Under Controlled Test Conditions

- Probe characterization and cleaning performance testing.

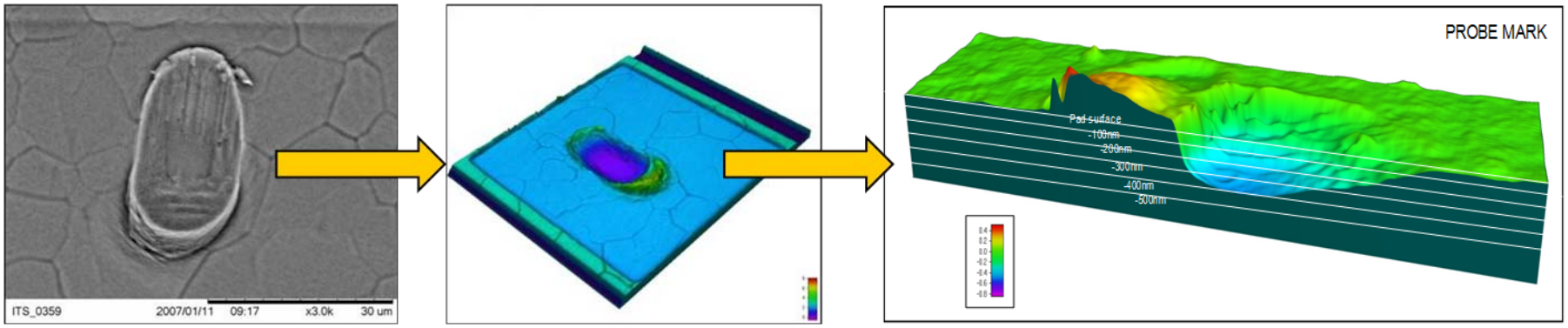


Martens, Allgaier, and Broz , SW Test 2008

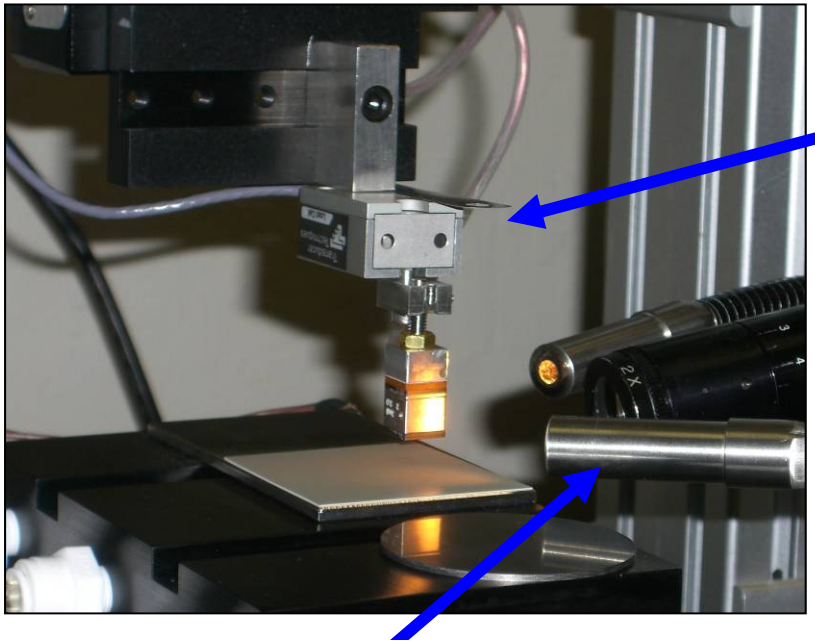
- Testing System Overview
  - Variable xyz speed and xyz-acceleration.
  - Low probe force measurements.
  - Synchronized load vs. overtravel vs. CRES data acquisition.
  - High resolution video imaging.
  - Current measurement with Keithley source-meter.
  - Micro-stepping to maximize touchdowns.
  - Multi-zone cleaning functions.

Use of Advanced Characterization Tools

- Hitachi SEM with EDS capabilities
  - Cleaning material, probe, device, solder ball, and bond pad imaging
  - Elemental surface analysis and assessment.
- Veeco 3D Confocal / Metallurgical Microscope Imaging System
  - Non-contact, high magnification surface characterization.
  - Cleaning material, probe tip, and probe mark inspection / quantification.

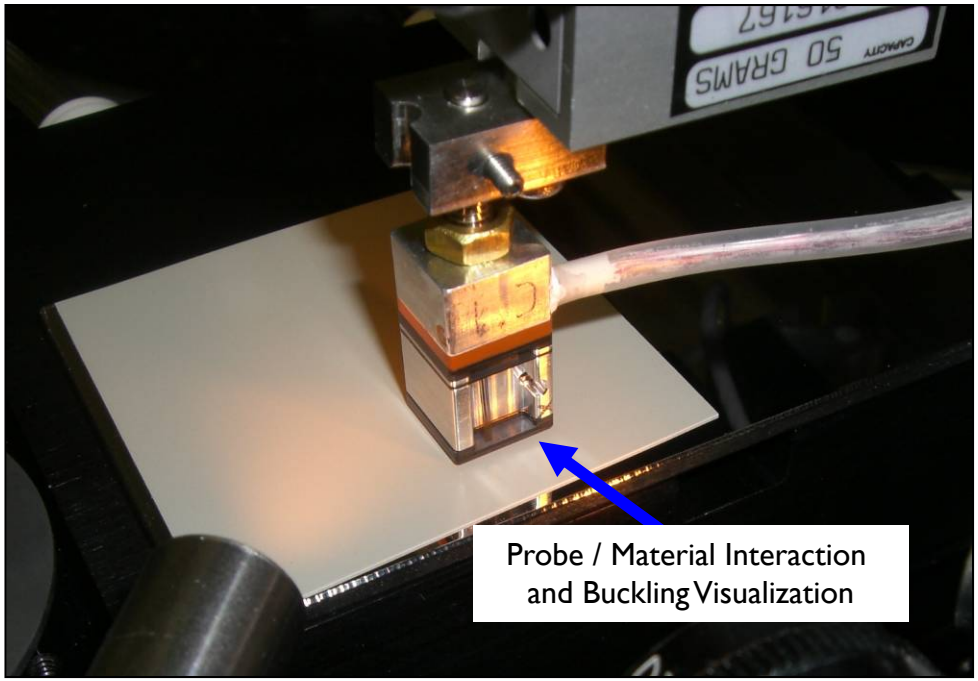


Test Vehicle and Cleaning Material



Test vehicle installed onto load cell

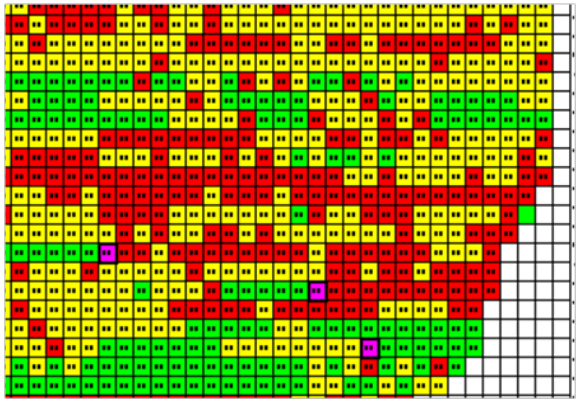
High resolution imaging system for video acquisition



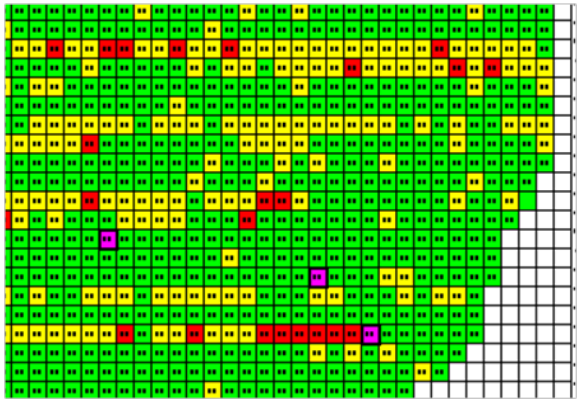
Martens, Allgaier, and Broz, SW Test 2008

Poor Cleaning Has Dramatic Impact

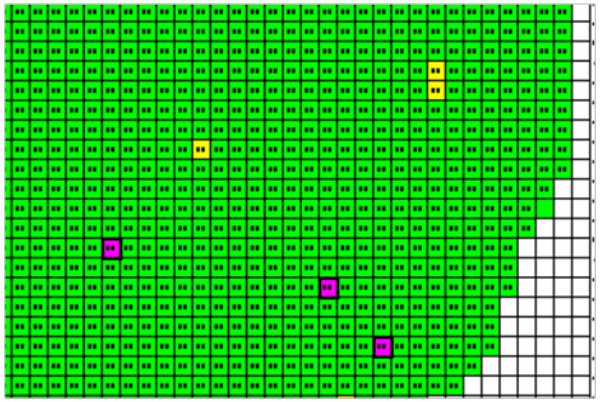
- Iterative assessments of multiple cleaning recipes stepping across multiple wafer sections was performed.
- Cumulative frequency distribution (CFD) for upper CRES limits was established based on process requirements.



Poor Clean Recipe
CRES values below Limit
CFD ~ 40% pass



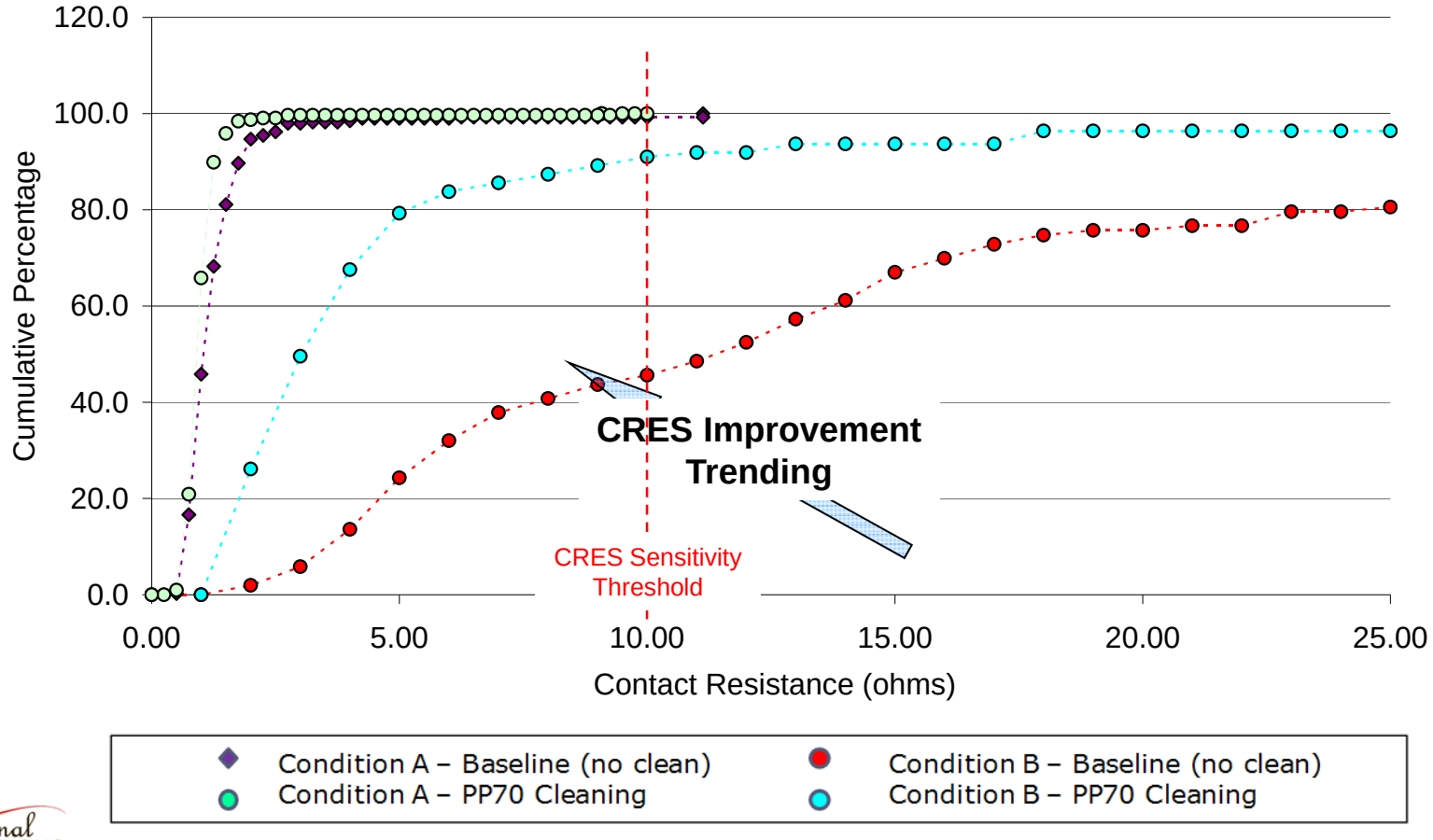
"Improved" Cleaning Recipe
CRES values below Limit
CFD ~ 80% pass



Optimal Clean Recipe
CRES values below Limit
CFD ~ 95%

CFD – Cleaning Process Assessment

- After several iterations, cleaning processes were developed for test conditions improved the stability of the CRES.



“Cleaning Process Science”

- “Standardized” test method combined with device bond-pad metal touchdowns demonstrated CRES performance.
- Iterative cleaning tests with probe test vehicles facilitate cleaning material performance assessment and effective cleaning recipe development under controlled conditions.
- On-line optimization and correlation with the test results must be performed at the customer-sites.

"Cleaning Process Economics"

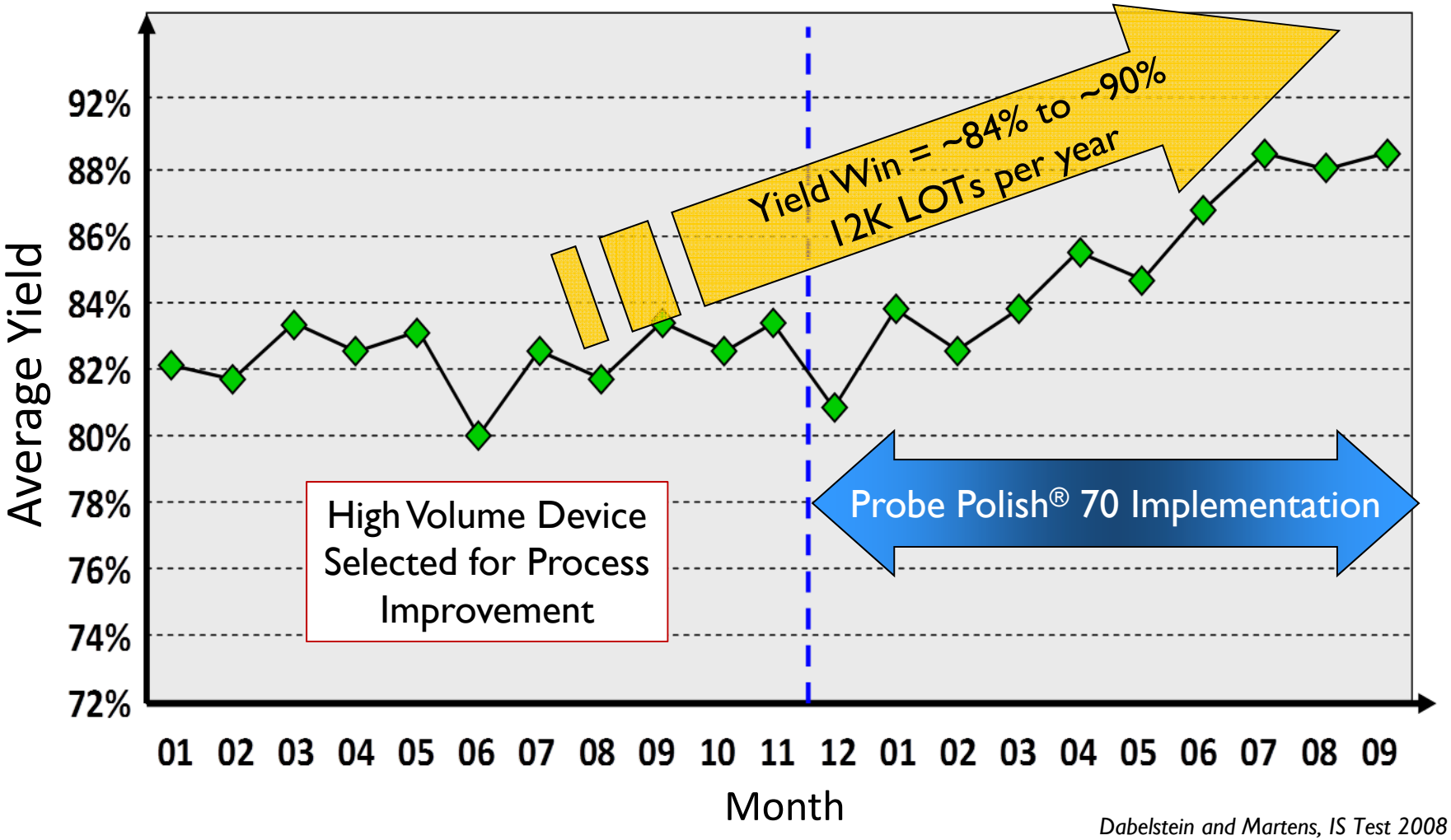
- For low volume devices and probe card technologies, iterative cleaning process developments are not economical.
- Determining cleaning requirement with "full-build" probe cards is often not feasible (or reasonable).
  - Single touch probes cards warrant special treatment
  - Assessing multiple probe-card technologies is expensive
  - Demanding electrical requirements may require several different cleaning procedures.
- Resources are limited for developing individual cleaning protocols for each probe-card technology and device.
  - Often a sound "best guess" from past experience is implemented.

Implementation

- NXP Semiconductor - Hamburg
  - High volume device sorted with large area array probe cards
  - Insufficient on-line cleaning to prevent bad performance
  - Frequent operator intervention and manual on-line cleaning
  - Off-line cleaning and repair time-consuming and expensive
  - Probe card repair costs were excessive
- Objectives for Sort Process Improvement
  - Implement Probe Polish® based on-line cleaning materials and practices
  - Optimize cleaning to maximize first pass yield and tool utilization
  - Reduce overall probe card repair costs and spares inventory

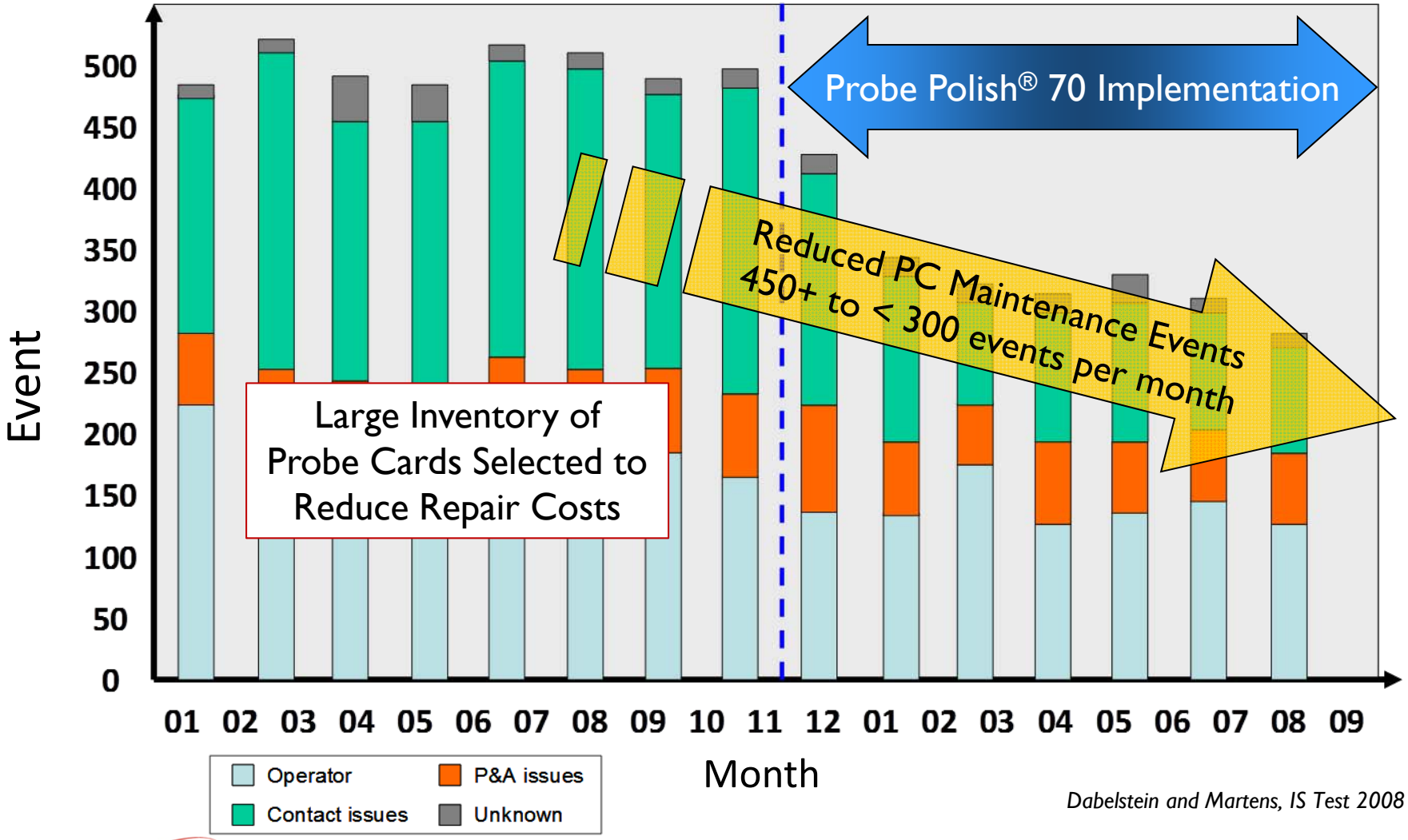
Dabelstein and Martens, IS Test 2008

Increased First Pass Yield



Dabelstein and Martens, IS Test 2008

Reduced Probe Card Repair Events



Dabelstein and Martens, IS Test 2008

Substantial COO Benefits

Probe Polish® 70 Implementation

- Wafer Sort Metric
  - higher yields attained
  - less retest needed
  - less maintenance
  - less tester downtime
  - less probe card downtime
  - longer probe card life

- Test-floor Benefits
  - 2% increase in 1st pass yield
  - Test capacity increase 1.2%
  - 30% reduction measured
  - 1 down event/day saved
  - 5 probe card repairs/day saved
  - 50% saving for probe cards

Dabelstein and Martens, IS Test 2008

Summary

- For high volume devices, cleaning processes are often optimized to the specific test environment and requirements.
- End-Users with multiple probe-card technologies and demanding device requirements may have several different cleaning recipes.
- Developing individual cleaning procedures for specific probe-cards and new devices requires extra resource allocation.
- ITS has developed a comprehensive suite of tools, methodologies, and infrastructure to provide a critical insights for wafer level test.
- Implementing an off-line approach and working with sort-floor engineers can significantly reduce the amount of resources required to develop key aspects of sort processes.

Acknowledgments

- ITS WW Applications Team and Sr. Management
- ITS Technical Partners
  - FeinMetall
  - NXP Semiconductor
  - Others that must remain "nameless"
- IEEE SW Test Workshop Archives
  - http://www.swtest.org
  - Abstract submission for IEEE SW Test 2012 is open !

Thanks for Attending !

Questions ???