



R&D Circuits, Inc.

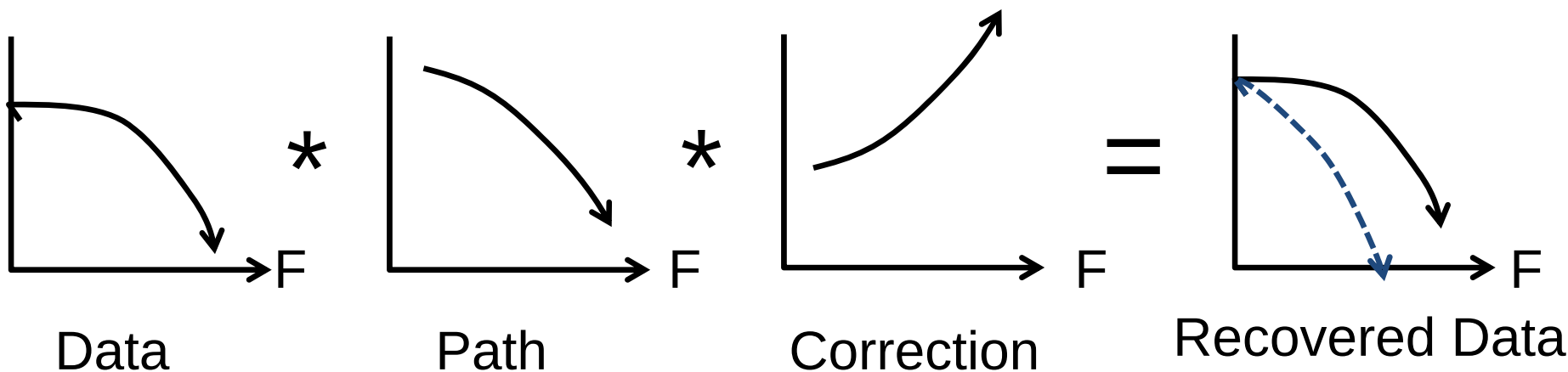
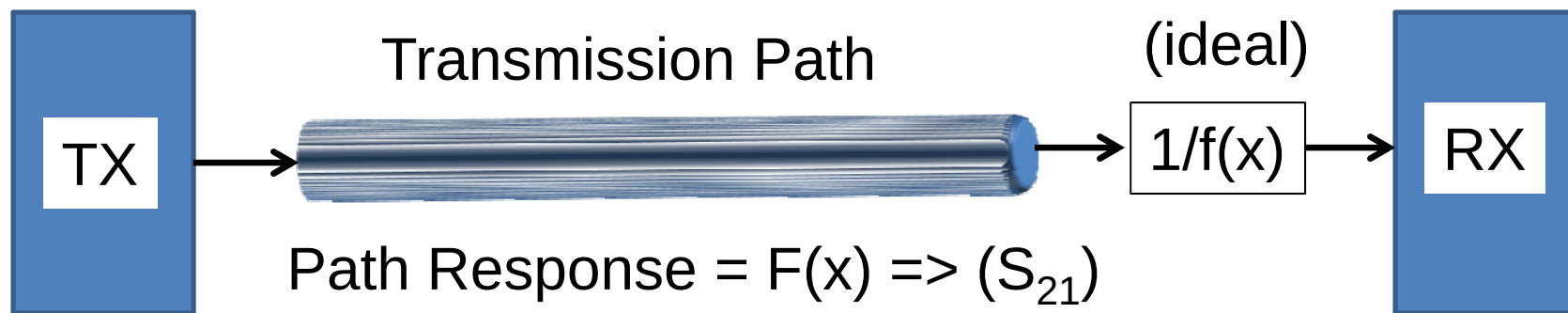
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Purpose and Outline

This presentation discusses on-going issues relative to the development of repeatable and effective test implementations for 25GB/s devices.

- Review of Correction Methods
- Primary Issues of Concern
- Via Structure
- Loadboard Consistency / Repeatability
- Power Delivery
- Concluding Comments

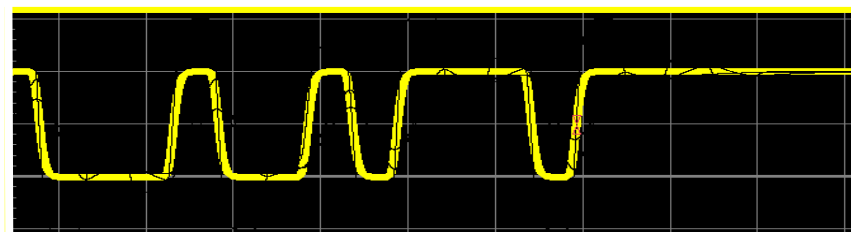
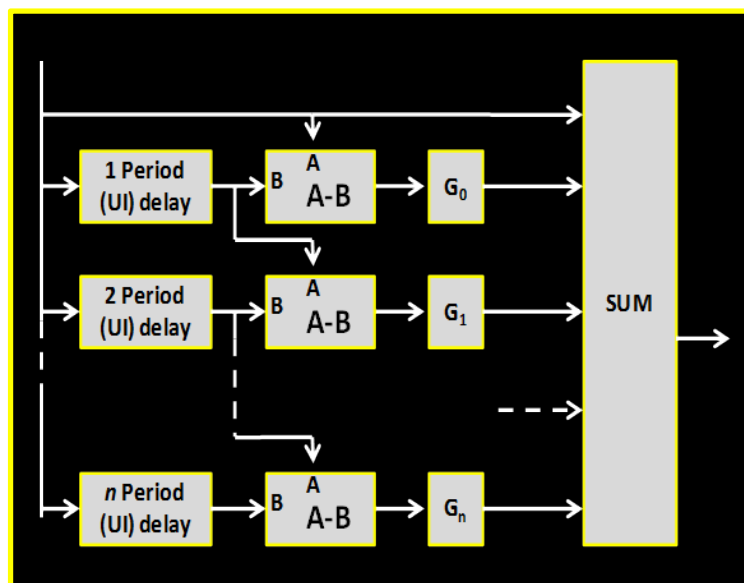
Review of Correction



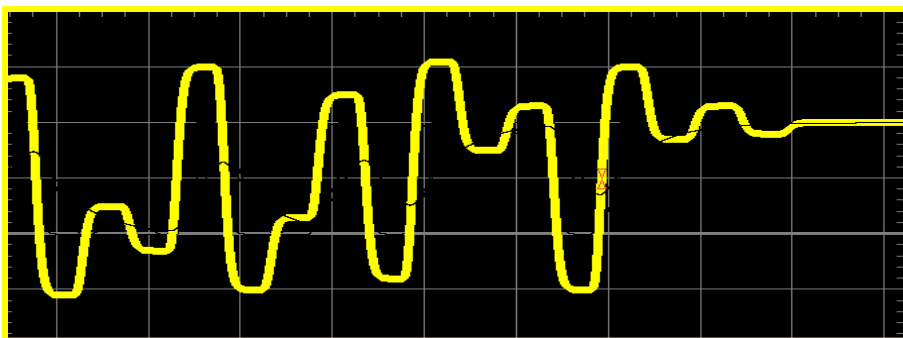
Review of Correction

In implementation, $1/S_{21}$ implementation is not practical in a broad sense. Therefore an “FIR” filter is used with a sampling rate based on the data period (under-sampling).

Pre-emphasis FIR



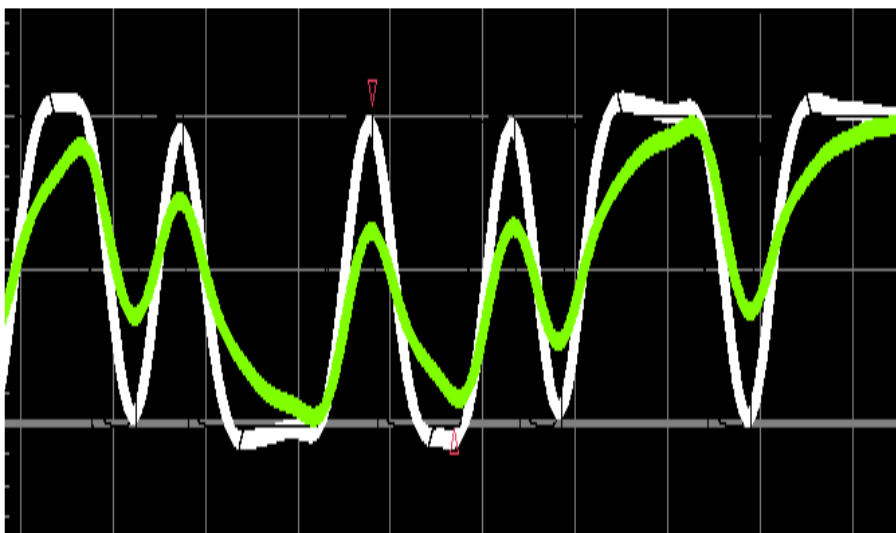
Pattern After Correction



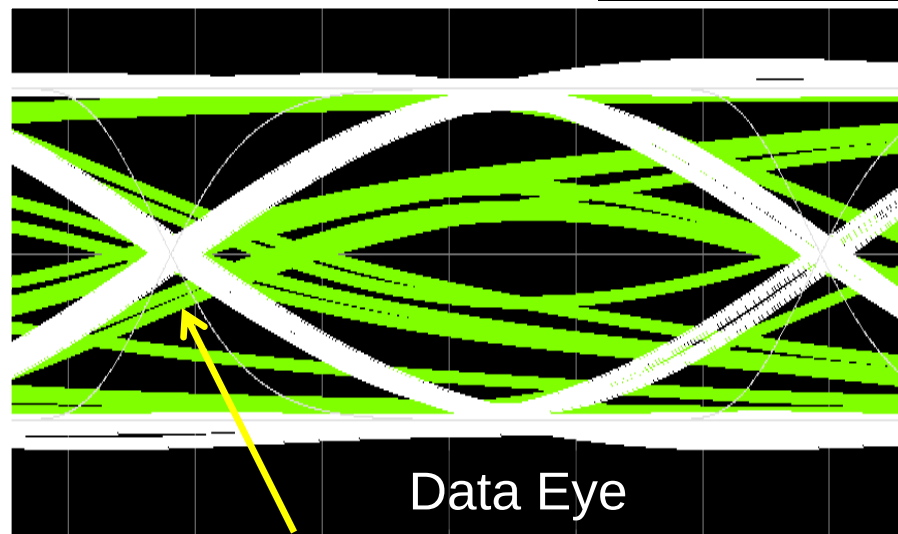
Review of Correction



Corrected



Uncorrected

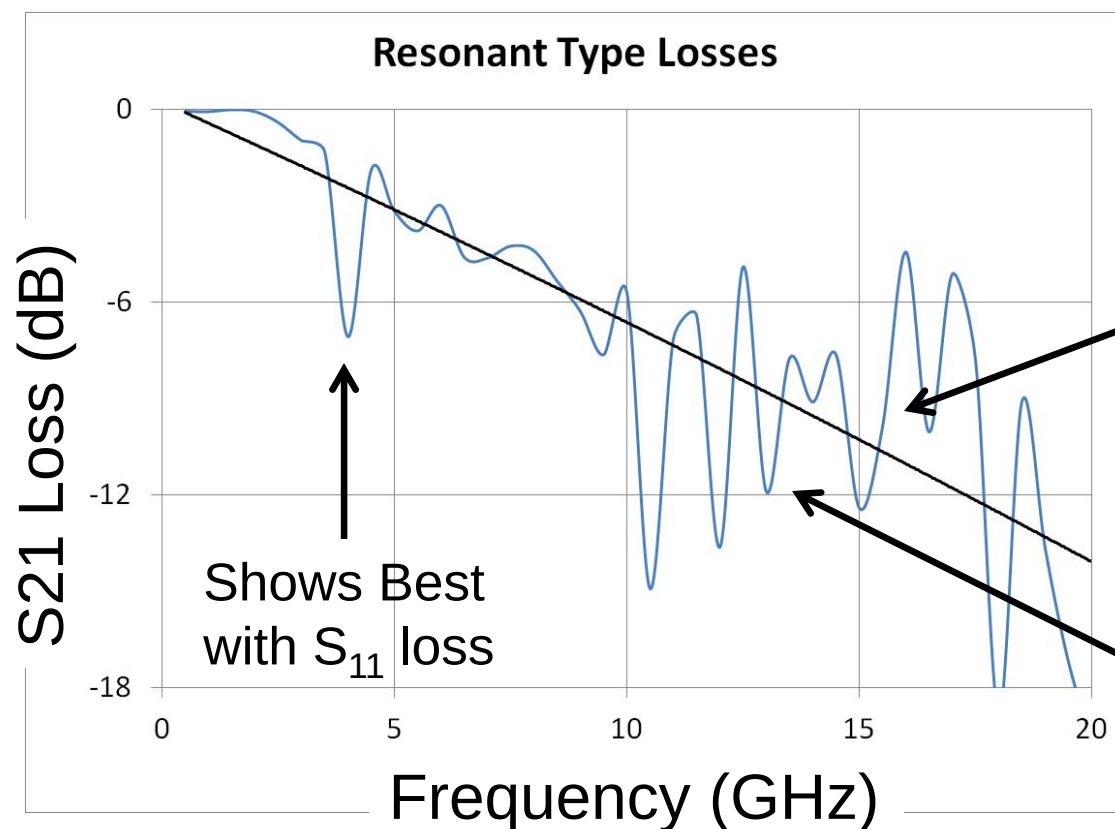


“Block correction” and other methods correct for other jitter sources (i.e. random jitter, uncorrelated jitter, etc.)

-- But correction has its limitations --

Primary Issues

RESONANCE POINTS



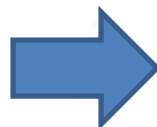
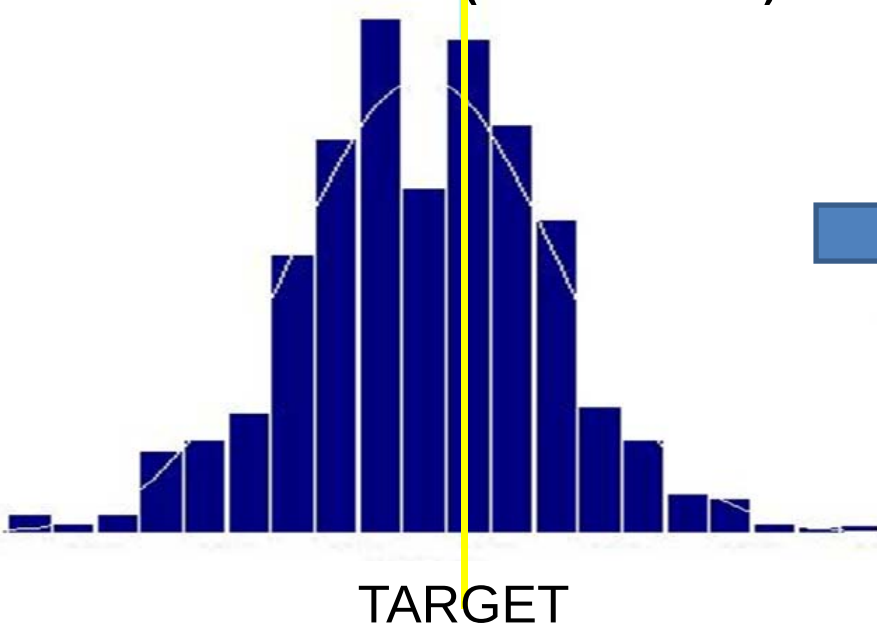
Under-sampling FIR
tap structures must
assume monotonic
loss

Vias and sockets
cause resonant
points

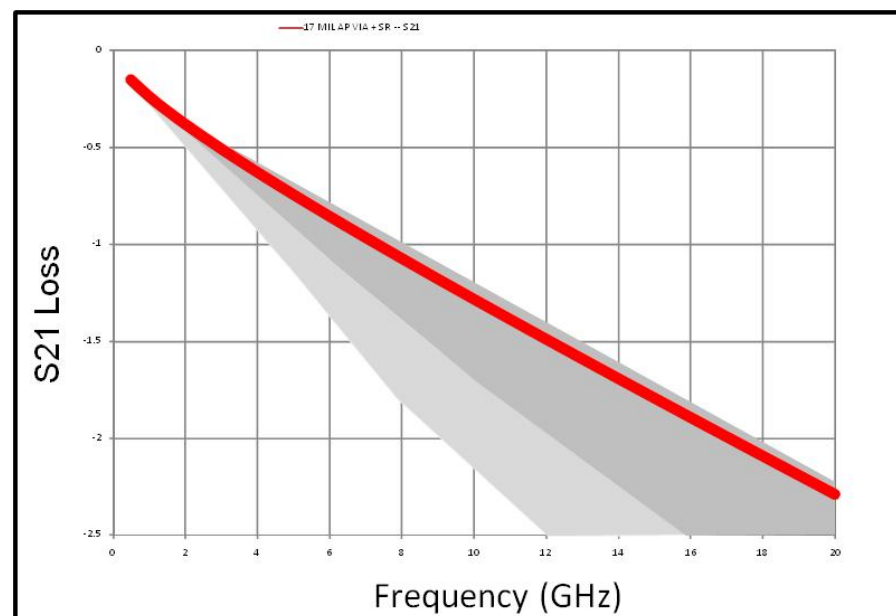
Primary Issues

Site to Site Measurement Repeatability

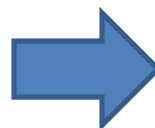
High Performance Core
Distribution (1300 Cores)



LOSS REPEATABILITY



$\pm 10\%$ Thickness variation

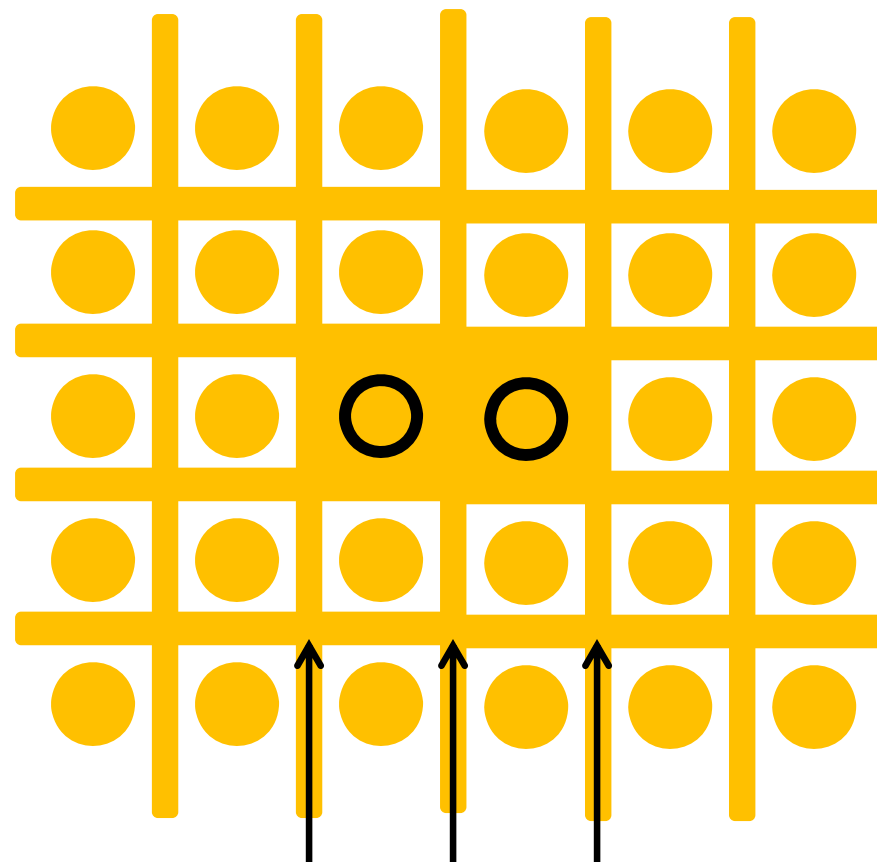
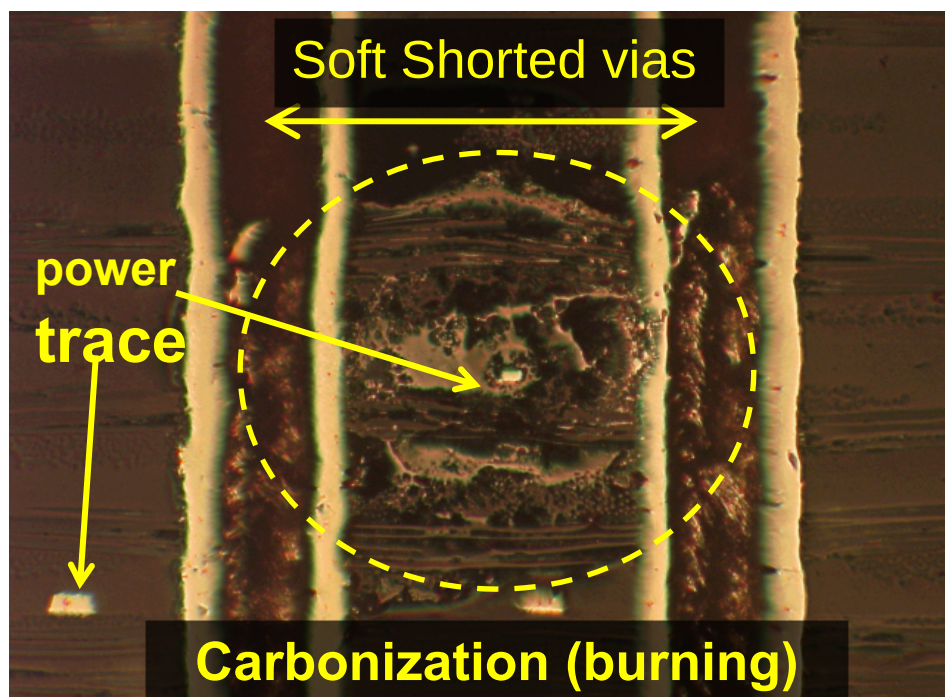


$\pm 6\%$ Impedance Variation



Primary Issues

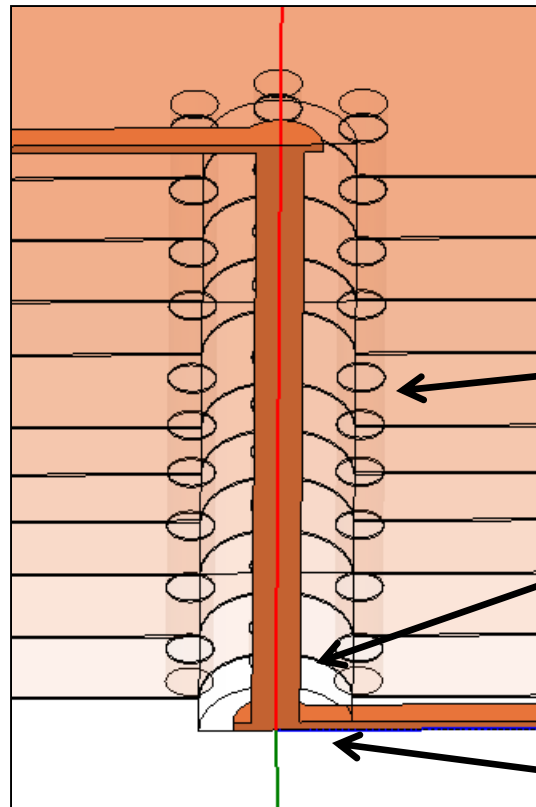
Power



>300ma in a web for 0.4mm pitch



Via Structures



Classic Via Impedance Depends on:

↕ Ground (Pwr) Plane Spacing

← Surrounding Ground Vias

← Via Anti-pad

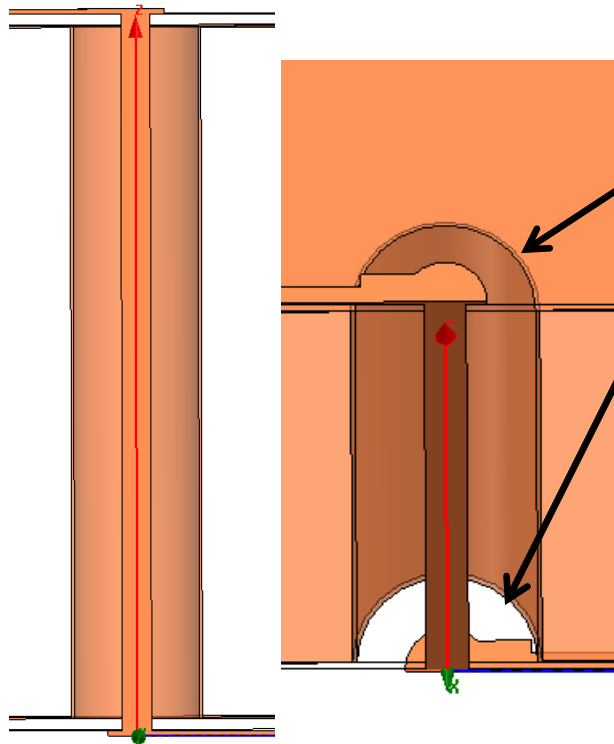
← Right Angle Bend:
Entry Pad + Trace Width + Anti-pad

End Result: frequency dependent structure



Via Structures

Coaxial Via: very consistent impedance

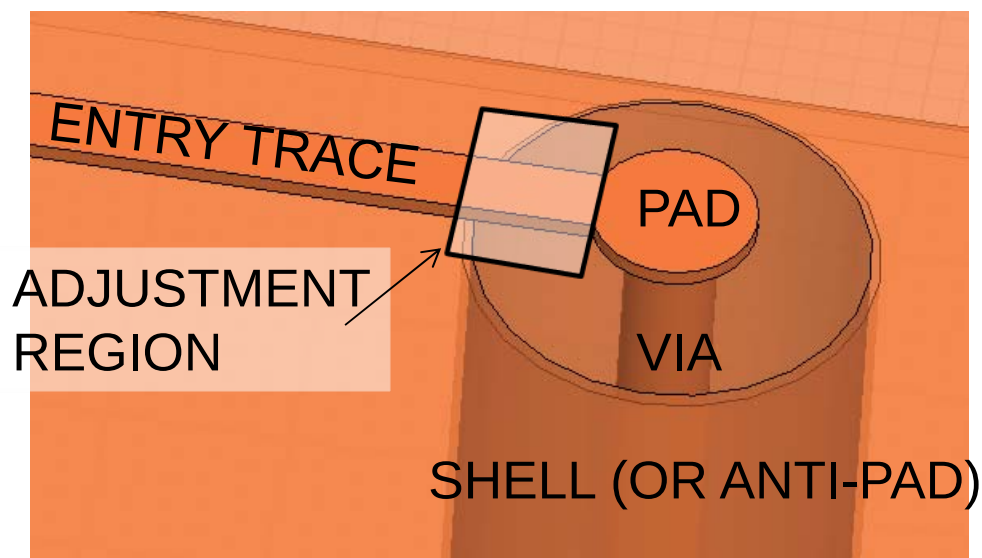


Only Impedance Dependency is the
Right Angle Bend:
Entry Pad + Trace Width + Anti-pad

Other Benefits:

- *Higher density* than surrounded gnd vias
- Lower Crosstalk

Via Structures



GENERAL GUIDELINES:

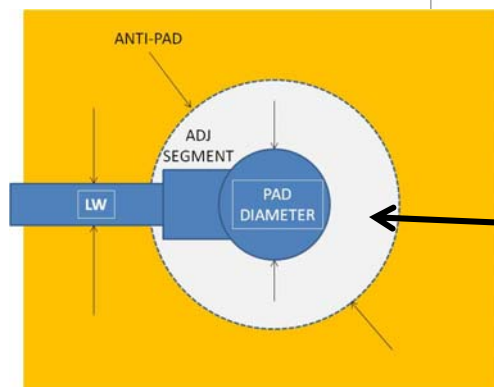
MICROSTRIP / NARROW TRACE RELATIVE TO PAD: ADJUSTMENT $< Z_0$

MICROSTRIP / WIDE TRACE RELATIVE TO PAD: ADJUSTMENT $> Z_0$

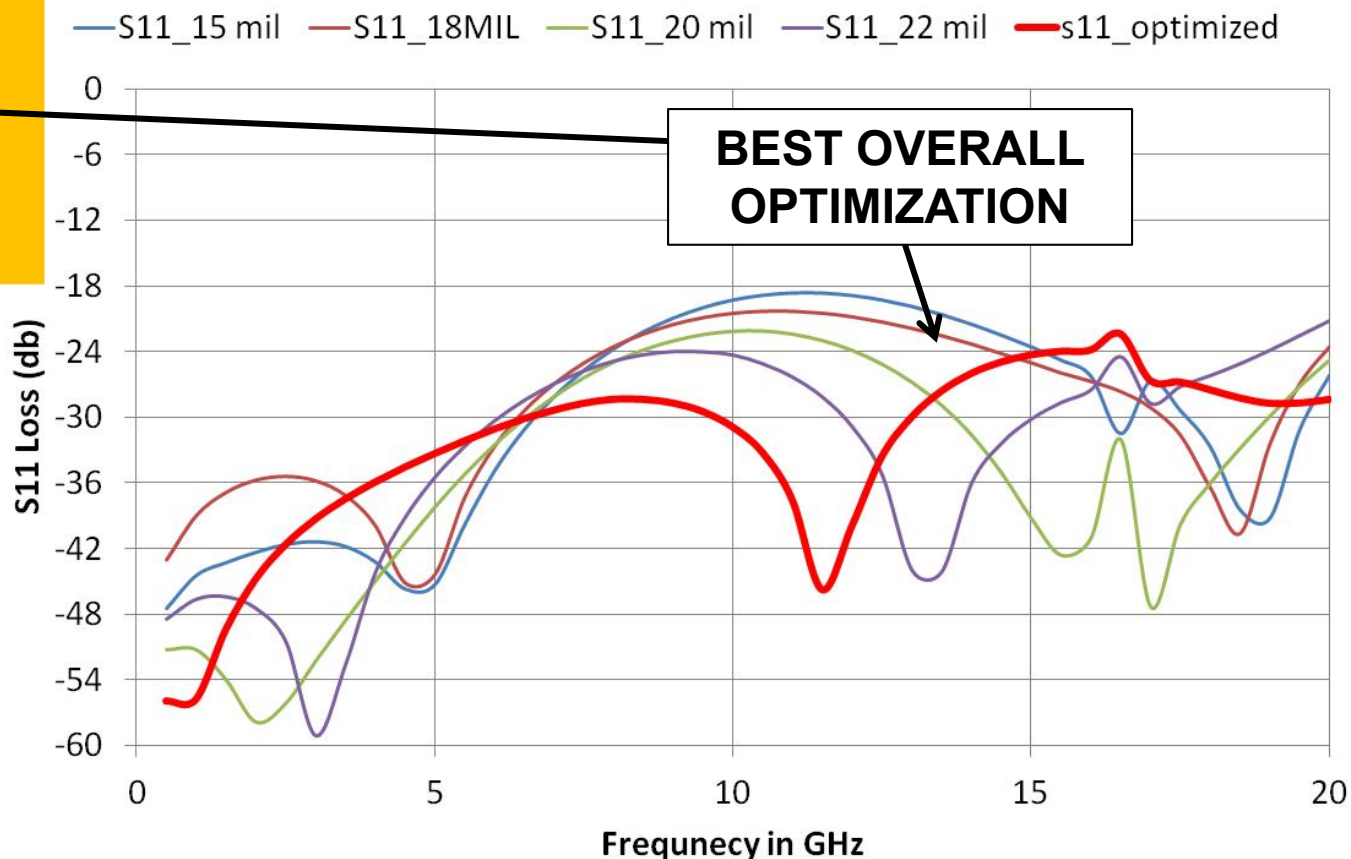
STRIPLINE / WITH STUB: ADJUSTMENT $> Z_0$



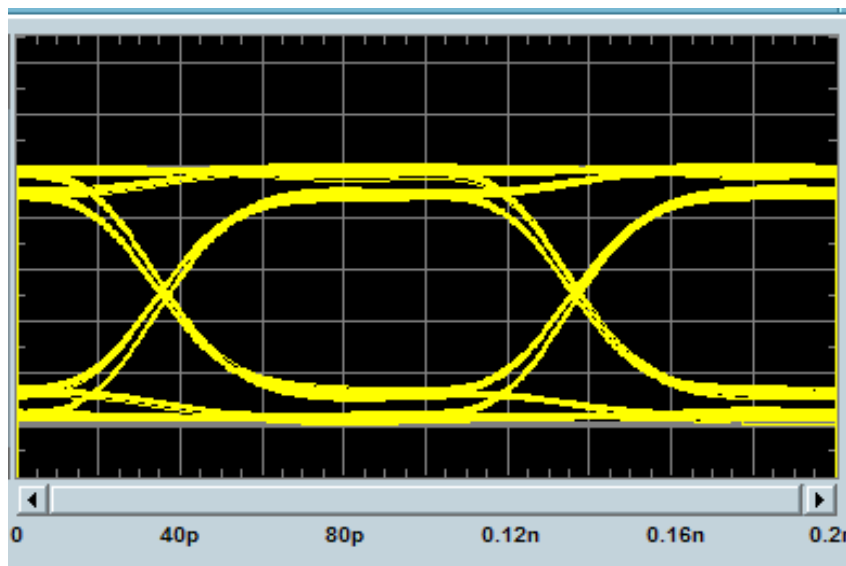
Via Structures



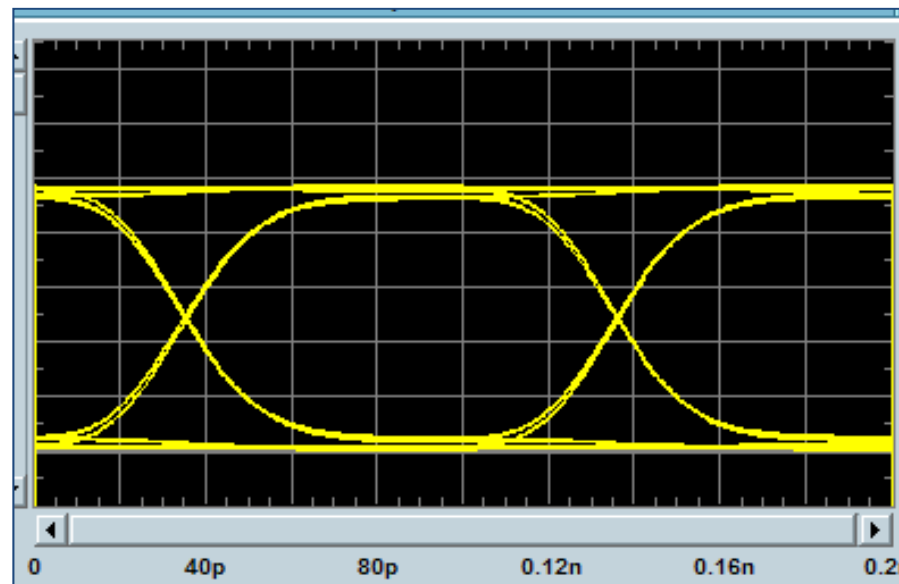
Comparison of the Effect of Via Pad Size on S11 Loss
(7.5 mil microstrip entry 10 mil core - 42.9 mil shell coaxial via)



Via Structures



Optimized Anti-pad Adjusted,
Surrounded by Ground Via
10GB/s



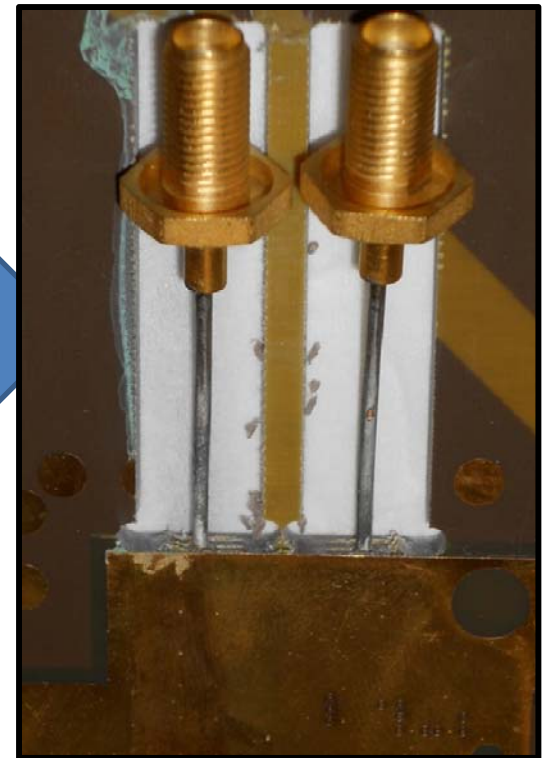
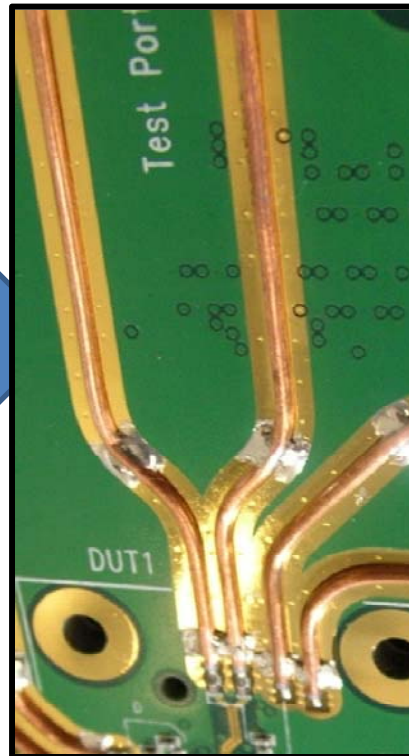
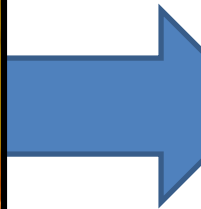
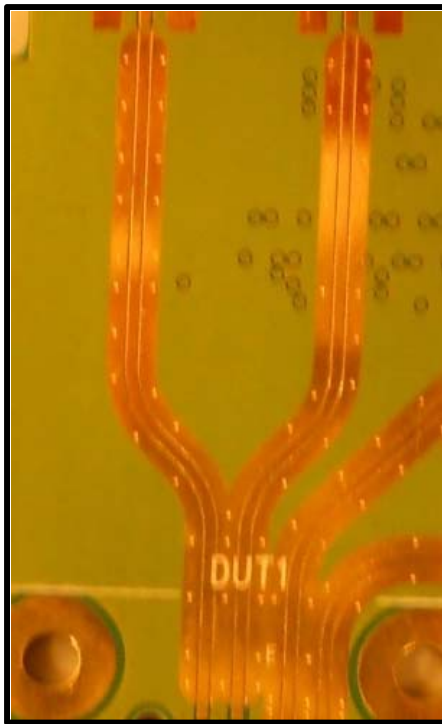
Coaxial Via
10/GB/s

Board Repeatability

- Greatest issues are in Material Thickness
 - General Guidelines
 - ✓ Core to Core Variation $\pm 10\%$ $\gg$ $\pm 6\%$ Impedance Variation
 - ✓ Within Core Variation $\pm 5\%$ $\gg$ $\pm 3\%$ Impedance Variation
- “Prepreg” material variability is much worse than “Cores” (= use of offset striplines)
- Traces with consistent Surrounding Copper Etch with lowest variability (e.g. co-planar wave-guide or like structures)

Board Repeatability

Emerging PC Board Methods

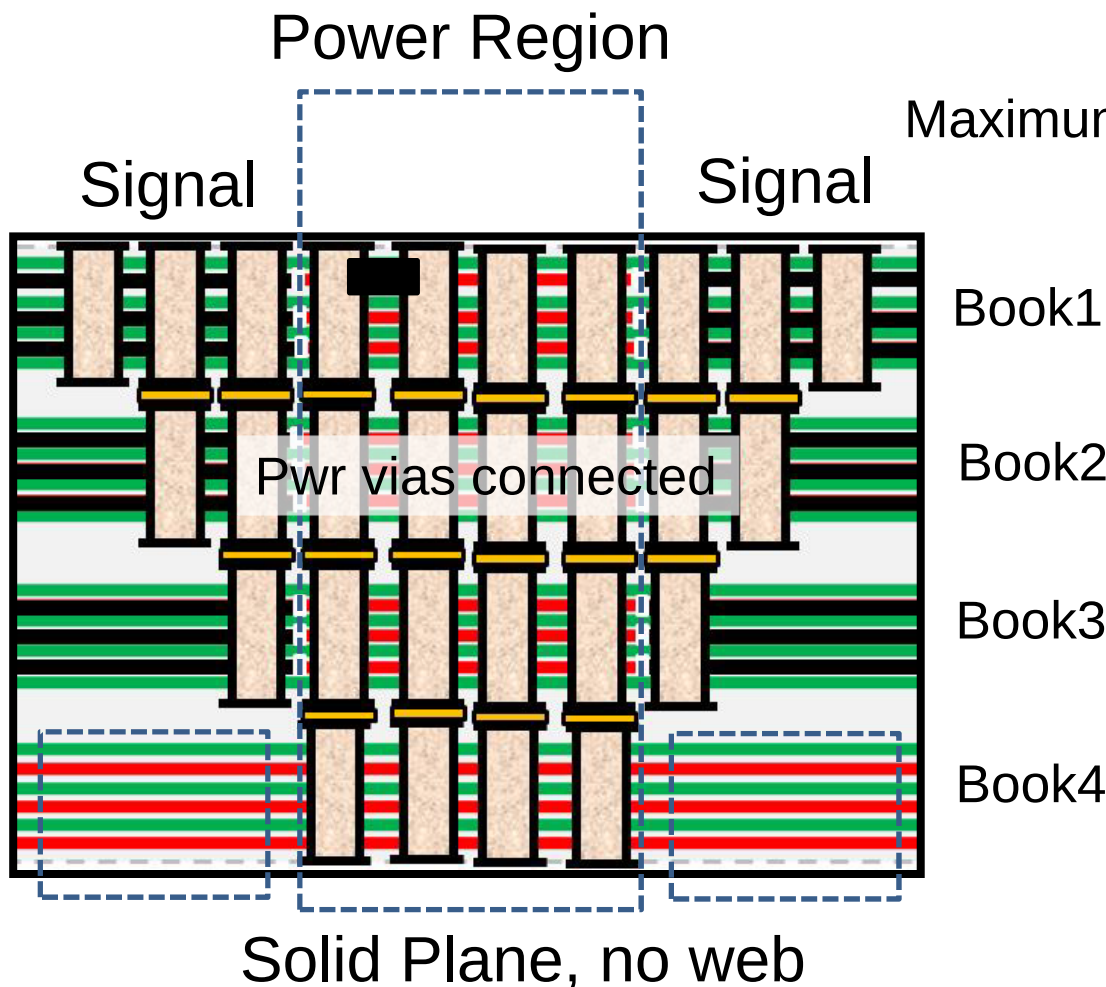


Power Delivery

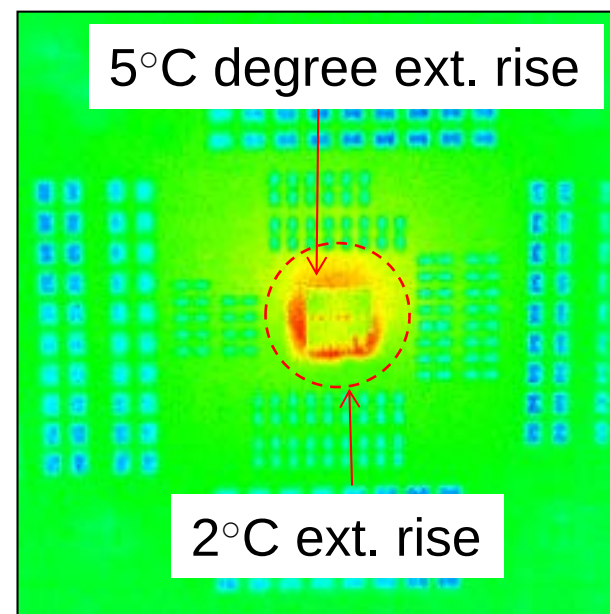
Two Critical Issues

- **Delivery of High Power in Fine Pitch**
 - Best Configuration depends on Power Pin Location
 - Lowest Inductance Path may no longer be the upper planes in the board.
- **Power Delivery Response to Transient Currents**
 - Power Decoupling to Differential pins mainly influences Common Mode Droop
 - Fmax testing / scan chain Fmax testing

Power Delivery



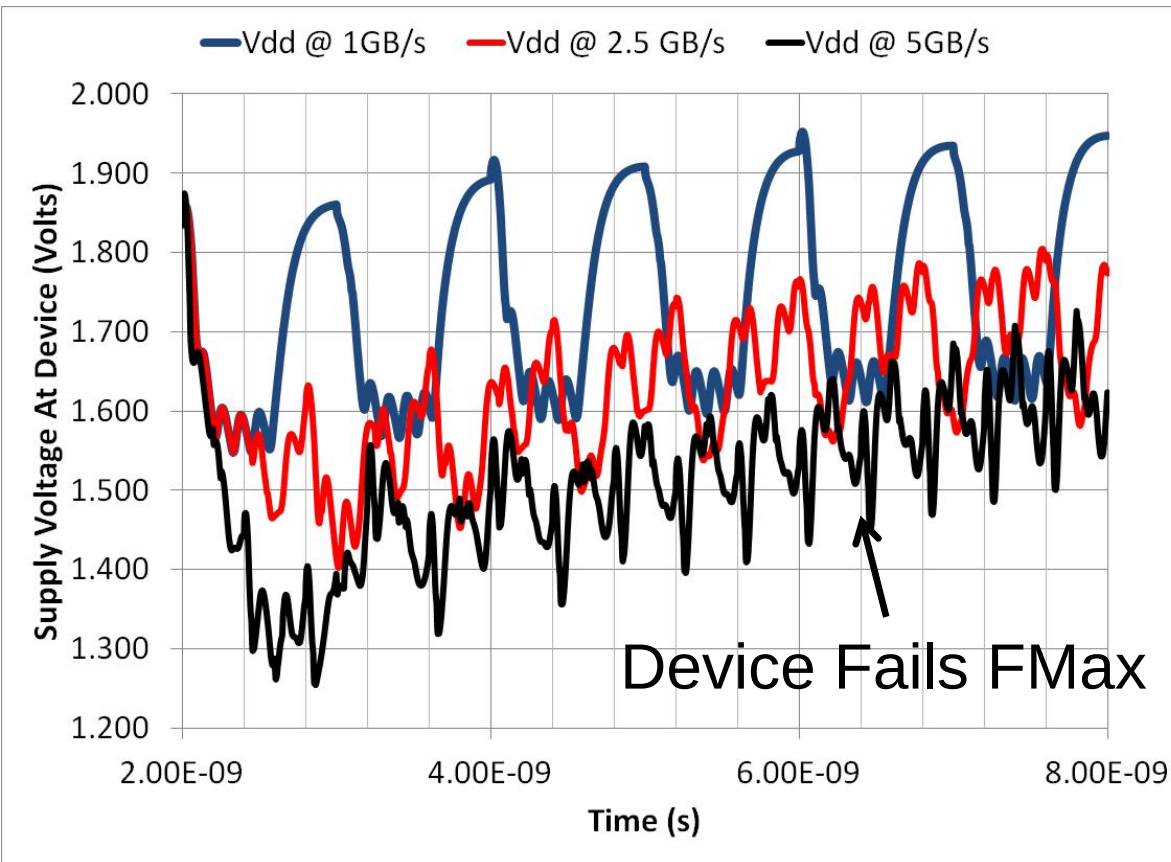
88 amps in 0.4mm pitch
Maximum Safe Point: 150 Amps @105 °C



(Flir T620)

Power Delivery

Transient Current: Multi-gate CMOS Chain



Assumptions:

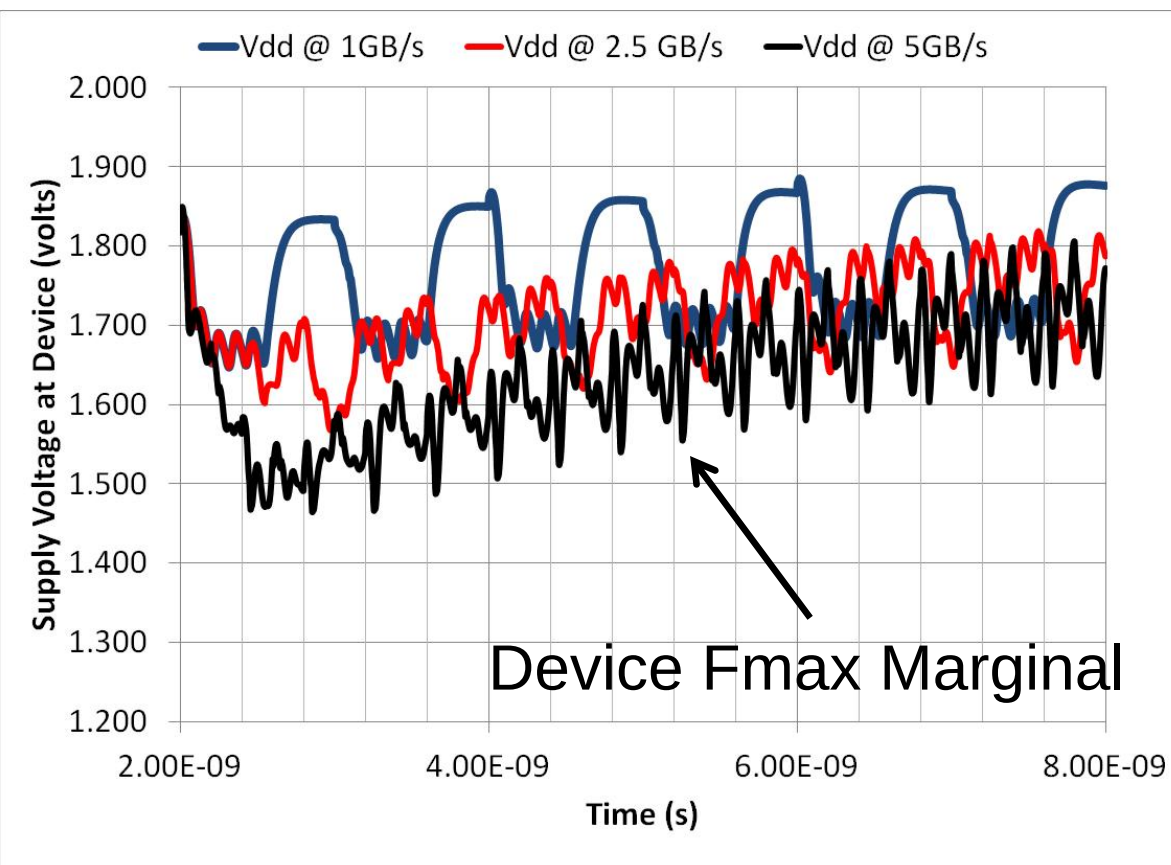
1. 10+ Million Gates
2. 2.5 million operational / 100 gate chain
3. 80 power pins
4. 320 ground pins
5. 0.95nh socket inductance / pin
6. 1.05 nh board inductance/ pin

Gate Models Courtesy of MOSIS



Power Delivery

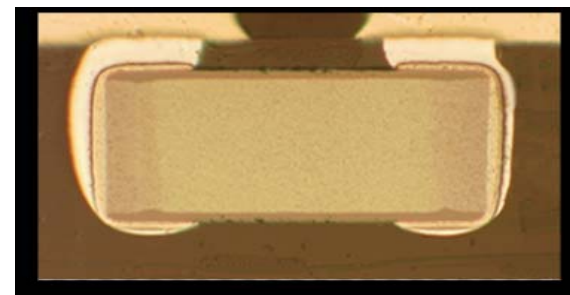
Transient Current: Multi-gate CMOS Chain



Improved Setup:

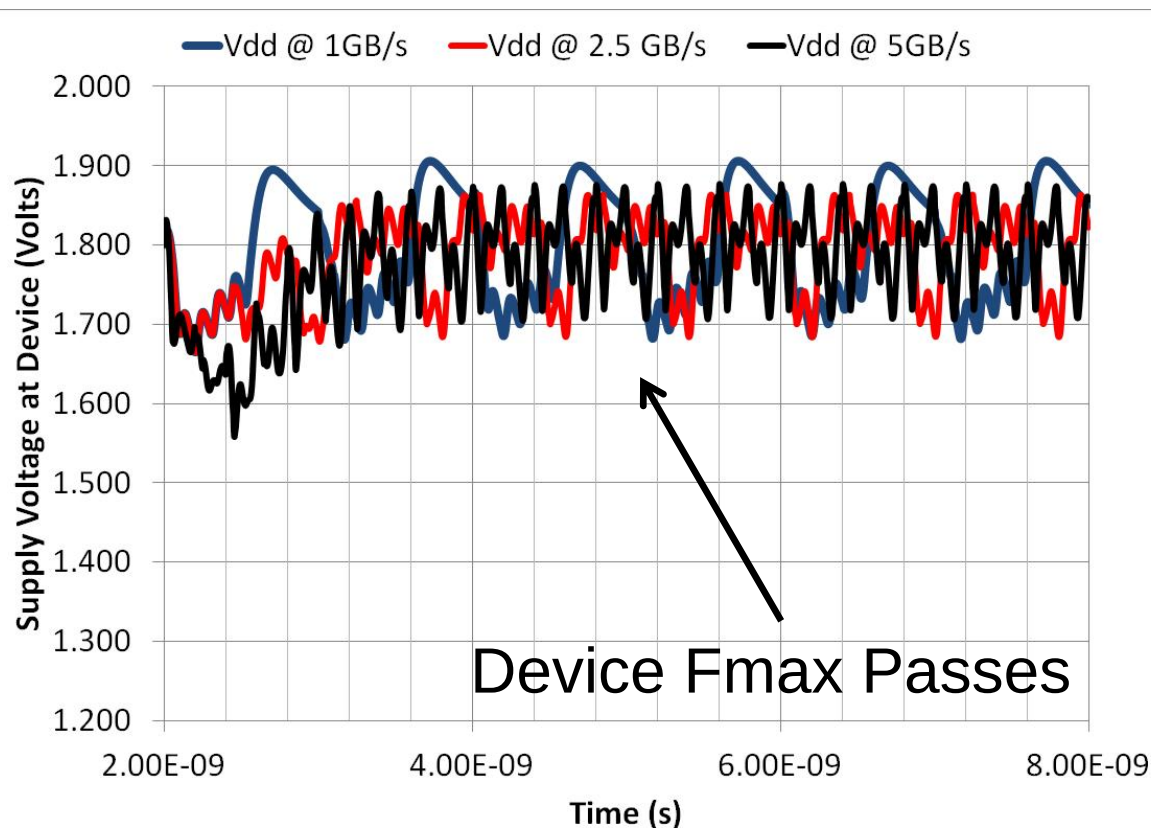
1. Embedded Decoupling

Embedded Capacitor



Power Delivery

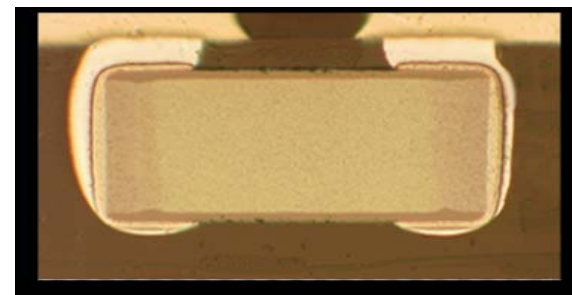
Transient Current: Multi-gate CMOS Chain



Improved Setup:

1. Embedded Decoupling
2. 0.1nh socket inductance / pin

Embedded Capacitor



Concluding Comments

- Socket and loadboard Issues previously ignored must now be considered.

- Critical issues:
 - Maintain a Smooth Loss Curve
 - Via structure
 - Via Entry
 - Socket to Via Path
 - Power Delivery
 - Board to Board / site to site consistency