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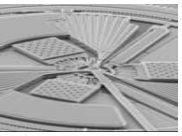
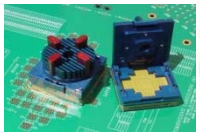





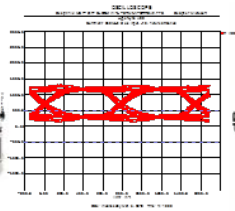
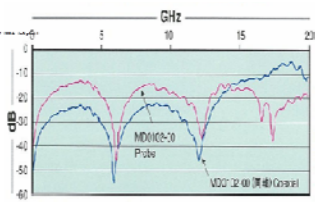

Embedded DRAM: Test Challenges and Methods

Craig Soldat
Cisco Systems, Inc.

Overview

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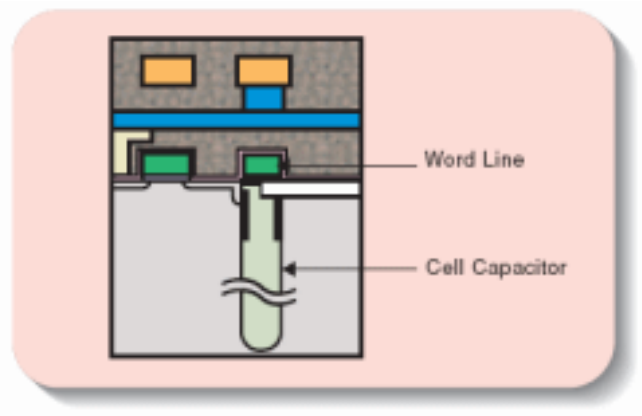

- Why Embedded DRAM
- Testing Challenges
- BIST- minimum requirements
- BIST- accessibility
- DRAM Hold Time- background
- Hold Time measurement challenges
- Conclusion

Why Use Embedded DRAMs

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1. Density Advantage
2. Bandwidth Advantage
3. Power Advantage

Historically eDRAMs were not always possible-

Embedded DRAM process improvements occurred to enable a logic based eDRAM process

Caveats

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Trade Offs

Cost:
Fabrication costs and increased die size costs

Leakage:
Maintenance operations- Refresh

Architecture:
Hold time issues (SEU, VRT)

Memory Test Motivations

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Standard Motivation- “Is the device good”

Unique design and fabrication attributes for memories

- Memories have the densest layouts
- Memories are very susceptible to
  - Systematic process variations
  - Random defects

Memory cores are analog designs that are combined with a digital interface creating a broad spectrum of fault models

Testing Challenges- Embedded Memory Accessibility

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External Test Access

- Not always possible
- When Possible:
  - Access is rarely direct
  - At-speed access not always possible
- Exercise Memory w/ Algorithmic Pattern and Non-Algorithmic Pattern

Internal Test Access

- At-speed test
- Topological Pattern Execution
- Algorithmic Pattern only
- Test portion of memory core at a time

BIST Engine Designs

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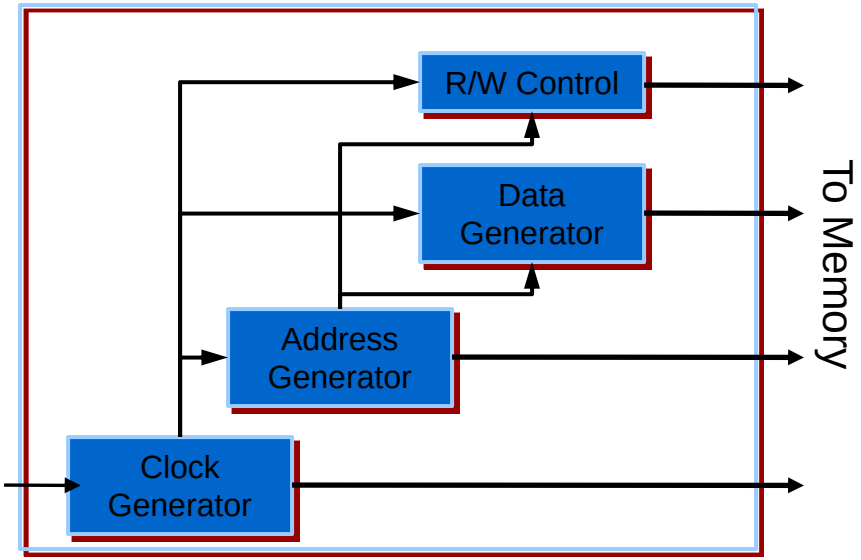
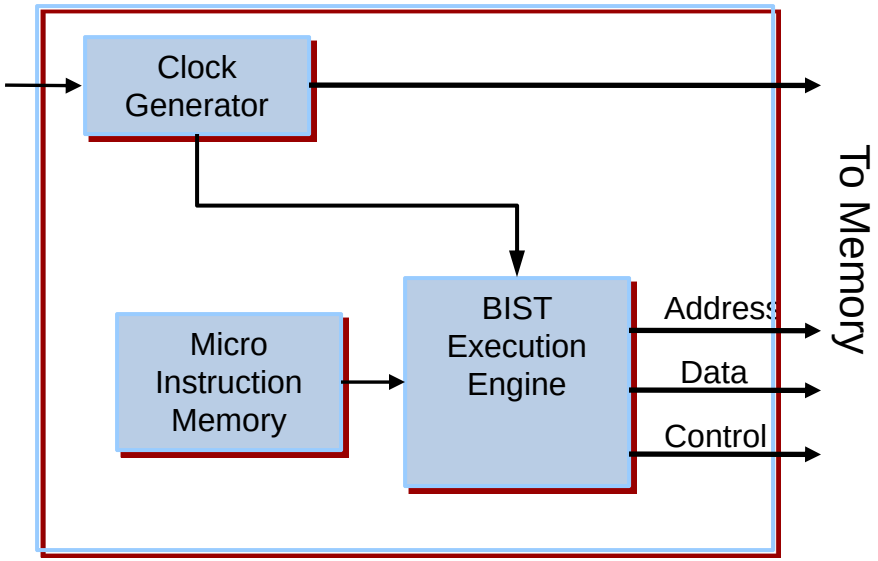
FSM BIST Engine



Microcoded BIST Engine



Algorithmic Patterns

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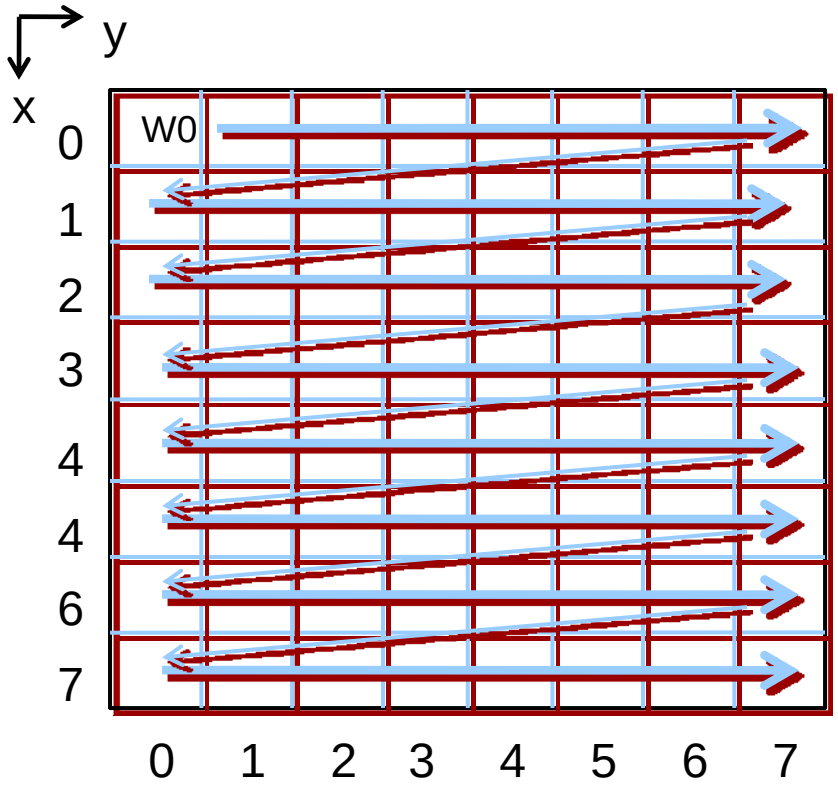
One or more loops of a counting sequence of addresses where one or more device operations occur for each address step.




```
for (x= 0; x < XMAX; x+=1)
{
    for (y=0; y < YMAX; y+=1)
    {
        Write 0
     }
}
```

Programmable Memory BIST

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Minimum Execution Capabilities

To support algorithmic loop execution the BIST must support:

- Address step in a positive or negative count direction
- Write or read programmable data-word or complement
- Perform one or more memory device Ops per address step
- Definition and Execution of Multiple Loops in one execution

Programmable Memory BIST

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Error Reporting Capabilities

Good:
Detect incorrect data received from the device
Failure Flag
First Failing Address and Data Bits

Better:
Number of failing bits
Number of failing addresses
First 1K Failing Addresses and Data Bits

BIST Applications

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Mbist Primary Mission:

1. Locate bad cells
2. Validate Address Decoders
3. Ensure Control Functionality
4. Test Data Sensing
5. Test Write Capability

Additional Mbist Application:

Leverage BIST to validate and characterize the ability of eDRAM cells to hold their data.

DRAM Cell Hold Time

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Charge stored in DRAM cells leaks away
Data represented by the stored charge is lost
> periodic “refresh”

ASIC must be designed to periodically refresh the eDRAM core to keep the data stored in the memory intact.

Hold Time Variations

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Cell Hold Time Variation:

- Voltage
- Temperature
- High Energy Particles (SEU/Soft Error)
- Xrays
- Design variation
- Process variation
- Device Aging
- Variable Retention Time (VRT) – Random!

Hold Time Measurement

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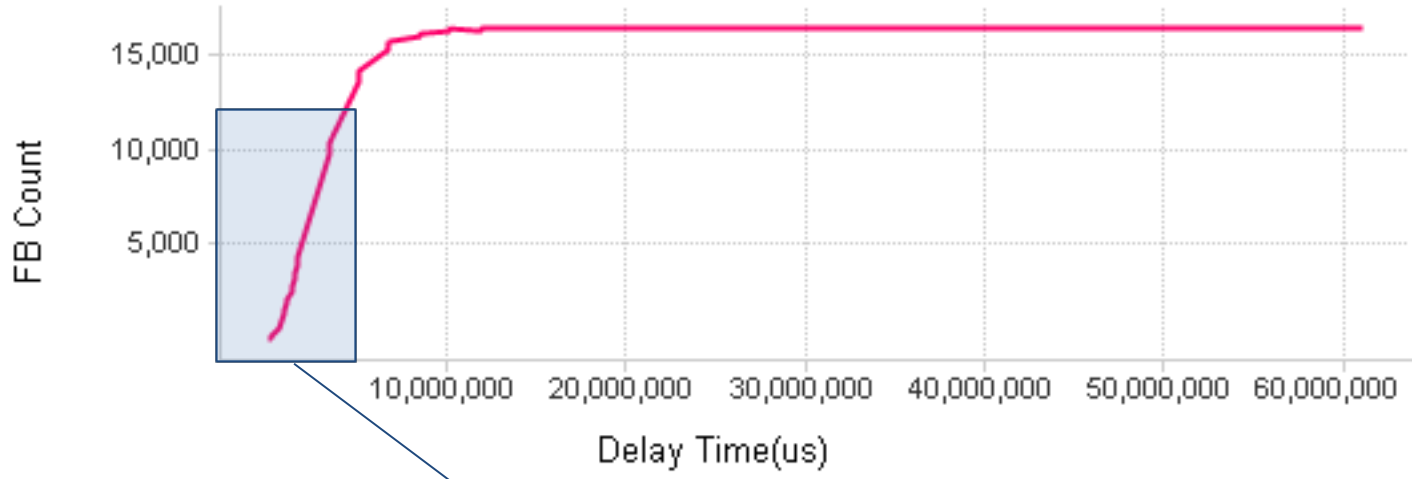
Hold Time (cell or region)

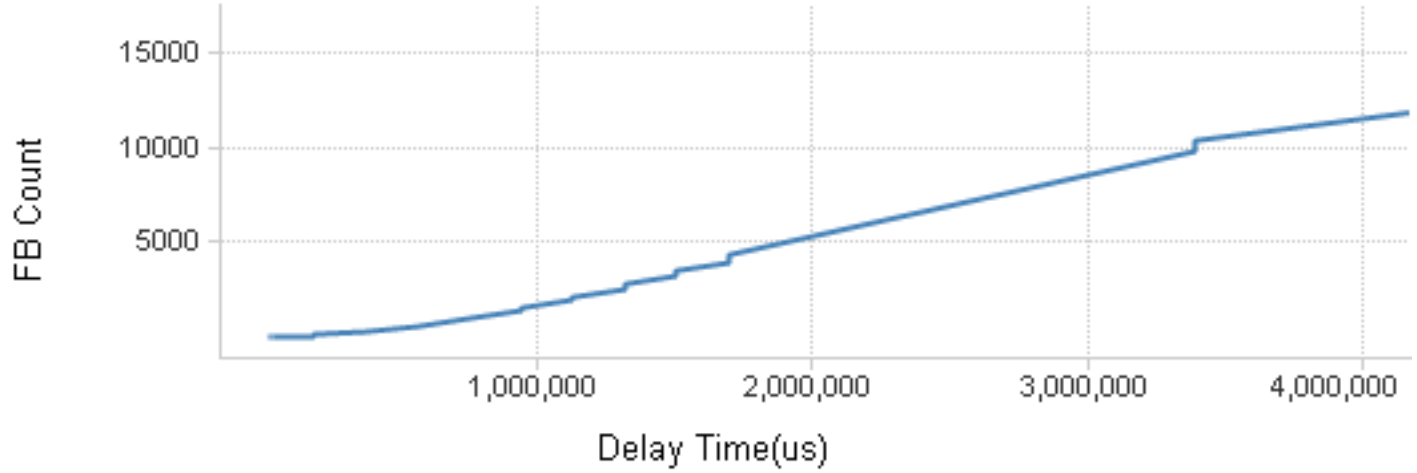
1. Writing data to the cell
2. Waiting for a time interval
3. Reading the cell
4. Check Read Results
5. Repeat w/ varied time interval

Hold Time Profiler

1. Profile data retention times until fail bit count saturates



2. Focus further searches on tail.



Hold Time Profiler

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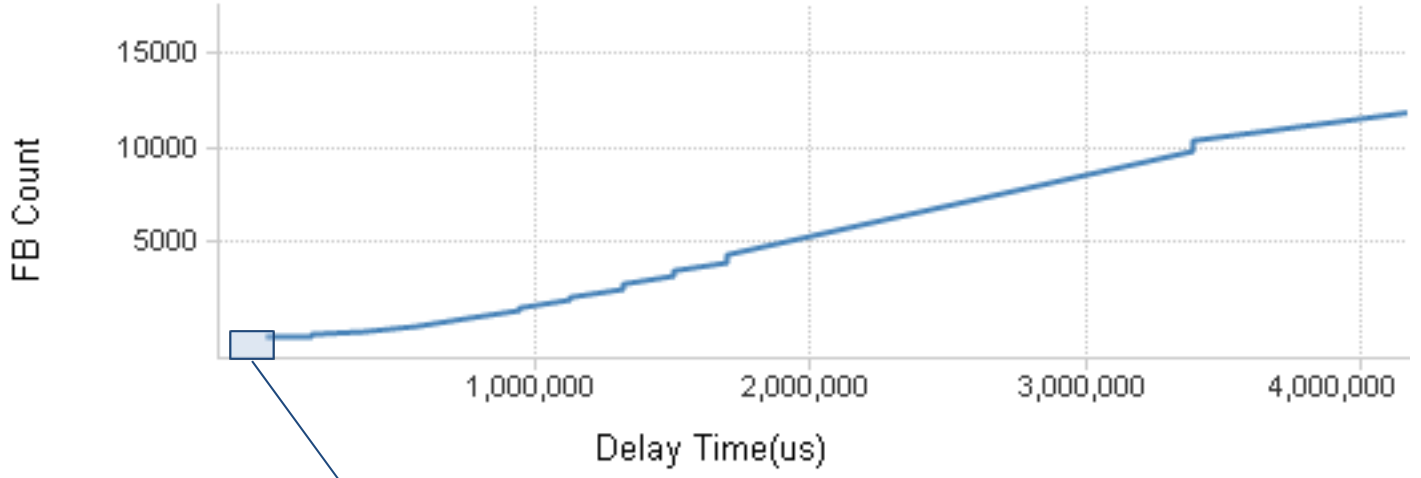
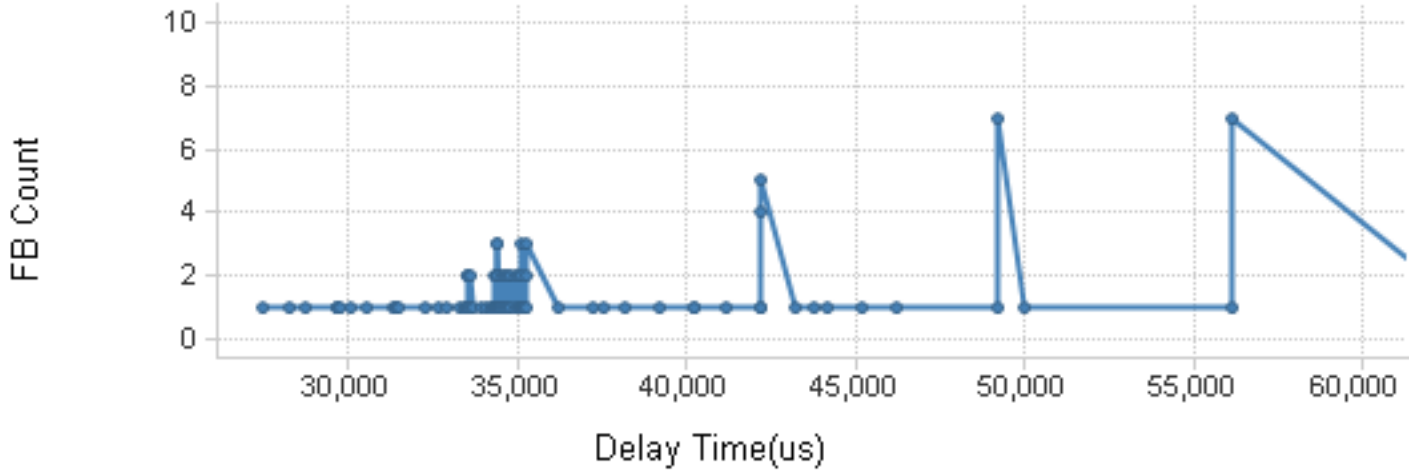
3. Focus further searches on tail



4. Search for instable region of tail



Hold Time Profiler

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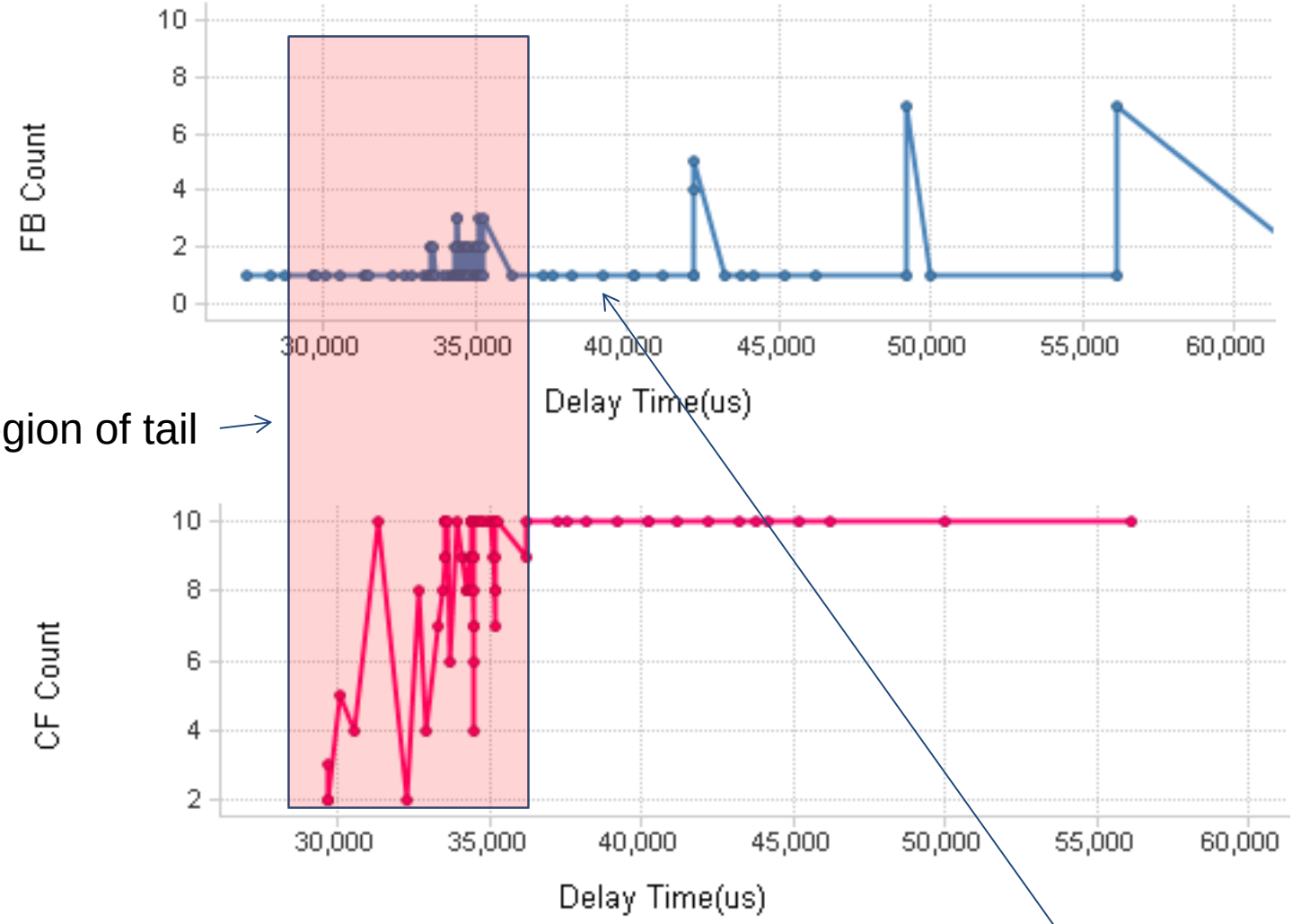
5. Search for instable region of tail.



Instable region of tail

6. Intensively profile stable region of tail.

Conclusions

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eDram – many advantages, but some disadvantages

eDRAM Test Challenge Introduction – BIST overview

A Memory BIST Engine is traditionally used to detect failing cells in the memory core. We have extended the use of the BIST engine to the characterization of an embedded memory core's Hold Time

Hold Time profiler and it's methodology was shown