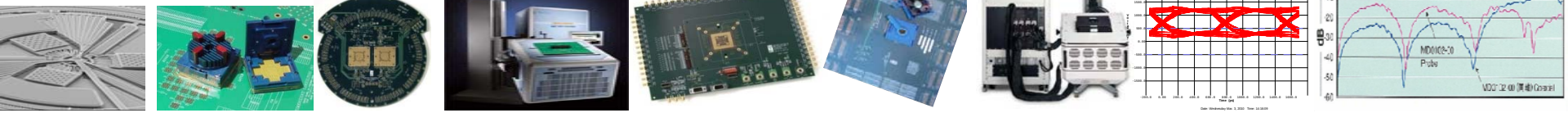


Broken Scan Chains Routinely Debugged with New Optical Technique

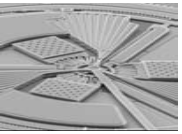
C. Kardach, DCG Systems Inc.
cathy_kardach@dcgsystems.com

Overview

- Status of LVI-based scan chain debug
- LVx Architecture
- Scan chain map generation
- Fabless/foundry chain debug workflow
- Review: 40 nm stuck-at case study
- Current work: transition failures

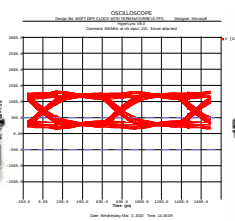
DCG Systems

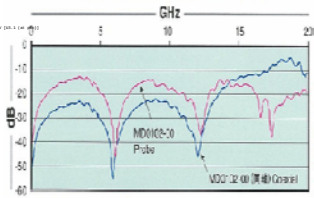
Silicon Valley Test Workshop









Status of LVI-based scan chain debug

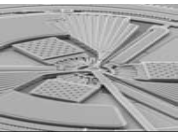
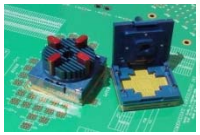
Status of LVI-based chain debug

Silicon Valley Test Workshop

- Proof of concept on 40nm packaged parts (NVIDIA, 2010)
  - 3 die for PFA; defect found on all 3
- Yield ramp on 28nm packaged parts (NVIDIA, 2011)
  - 47 die analyzed with LVI/LVP and sent for PFA
  - To date PFA on 34 die and only 3 missed defect
- PFA success rate >90%

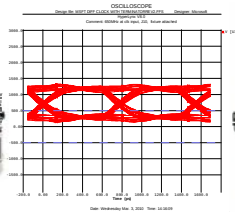
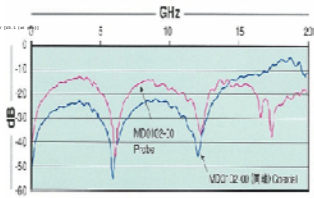
DCG Systems

Silicon Valley Test Workshop





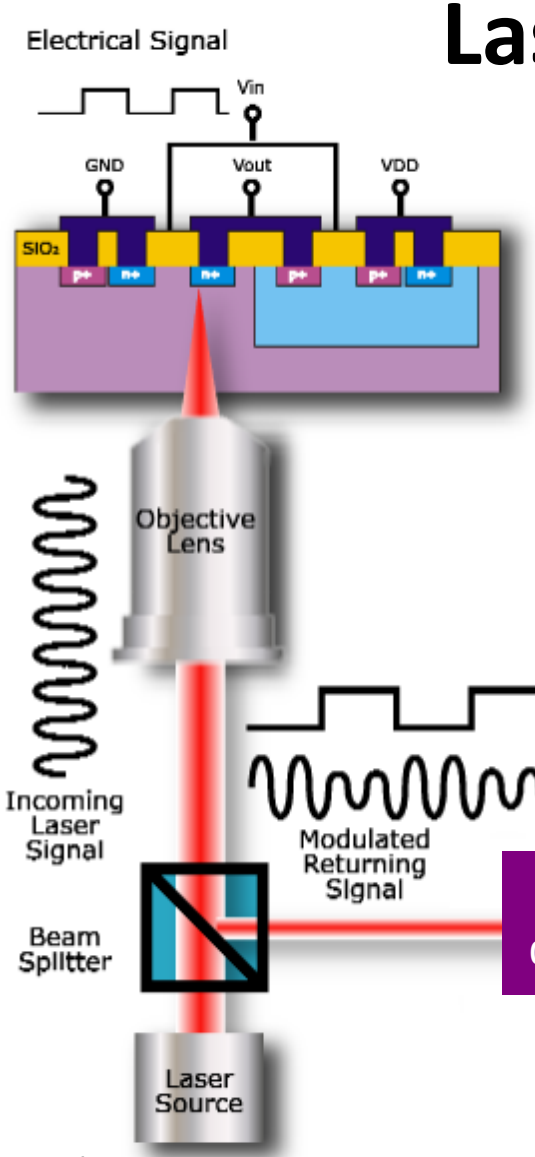



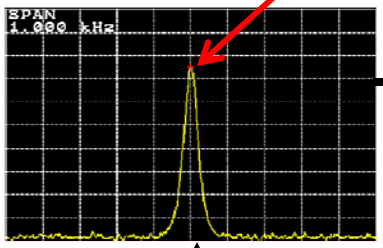
LVx Architecture

LVI[1]

Laser voltage imaging

Silicon Valley Test Workshop





Spectrum Analyzer

target frequency

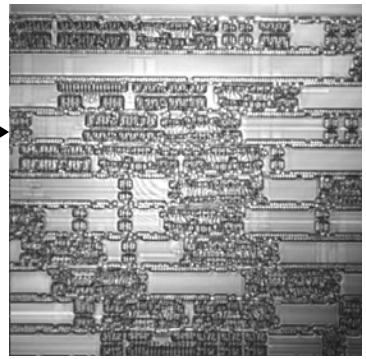
LVI image @ target frequency

RF Component

photo-detector

RF amplifier

DC Component



LSM (reflected) image

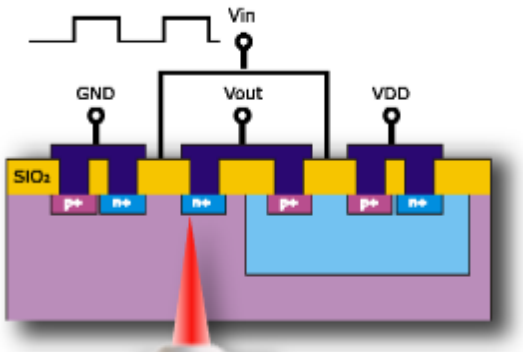
[1]*DCG patents granted*

DCG Systems

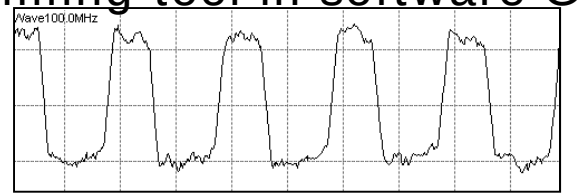
LVP

Laser voltage probing

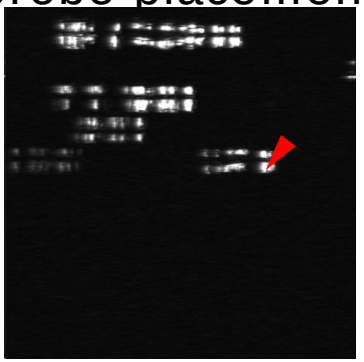
Electrical Signal



Timing tool in software GUI



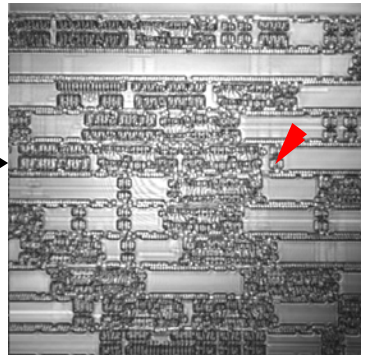
LVI image can be used for optimal probe placement



Trigger → digital scope

RF Component

LSM (reflected) image



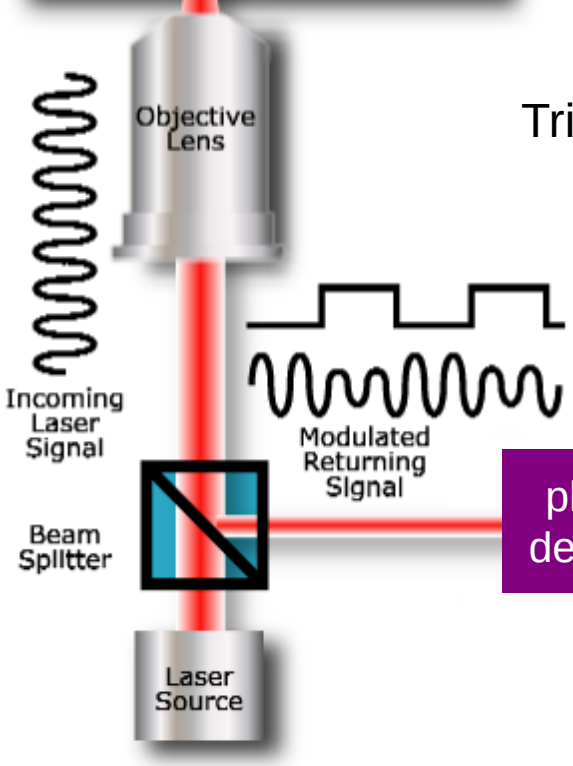
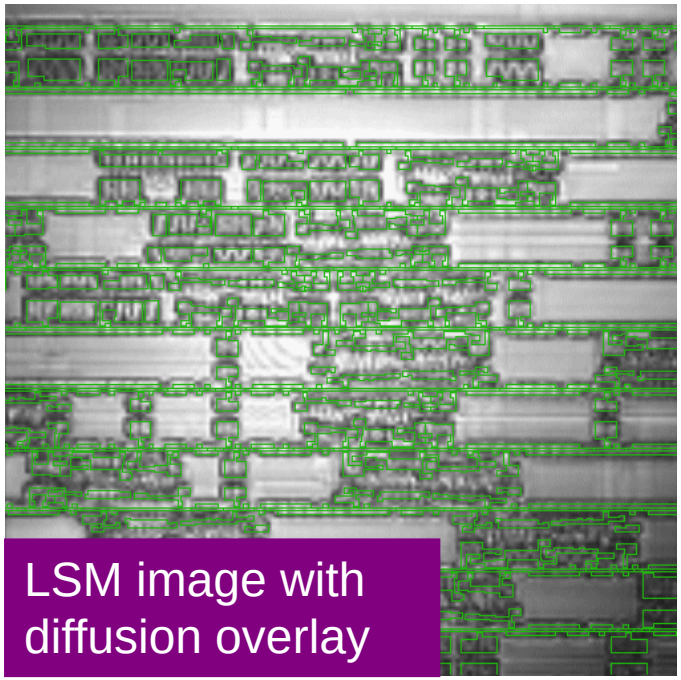


photo-detector → RF amplifier → DC Component

CAD-to-LSM-to-LVI registration

- Diffusion layers used for LSM-to-CAD alignment
- LVI & LSM images acquired simultaneously for 1-pixel accuracy

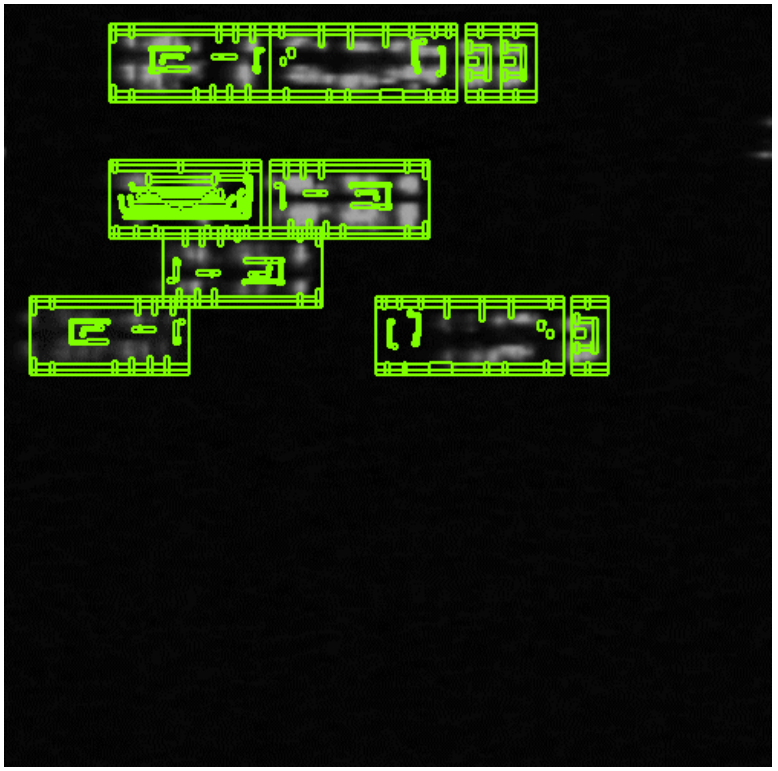


LSM image with diffusion overlay

LVI image with same overlay

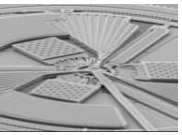
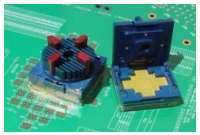
Load cell bounding boxes

- Accurate overlay of scan flop bounding boxes critical
- Cell bounding boxes generated by design house using LEF/DEF



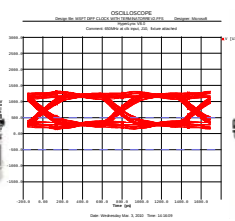
DCG Systems

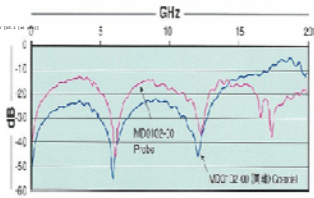
Silicon Valley Test Workshop





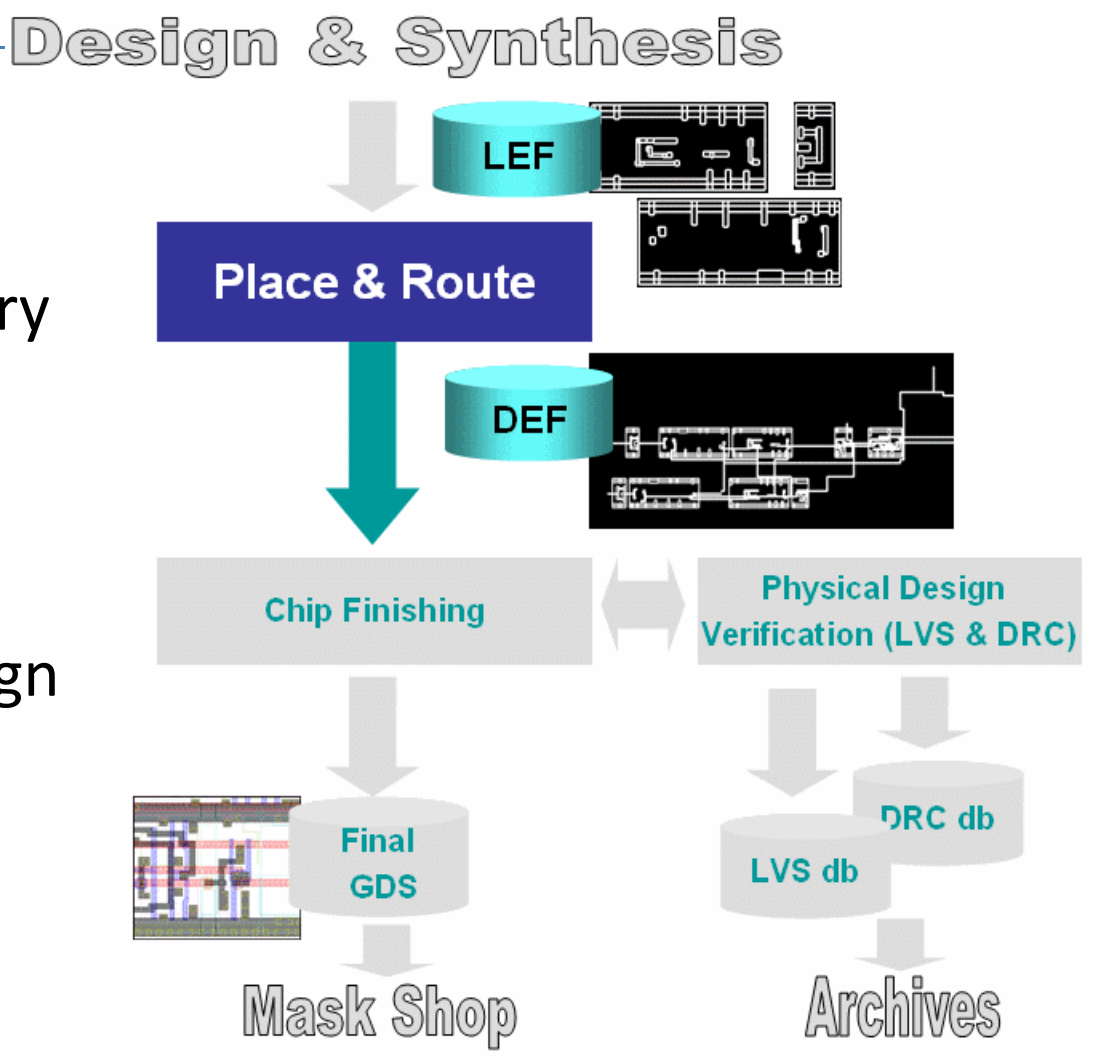




Scan chain map generation

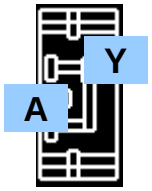
LEF/DEF in the chip design flow

- LEF – Library Exchange Format
- DEF – Design Exchange Format

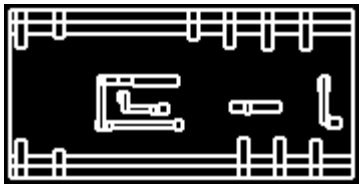


LEF/DEF Basics

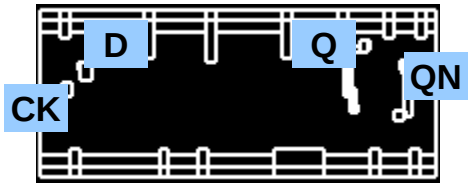
LEF is a library of cell types and their pins



INVX3

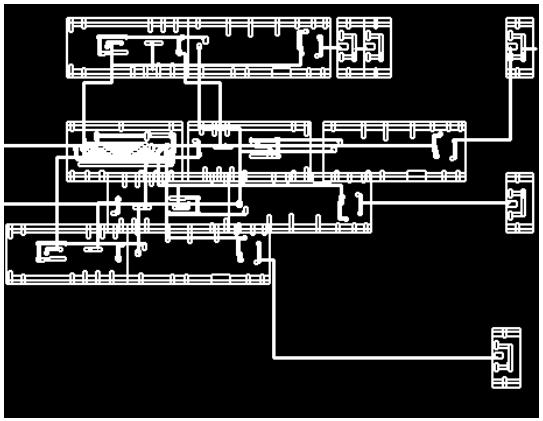


NAND4X4



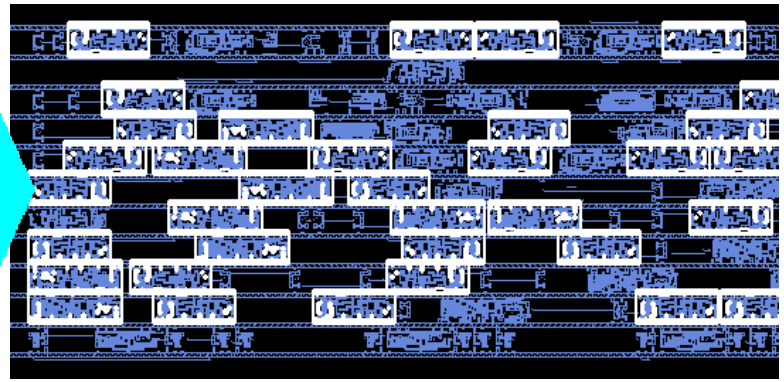
DFFX2

DEF contains the cell placements and routing and annotation



Flop names are translated

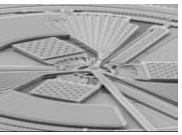
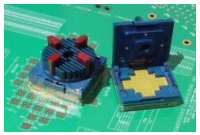
```
Scan path for chain=chain0: begin_position=SCO, end_position=SCI
gate_type   cell_id   cell_type   inv   instance_name (type)
---------   -------   ---------   ---   ------------- ------

DFF  ---     ---     ---     i_so2/cntr/c1/d2          SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlata/b4            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b0            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b1            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlata/b3            SDFFHXQ2
DFF  ---     ---     ---     i_so2/div4/d1             SDFFHXQ2
DFF  ---     ---     ---     i_so2/div4/d2             SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlata/b1            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlata/b2            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b3            SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c1/d0          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c1/d1          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c1/d2          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c1/d3          SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlata/b0            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b4            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlata/b7            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b5            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b6            SDFFHXQ2
DFF  ---     ---     ---     i_so2/dlatb/b7            SDFFHXQ2
DFF  ---     ---     ---     i_so2/clkdiv/d1           SDFFHXQ2
DFF  ---     ---     ---     i_so2/clkdiv/d2           SDFFHXQ2
DFF  ---     ---     ---     i_so2/clkdiv/d3           SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c2/d0          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c2/d1          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c2/d2          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/c2/d3          SDFFHXQ2
DFF  ---     ---     ---     i_so2/cntr/d8             SDFFHXQ2
```



GDS viewer

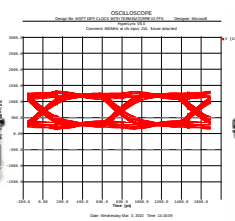
DCG Systems

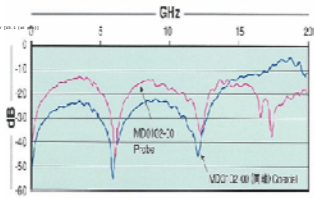
Silicon Valley Test Workshop



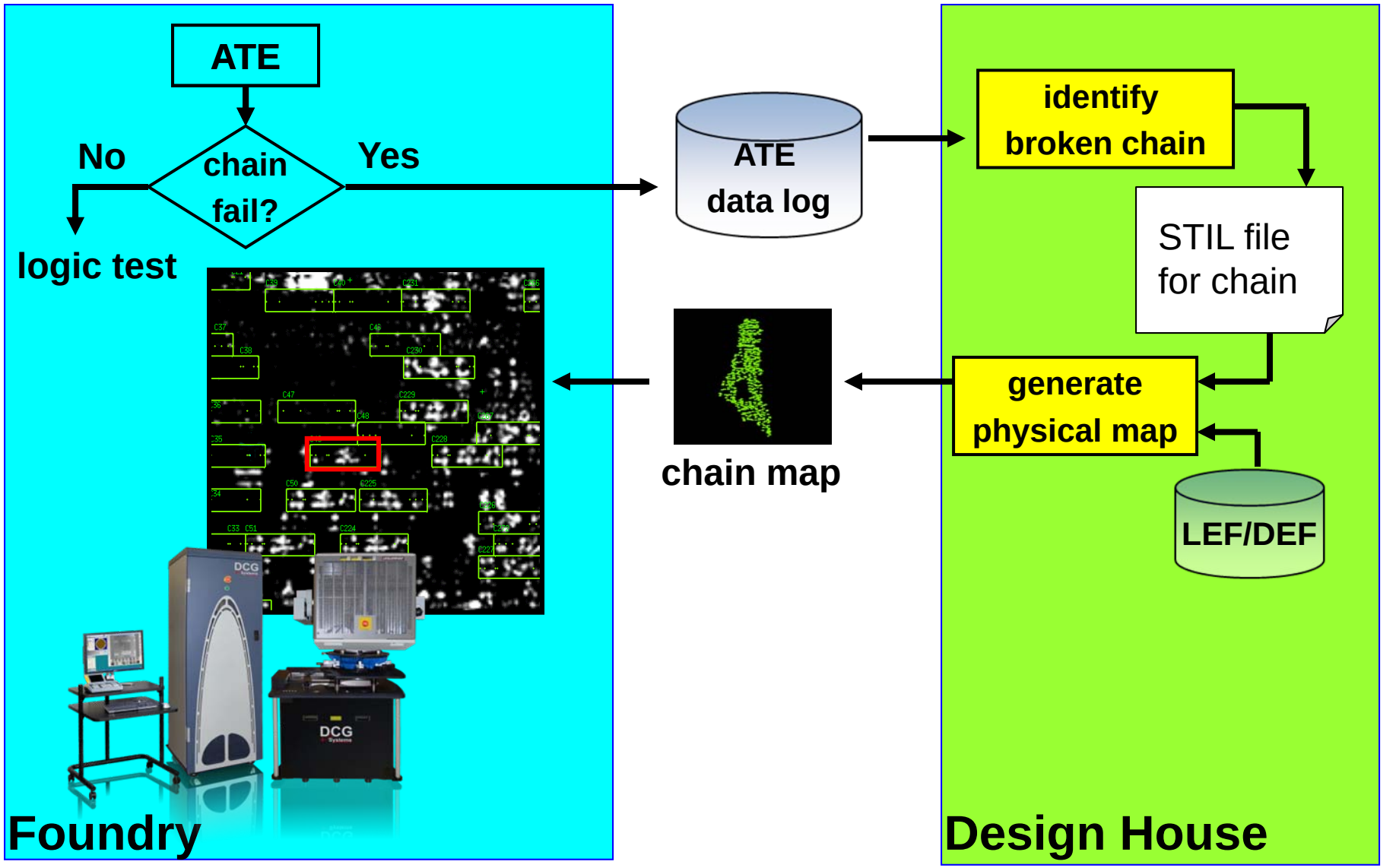






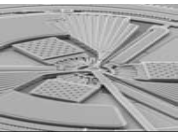
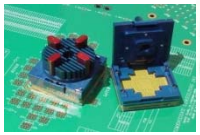
Fabless/foundry chain debug workflow

Fabless/foundry chain debug



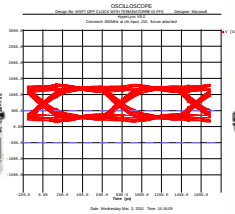
DCG Systems

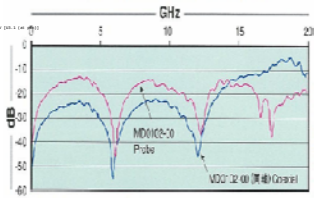
Silicon Valley Test Workshop







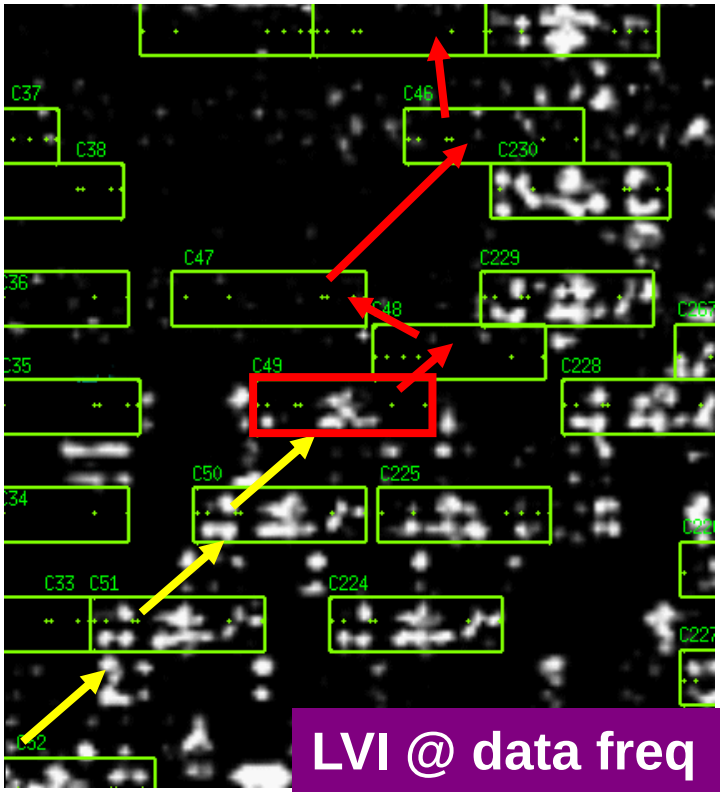


40 nm stuck-at case study

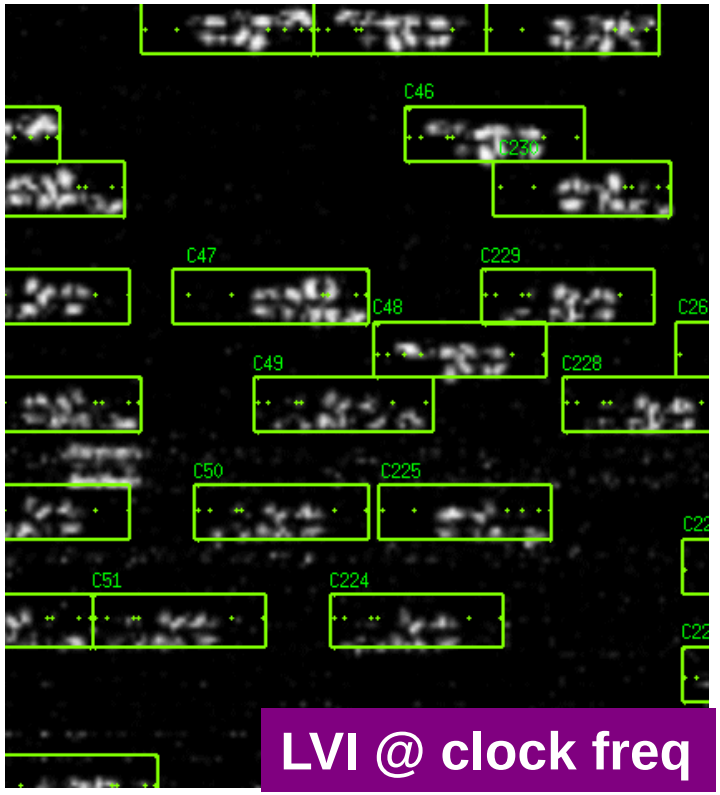
Case Study Introduction

- Chip is 40nm CMOS Graphics Processor Unit (GPU)
- The failure was identified on a production compressed shift pattern
- 11001100… pattern through chain and looped
  - Scan clock = 11 MHz
  - Scan data = ¼ scan clock = 2.75 MHz
- Binary search on LVI-data and –clock images

Final images on 40nm case study

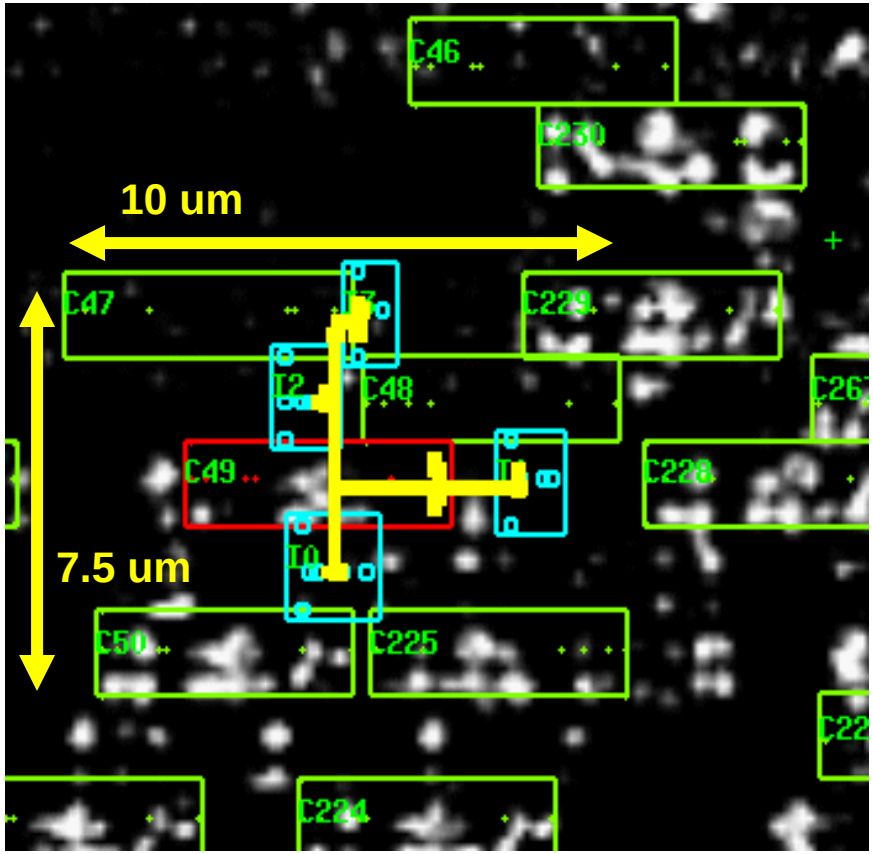


LVI signal degrades in #49



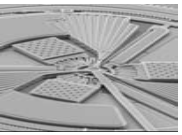
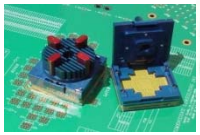
All flops have clock signal, even data-starved flops

Trace fan-out in GDS



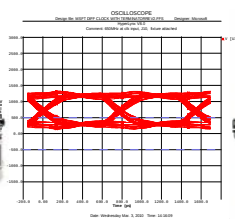
DCG Systems

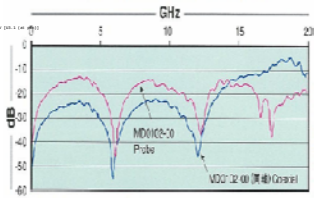
Silicon Valley Test Workshop







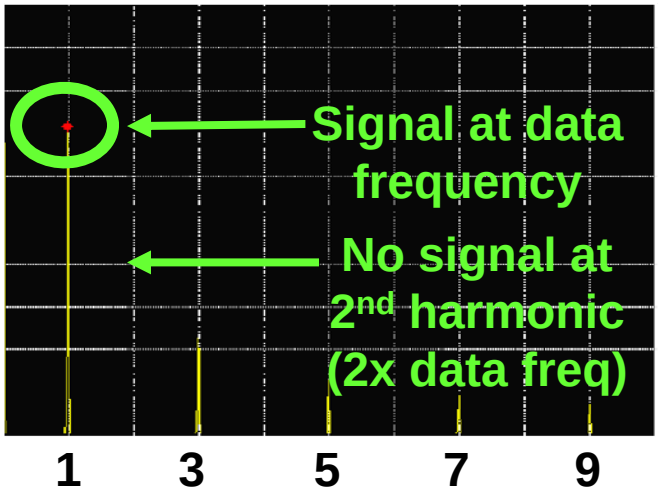


Using LVx to debug transition failures

11001100… -> 10001000…

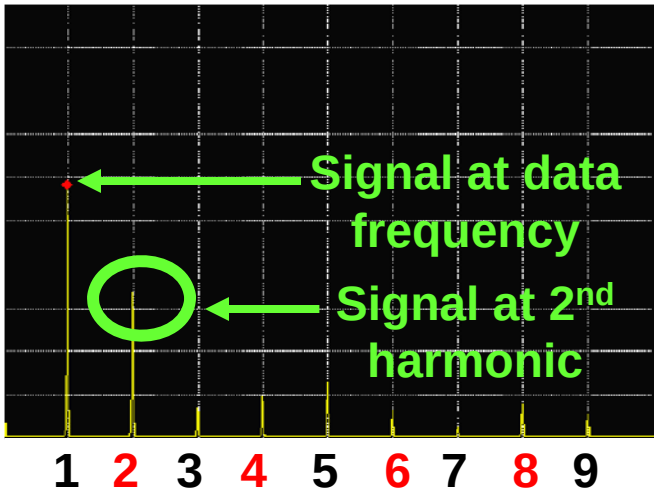
2nd harmonic finds transition failures

Spectrum for input pattern of 11001100… (50% duty cycle)



Only odd harmonics are present at 50% duty cycle

Spectrum for output (fail) pattern of 10001000… (non-50% duty cycle)



Even harmonics appear at non-50% duty cycle

Transition failure debug strategy

- Probe scan chain output with LVP to verify the pattern has changed to 10001000…
- Tune the spectrum analyzer to the 2nd harmonic of the data frequency
- Continue binary search using LVI to find transition from dark flop (good) to bright flop (bad)

Transition failure method: results

- NVIDIA debugged 7 transition failures using LVx
- Transition failure case study to be presented at ISTFA 2011 in San Jose, CA:

S Kasapi, W Lo, J Liao, B Cory, H Marks, "Advanced scan chain failure analysis using laser modulation mapping and continuous wave probing."

Conclusion

- LVI-based scan chain debug: highly successful in driving yield at 28nm
- Fabless/foundry data exchange: easily adoptable, based on open formats (LEF/DEF and GDS)
- LVI in 2011: moved beyond stuck-at failures
- Broken Scan chain debug: transformed from very difficult to very easy due to LVx methodology

Acknowledgements

Dr. Steven Kasapi invented modulation mapping, and now at NVIDIA has proven its effectiveness for scan chain fault isolation

Dr. Joy Liao has been a key facilitator at NVIDIA in transitioning methodology to foundry yield operations

Special thanks to NVIDIA managers that invested time and capital to make this technology a viable yield driver:

Bruce Cory, DFx Manager, NVIDIA

Howard Marks, Silicon FA Lab Manager, NVIDIA